COMITETUL DE STAT PENTRU ENERGIA NUCLEARA

INSTITUTUL DE FIZICA ATOMICA

NE-16-1974

# DATA ACQUISITION SYSTEM FROM UNCORRELATED EXPERIMENTAL INPUTS

I.BALS, M.CAPRINI, B.GORAN, S.LUTESCU

AND D.NICULESCU

Bucharest - ROMANIA

# DATA ACQUISITION SYSTEM FROM UNCORRELATED EXPERIMENTAL INPUTS

I.Balş, M.Caprini, B.Goran, S.Lutescu, D.Niculescu

Institute for Atomic Physics, Bucharest, Romania

## INTRODUCTION

The increase of the complexity of the available data in nuclear physics experiments made necessary the development of some systems for acquisitions,sorting and preliminary processing of the data.

Generally there are two ways of doing this: either using small computers accordingly interfaced, or developing specialized systems.

The system described in this work was performed as a small acquisition center for neutron physics experiments and was designed as a specialized device.

This device can collect data from maximum 16 uncorrelated experimental inputs and store them in a 4K memory. For each experiment is reserved a storage zone of $2^k$ x 64 bits (k= 1,2,3,4).

The experimental data are of two kinds - from 12 inputs serial data and from the rest of 4 inputs - data of parallel type.

The data of serial type are stored in successive address-

es, each address storing the number of pulses received in a time interval between start and stop pulses (multiscaler mode).

The parallel data are supplied by a measuring device,being stored in successive addresses at external control signals.

The system has also some others capabilities as : manual introduction of the data in the memory, algebraic sum of the contents of the two zones of the memory. The content of the memory can be displayed in analogic form on a CRT and on a xy recorder and in digital form on CRT printed paper and punched tape. It is also possible to monitor the experiment displaying the accumulated spectrum in a certain zone during data acquisition.

SYSTEM ARCHITECTURE

The features of the system imposes an architecture similar to small computers.

The main units of the system are : memory unit including corresponding circuitry, arithmetic unit, interfaces for experimental units (serial inputs and parallel inputs), CRT display,interfaces for data output and control unit (fig.1).

Some modern principles of data handling have been used to solve problems related to interconnection among system units /1, 2/. Thus the information flow among system units uses a bus structure, the input interfaces have a modular structure, the control unit is built up by programming units connected through a bus structure.

The data are stored in core memory in binary two's complement form, that have been picked up for arithmetic operations

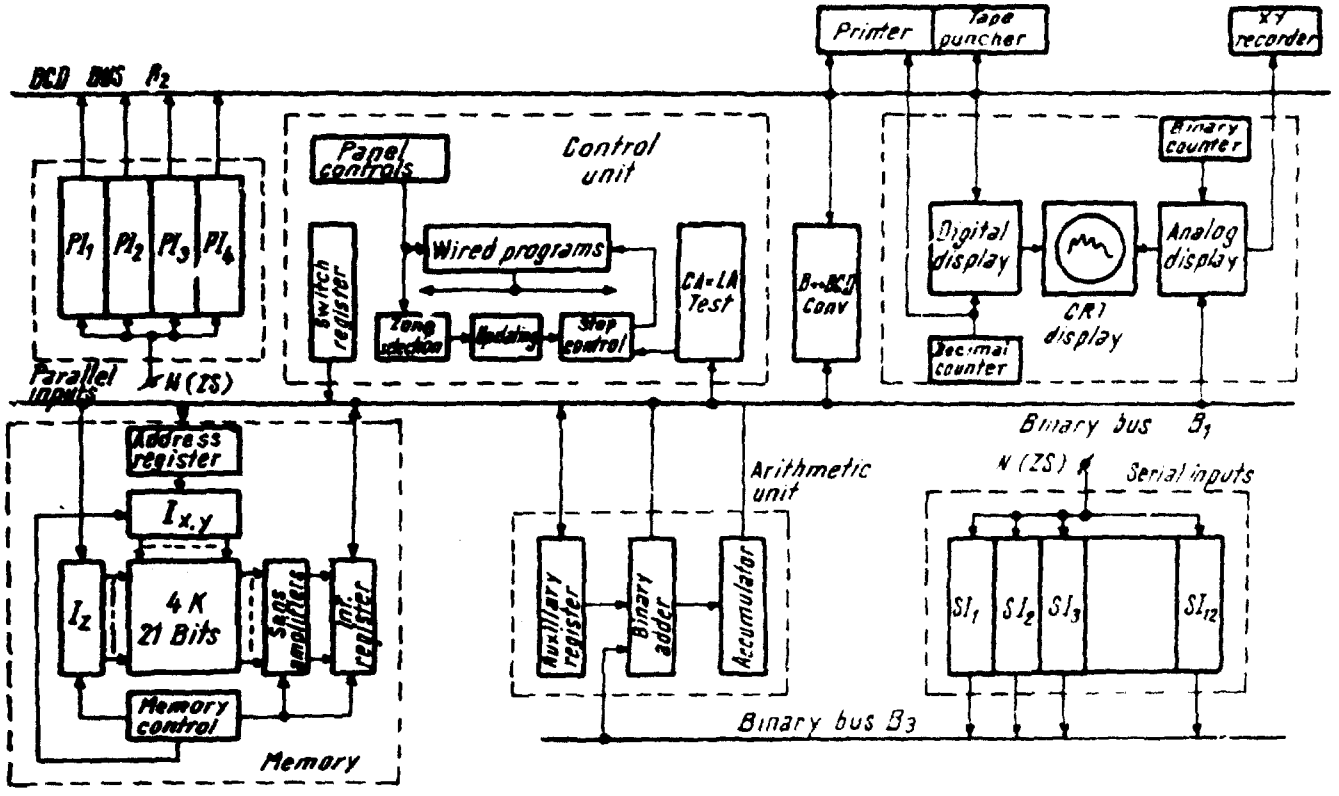


Fig.1.
System architecture.

reasons. The link among memory registers, arithmetic registers and analogic display is realized by B1 binary bus. The parallel inputs deliver decimal data; the decimal code is also used for digital display on CRT, printer and paper-tape puncher. The B2 bus is used to interconnect transducers. Information transfer between B1 and B2 buses is realized by means a BCD to binary and binary to BCD converter. The multiplexer inputs have buffers (binary counters). These buffers are connected to arithmetic units by the B3 binary bus.

A wired memory is used to store controller command sequence (transfer among registers, operation with memory unit, synchronization of the system with input and output channels).

The microprogrammed organization of the system was preferred to the programmed one, because the last involves the controller commands to be stored as instructions into the memory unit. The reason consists in a shorter accumulation cycle, hence increasing the rate of data acceptance through experimental channels.

The memory unit preserves the first and last address of each zone, as well as current address. This allows an easy modification of zone dimension.

## FUNCTIONAL UNITS DESCRIPTION

### Memory Unit

The memory word is 21 bits long. Thus it can be stored numbers up to ($\pm 2^{20}-1$). The first 64 addresses are used to store first, last and current addresses for all zones (fig.2).

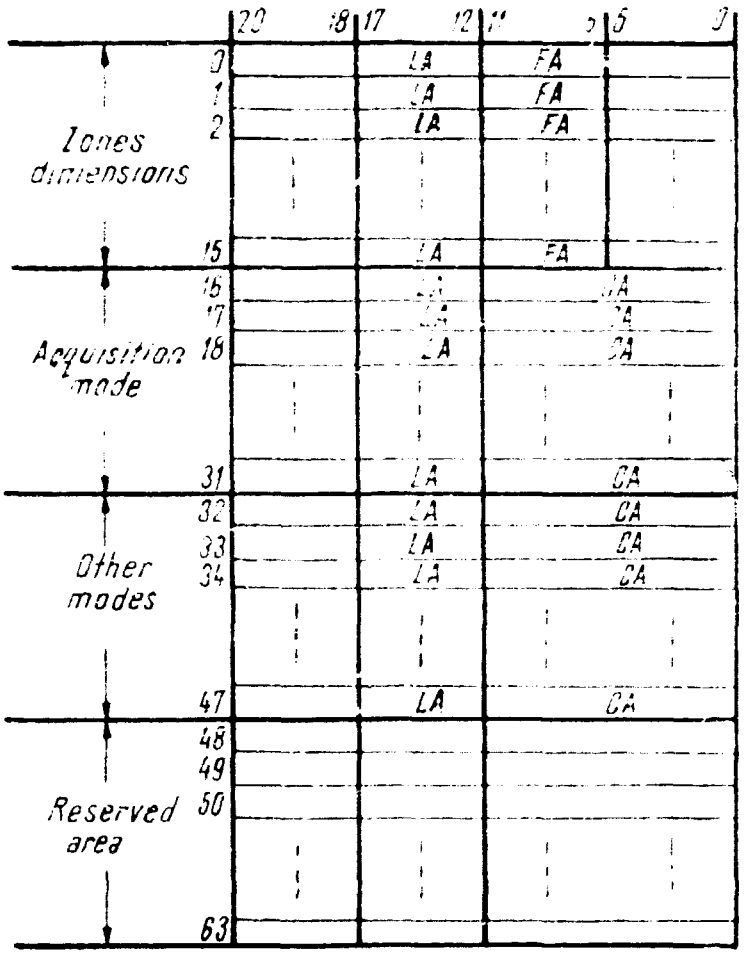


Fig.2.
Structure of the memory area used for zones dimensions.

The last and current addressed are stored in the same word, in order to be easily compared. The zone dimension are multiple of 64, so the last address is represented by its six more significant bits. The current address is 12 bit long.

The 0-15 words are used to store the last and first addressed for all zones; the 16-31 words to store final and current

addresses during data accumulation, the 31-47 words to store final and current addresses during other operation modes, and the 48-63 words are reserved for further developments. Two current addresses are used for each zone in order to enable a CRT display during accumulation.

The memory cycle is 3 μs.

Arithmetic Unit

The arithmetic unit is used during accumulation from serial inputs, in order to add the content of buffers existing in interface units to the content of the current address of a zone. The arithmetic unit performs an algebraic sum of the content of two given zones (address by address), transfering the result to another zone (spectra comparison operations or back-ground subtraction).

Another employment of the arithmeric unit is to increment current address, as well as to realize a bidirectional conversion between two's complement binary code - used to store data into the memory unit - and binary representation of number by magnitude and sign, used for binary to BCD conversion.

A parallel network realization for the arithmetic unit was imposed to achieve a short acquisition time. The typical addition time is less than 300 ns.

Input Interfaces

The uncorrelated character of data from the 16 experiments imposed some interfaces to organize a lossless data transfer to memory unit. CAMAC principles /1/ have been used to realize these interfaces.

The controller unit sequentially scans the 16 interfaces, by using individual wires. An "yes" answer from a given interface, sent on a Q bus-organized wire, is interpreted as an interrupt and initiates a data transfer from that interface unit to the main memory. This transfer is controlled by a wired accumulation subroutine. The scanning procedure has the advantage to avoid the searching for identification of the unit asking for transfer.

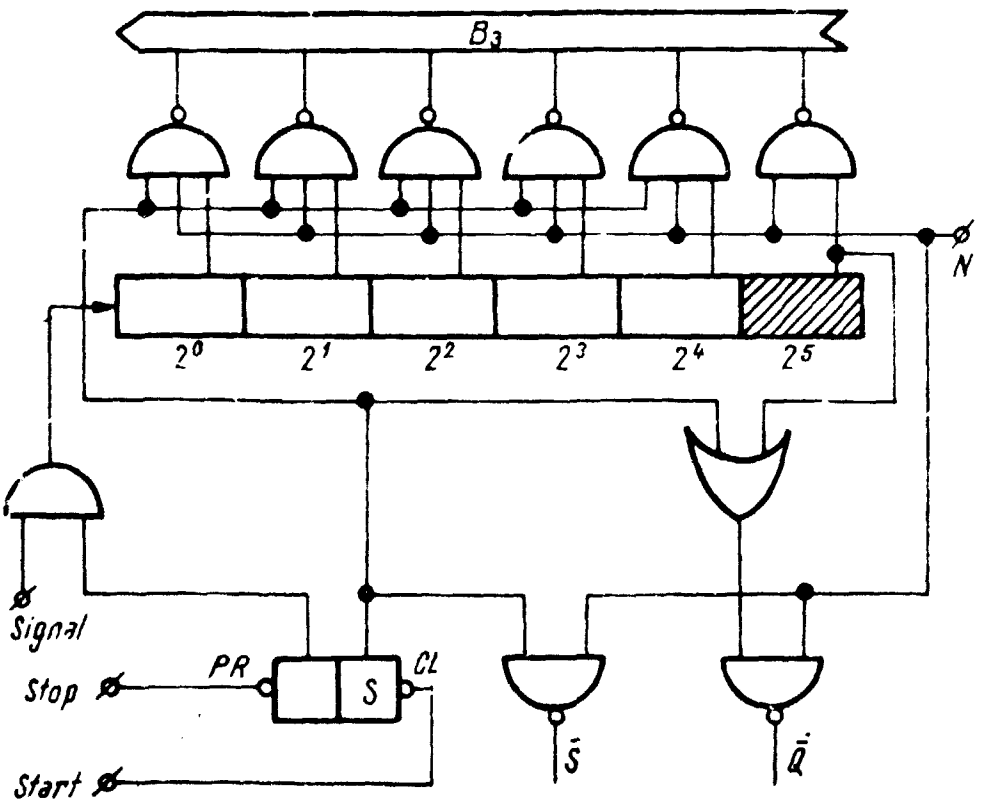


Fig.3.
Schematic diagram of serial input buffer.

An interface unit one for each of the 12 multiscaler - type inputs - contains a buffer, realized by a binary counter, designed to count pulses between START and STOP signals (fig.3).

When the most significant bit of the counter is 1 or when STOP pulse has arrived, the unit generates a data transfer request. Accumulation program, when initiated, adds - using the arithmetic unit - the current address content to the buffer content, represented either by the most significant bit of the counter-when the stop pulse did not arrive- or the whole content of the counter, when the STOP pulse has arrived. When a STOP pulse arrives, the $\overline{S}$ - bus turns on and the current address of the zone attributed to that input which generated the interrupt, is incremented.

The number of memory cells for the buffer (6) was established according to the input statistics and the duration of the accumulation program (25 μs). Besides the circuits presented in fig.3, there are phasing circuits for START and STOP signals, as well as circuits to disconnect the experimental channel without interrupting data accumulation from other experiments.

The transfer for parallel inputs has a slow rate. The interface units include code converters from experimental device code to BCD.

The information is passed through BCD-binary converter and sent to the memory, in a binary code, via B1 bus. The existence of two different buses allows the code conversion to be done while accumulating at the others inputs. The control signal for the data transfer operation to the main memory is generated at the end of the BCD-binary conversion. Therefore the system is kept busy for the data transfer from a parallel input for only 25 μs.

The bidirectional BCD-binary converter is used for parallel inputs data acquisition and for digital delivery of data.

Since in both these cases there is no restriction [illegible] was chosen a serial scheme using two 24 bits shift registers [illegible]. The conversion time is about 1 ms.

Display Unit

The display unit is used to visualize the spectra accumulated in any zone in the CRT and to read in digital form the content of any address, selectable from the front panel. It is possible to have done the visualization while accumulating. To do this when the scanning reaches, the zone to be displayed, a signal is generated to initialize the wired program for displaying the content of the current address stored in one of the addresses 32 through 47. The content of the current address is fed to display unit via B1 bus. The display unit has also a register to store the current address with respect to the beginning of the zone. About 30 µs are needed to display one point.

The digital display of the content of any address decimal selectable from the front panel, is performed in the following sequence : conversion of the number of the address in binary form, reading of the content from memory and its conversion in BCD, display of the address and its content on the CRT using seven segments figures.

In order to do this the CRT display unit is connected to B3 bus.

The interface units for delivering the data (printer and paper tape puncher) are also connected to B3 bus.

Control Unit

The control unit is composed of input scanning unit, updating unit, stop control unit and microprogramming unit that control information flow among registers, memory and input - output interfaces. The microprogramming unit is realized in a modular structure (fig.4). There have been elaborated 11 modules addressed as subroutines during system operation. The modules are designed for : accumulation, increment of the current address, visualization of a certain point, manual access in a memory address, updating for the 15-th to 47-th addresses of the memory unit, power failure memory protection, searching of the address to be displayed in digital form, automatic increment of the address register when delivering blocks of digital data, algebraic sum of the contents of two zones.

The microprogramming unit is implemented using diode read-only memories, parallelly addressed by a 5 cell binary counter ; to set a certain program, one has to activate by a START pulse a flip-flop of the module. Each module has individual address wires, which examine a given set of logical variables. It has also a set of flip-flops designed to store the result of certain tests.

The outputs of all modules are parallelly connected on a bus. The adopted bus structure offers a flexible architecture of the system, in view of future system development by simply adding new modules. According to a specific mode of operation the START and END wires are connected through gates to assure the right succession of subroutines.

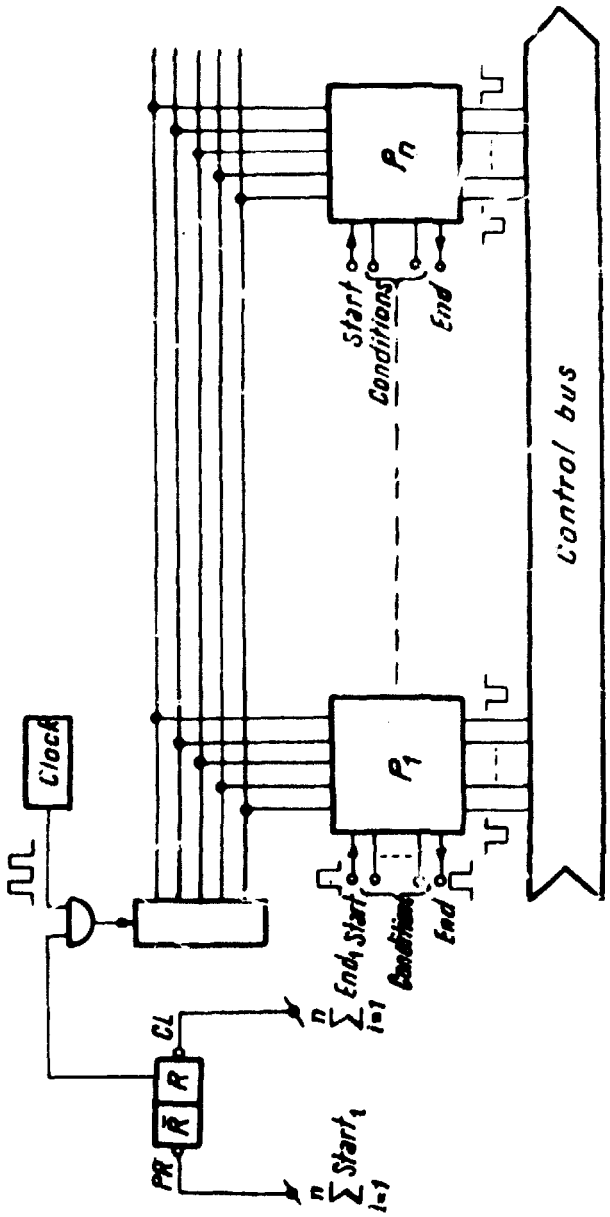


Fig 4.
Schematic structure of programming unit.

For checking the normal operation of the programs, it is possible to execute them step by step. In this case the address counter of the controller is incremented from the front panel and the [illegible] of the I bus is displayed.

IMPLEMENTATION

The system was entirely MSI and SSI integrated circuits performed (more than 25 types) using 7 double sided printed circuit boards (240 x 200 mm). The modular structure with information flow on buses led to wiring simplification.

The system can be further developed, using appropriate interfaces and programming modules to extend the range of possible experiments (time and amplitude analysis).

BIBLIOGRAPHY

/1/ EUR 4100e - CAMAC. A modular instrumentation system for data handling - May 1969

/2/ C.Gordon Bell, J.Grason, The register transfer module concept, Computer Design, May 1971, p.87

/3/ J.D.Nicoud, Convertisseur binaire - décimal en code décimal, Systèmes logiques, Nr.2, Avril 1970, p.92-97.