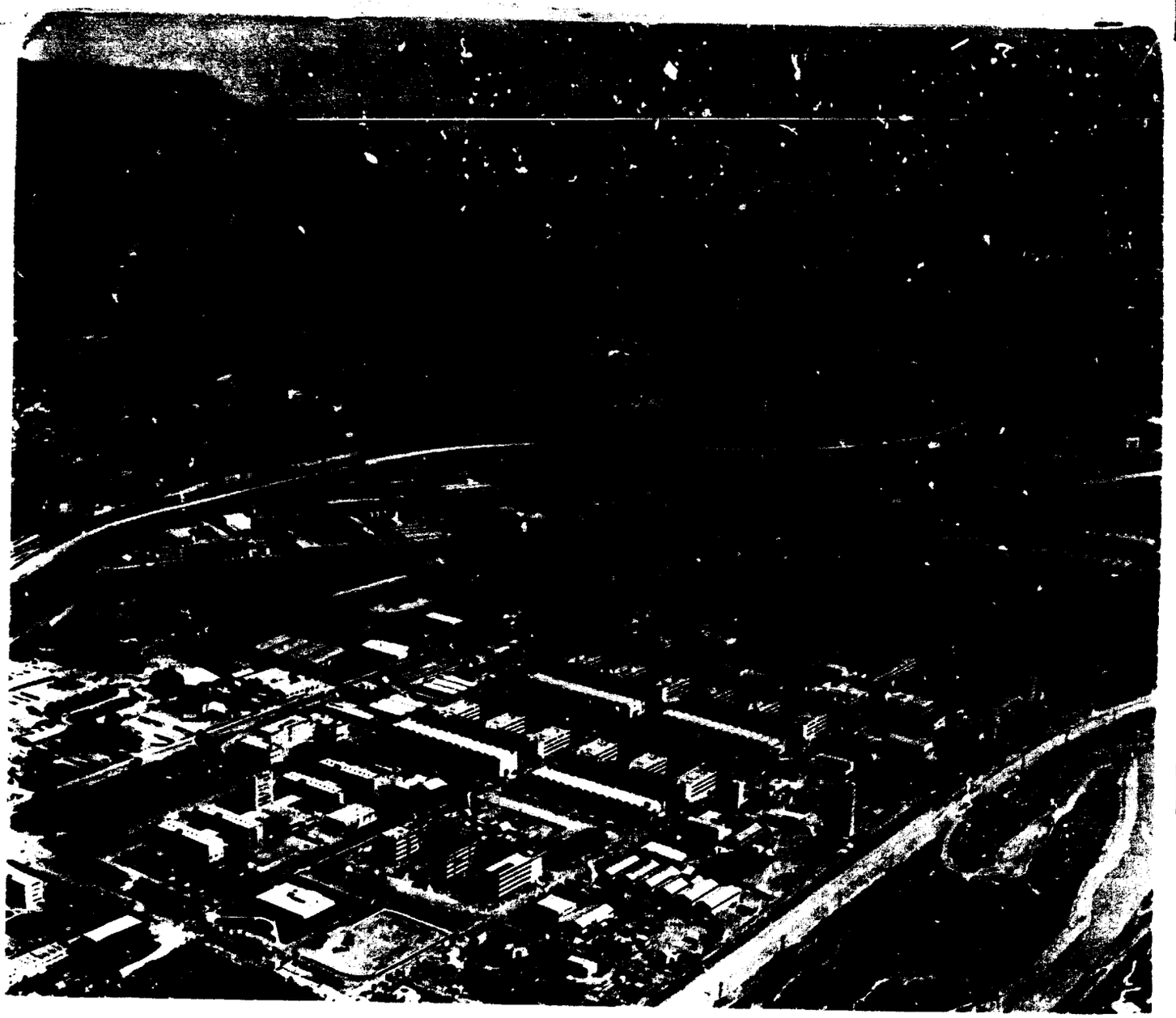

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# PHYSICAL MODELING OF SOS P CHANNEL MOSFET AND COMPARISON WITH BULK DEVICES.

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INTRODUCTION :

The advantages of MOS technologies on silicon on insultating substrate are well known.

For P channel MOSFET's, the kink due to carrier multiplication in the drain space charge region, is reasonably low for channel length larger than 5 µm and drain voltages smaller than 10 v.

In this paper, we first recall briefly the main technological steps applied to P channel MOSFET's on SOS. Then we present a large-signal model derived from a physical analysis.

A comparaison of typical parameters obtained on SOS and Bulk devices will be given.

. Figure 1 Shows the technological steps applied to SOS MOST's. The main differences with Bulk devices are the following :

- SOS MOST's are located on silicon islands which are etched from epitaxial silicon films on insulating substrates.
- the film thickness is relatively small (0,6 µm) and the charge below the gate is finite and small.
- the substrate potentiel is floating and influence in a pronounced way the current voltage characteristics.
- for P channel devices, the electron current produced by multiplication in the Drain space charge region is small and the Substrate Source-diode is forward biased by the Drain-Substrate reverse current.

. Figure 2 We see an cut view of the device before saturation. The substrate doping level is arround $10^{15}/cm^3$ and so, the substrate volume is depleted at strong inversion.

Field effect on mobility within the channel, is taken into account and two critical fields are defined :

$E_{CN}$ normal critical field

$E_{CL}$ lateral critical field

At the silicon-sapphire interface, the normal electric field is assumed to be zero.

. The results obtained before current saturation are given Fig. 2.

. A cut view of the device at channel pinch off, is given Fig. 3.

The pinch off point is defined by continuity of potential, lateral electric field and its derivative.

$E_P$ is the lateral electric field at pinch off

$V_{DSS}$ the drain saturation voltage

$I_{DSS}$ the saturation current

A is a parameter proportionnal to channel length and substrate doping level

$BI_D$ represents the effect of mobile carriers (holes) on the drain space charge width.

. Figure 4 We present the large-signal transistor model.

Gate-Source and Gate-Drain capacitors have been linearized versus drain voltage.

Due to low injection, we only take into account the diffusion capacitance of the Source-Substrate forward biased diode, and the depletion capacitance of the Drain-Substrate reverse biased diode.

. Some typical parameters measured on SOS and Bulk devices are given Fig. 5. The parameter spread is given for devices on the same wafer.

The thin oxide thickness was 1200 Å for SOS and 1000 Å for Bulk devices.

We can see that threshold voltage spread is quite the same in both cases, and less than 5 % on the same wafer.

Surface mobility is about 10 % less for SOS devices.

An important difference is observed in the value of the lateral critical field and its spread. For SOS devices, we observe that correlation between $\theta_D$ and channel length is, in most cases very bad. It seems that boundary conditions have to be better investigated at the Silicon-Sapphire interface, specially in current saturation regime.

. Figure 6 We compare experiments with theory on $I_D$ ($V_D$) and $I_D$ ($V_G$) characteristics.

. FIGURE 7 and FIGURE 8 show the DC transfer curves and the transient behavior of a NOR gate.

Reasonable agreement is obtained and we can conclude that the model is of interest to optimize the characteristics of SOS P channel MOSFET's.

Nevertheless, for a better physical understanding of the true behavior of the device (near the Silicon-Insulating interface), it seems necessary to make a two-dimensionnal computer analysis.

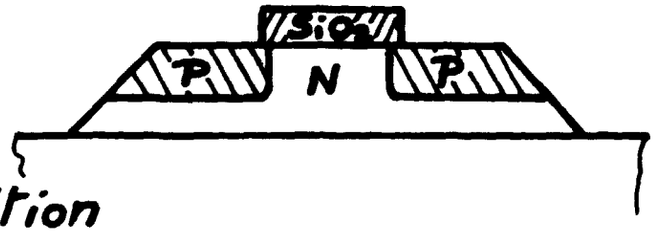
## LISTE DES FIGURES

Etch of Si


Deposition of $SiO_2$
(0,6 µm)


Etch of $SiO_2$

Boron predeposition




Thin Oxide

Contacts

Connections

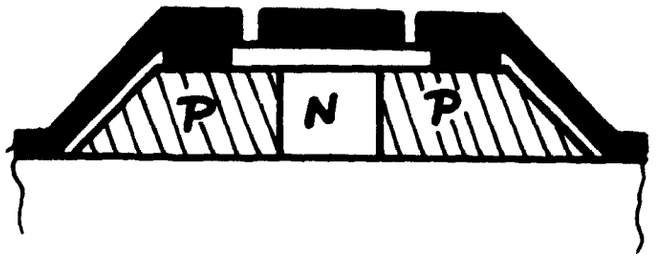
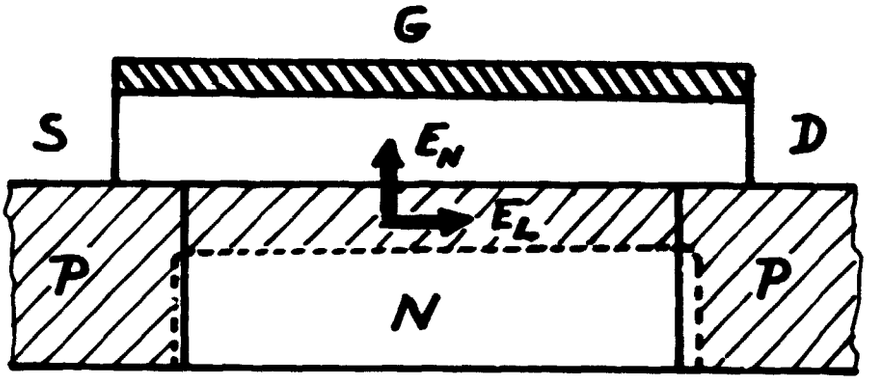



Fig. 1 Technology

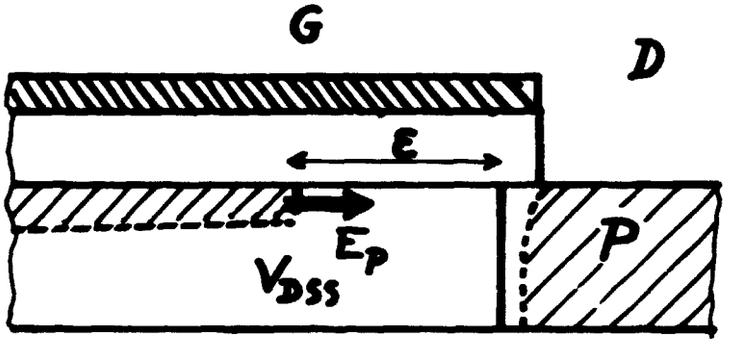



$$\mu = \frac{\mu_o}{\left(1+\frac{E_N}{E_{CN}}\right)\left(1+\frac{E_L}{E_{CL}}\right)}$$

$$V_G' = V_G - V_T \qquad \theta_G = \frac{C_{ox}}{\varepsilon_{si} E_{CN}} \qquad \theta_D = \frac{1}{L E_{CL}}$$

$$I_D = \mu_o C_{ox} \frac{Z}{L} \frac{1}{\theta_G(1+\theta_D V_D)} \left[ V_D + \frac{1}{\theta_G} \log\left(1 - \frac{\theta_G V_D}{1+\theta_G V_G'}\right)\right]$$

Fig. 2 Current - Before saturation



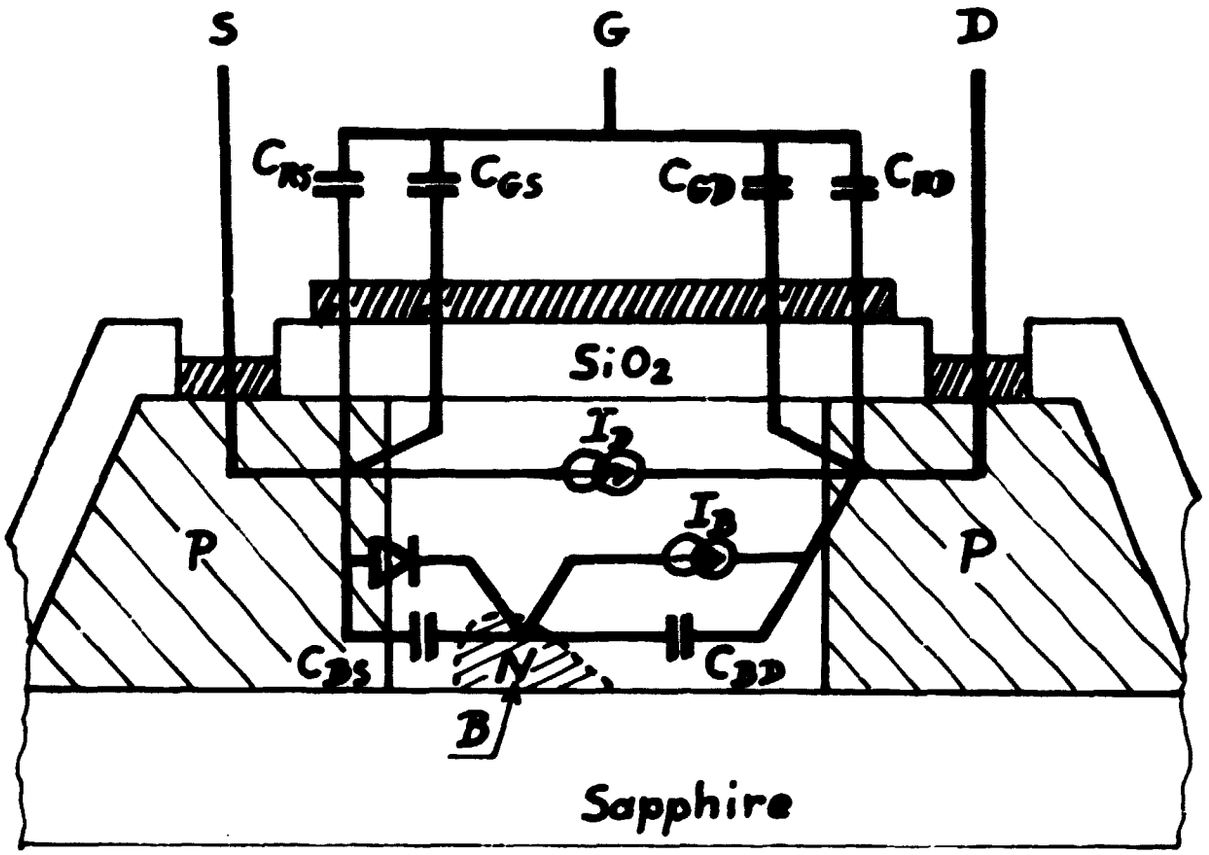

$$E_p = \frac{1}{L}\left[\frac{I_D A(1+BI_D)(1+\theta_G(V_G'-V_{DSS}))}{\mu_o C_{ox} Z/L}\right]^{2}^{1/3}$$

$$V_{DSS} = V_G' - \frac{1}{\frac{\mu_o C_{ox} Z E_p}{I_{DSS}(1+\theta_D L E_p)} - \theta_G}$$

$$I_D = I_{DSS}\left[1 - \frac{\varepsilon}{L(1+\theta_D V_{DSS})}\right]^{-1}$$

$$\frac{\varepsilon}{L} = \frac{\left[L^2E_p^2 + 2A(1+BI_D)(V_D - V_{DSS})\right]^{1/2} - LE_p}{A(1+BI_D)}$$

Fig. 3 Current - Saturation



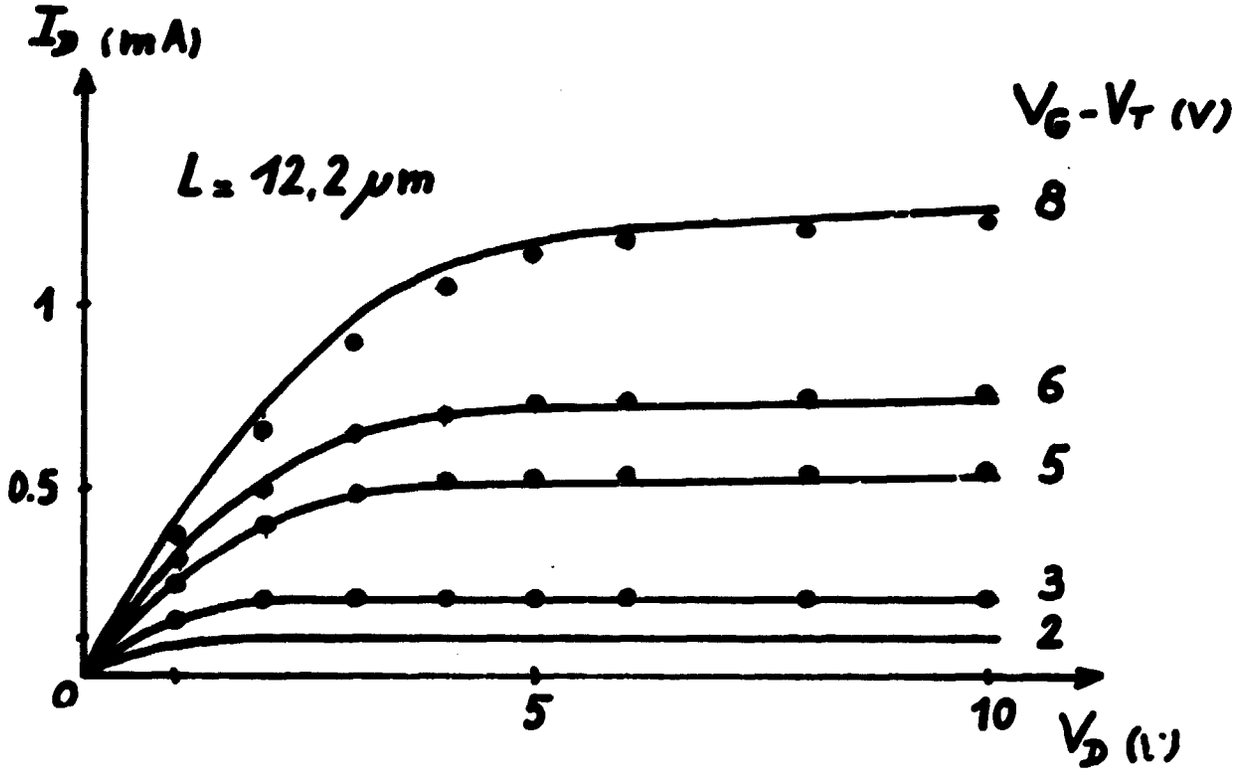

$$I_B = (M-1)I_D + I_R(V_{DB})$$

$$I_B = I_o\left(e^{\frac{V_{DB}}{nV_T}} - 1\right)$$

Fig. 4 Transistor Model

| | SOS <100> | Bulk <100> |
|---|---|---|
| $N_D$ (at/cm$^3$) | $2.10^{15}$ | $10^{15}$ |
| $C_{ox}$ (F/m$^2$) | $3.10^{-4}$ | $3,5.10^{-4}$ |
| $V_T$ (v) | $-2 \pm 5\%$ | $-1,9 \pm 5\%$ |
| $\mu_o$ (cm$^2$/v.s) | $220 \pm 10\%$ | $250 \pm 7\%$ |
| $\theta_G$ (v$^{-1}$) | $3.10^{-2} \pm 35\%$ | $3.10^{-2} \pm 35\%$ |
| ($E_{CN} \simeq 100$ v/µm) | | |
| $E_{CL}$ (v/µm) | $2 \pm 50\%$ | $10 \pm 30\%$ |

Fig. 5 Typical parameters




• theory
— experiment

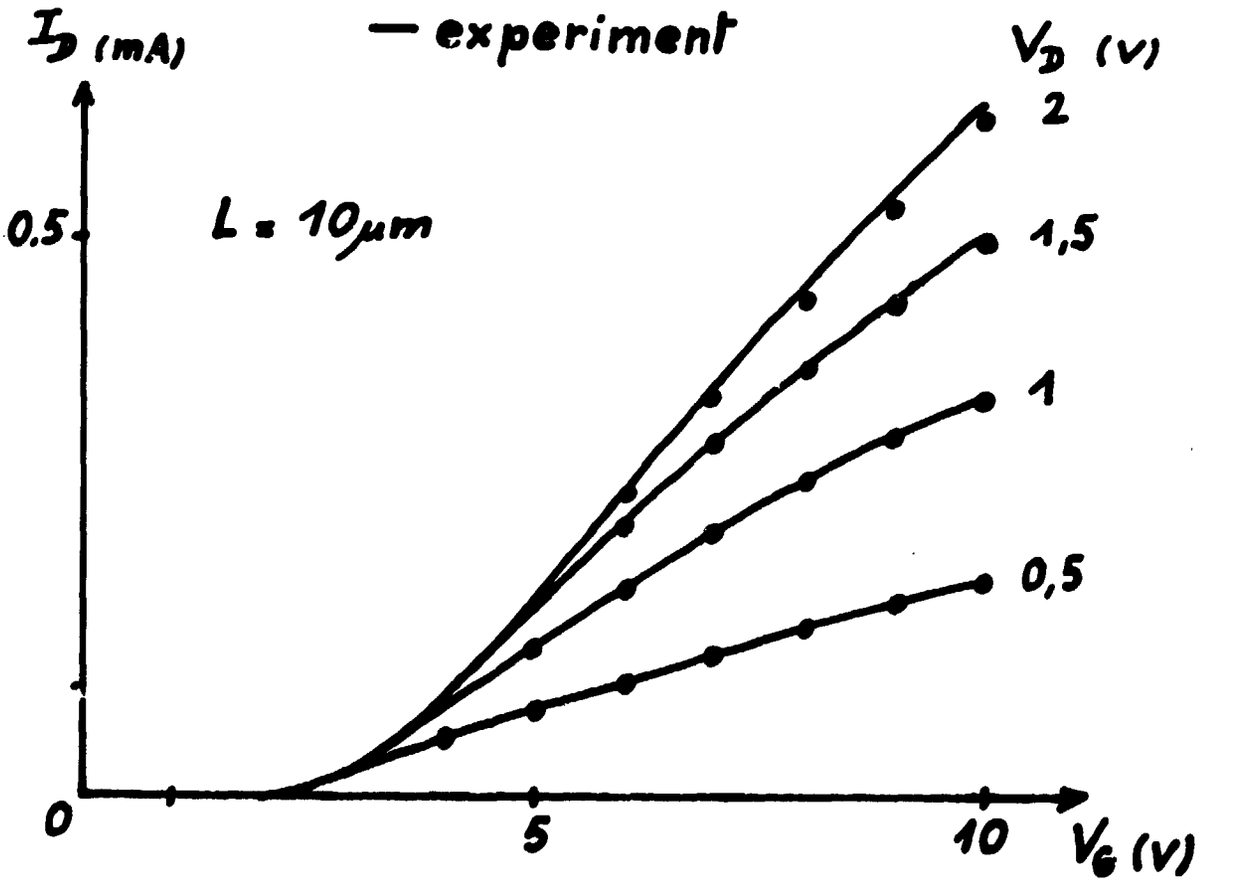



Fig. 6

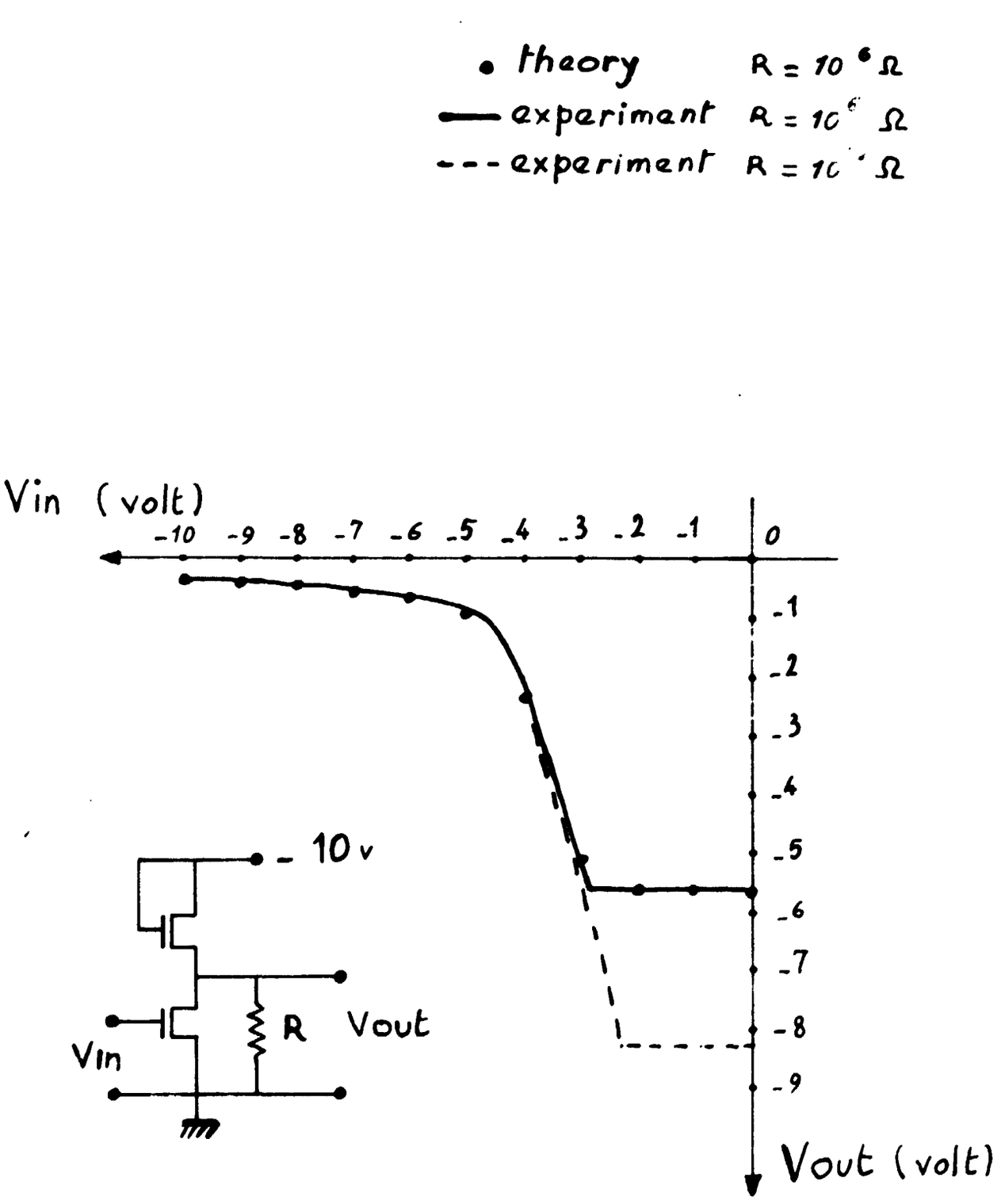



Fig. 7 Transfer Curve

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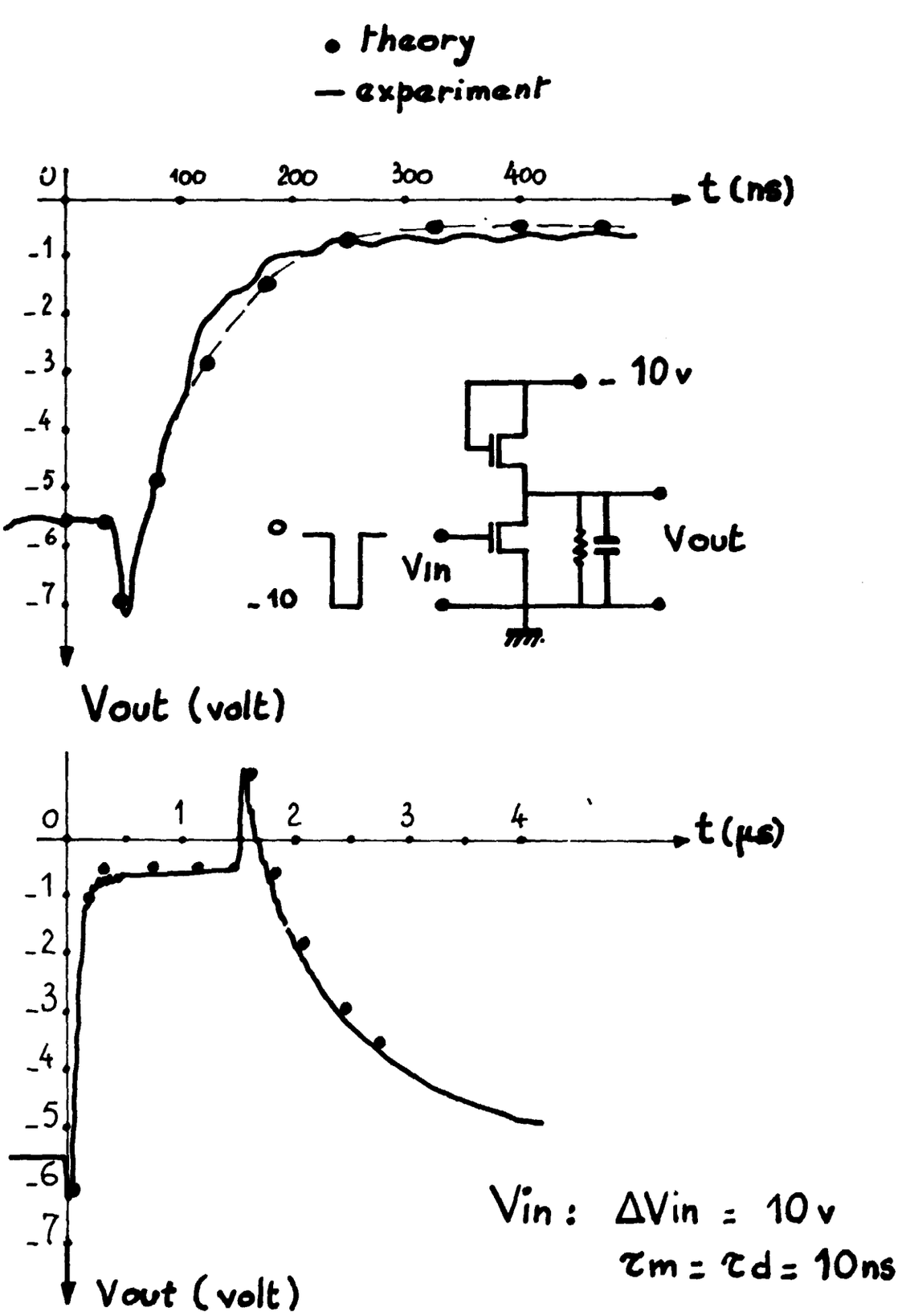


Fig. 8 Transient Curves