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CONTACTS TO SEMICONDUCTORS

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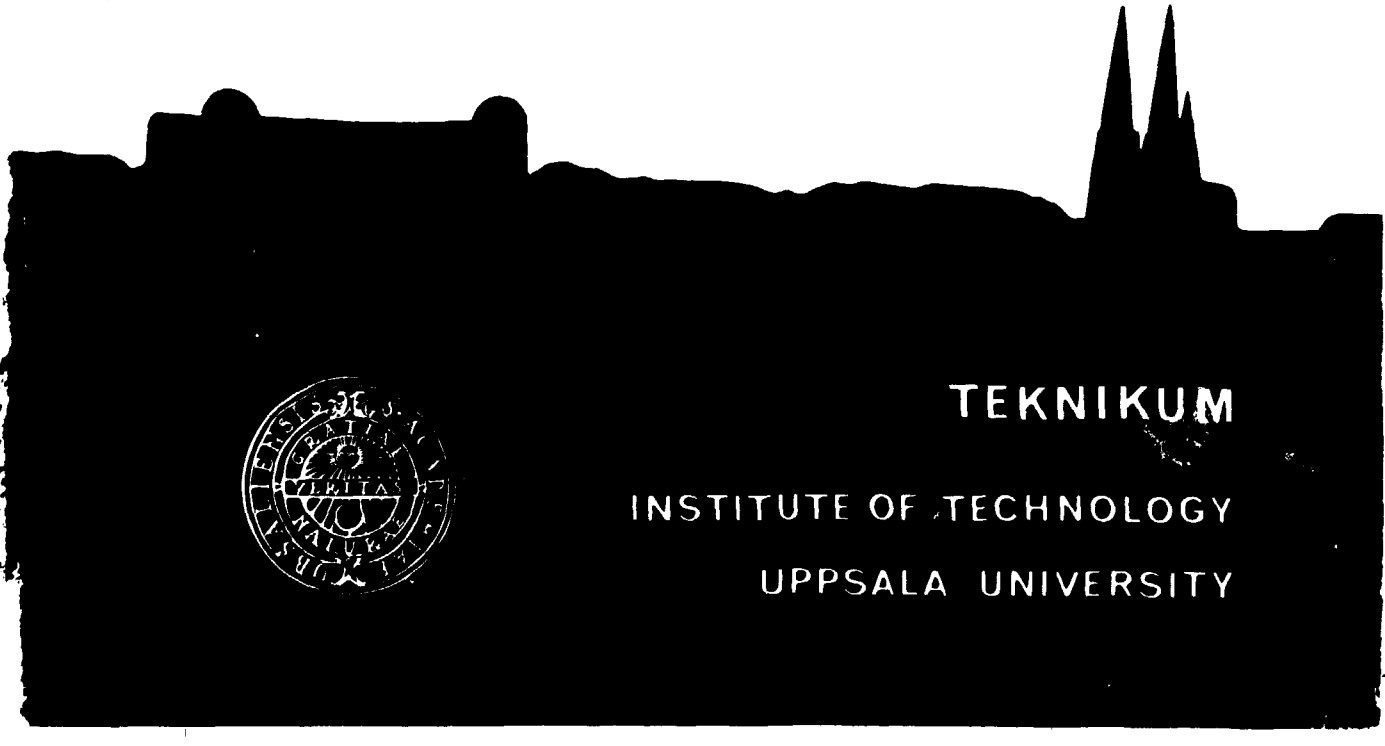

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Contacts to semiconductors x/

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1. Introduction

Contacts to semiconductors play an important role in most semiconductor devices. These devices range from microelectronics to power components, from high-sensitivity light or radiation detectors to light-emitting of microwave-generating components. Silicon is the dominating material but compound semiconductors are increasing in importance. The following survey is an attempt of classifying contact properties and the physical mechanisms involved, as well as fabricatio. methods and methods of investigation. The main interest will be in metal-semiconductor type contacts where a few basic concepts will be dealt with in some detail.

One way of classifying semiconductor contacts is according to the properties, e.g. as follows:

"ohmic"	"blocking"	rectifying	injecting	non-injecting	current-limiting	"free from edge effects"

We can also start from the physical build-up and the physical model used for explaining the function and then get

"tunneling" contacts	contacts with high generation and recombination velocity ("surface-destroyed" contacts)	metal-semiconductor transitions (MS-junctions)	semiconductor junctions (pn junctions)	semiconductor hetero-junctions

In the three latter cases we have directly touched upon the fabrication methods which can also be used as a classification ground. A few methods are listed below.

x/ lecture given at a symposium at Skokloster in may 1975

Fabrication methods

Metal deposition	Formation of a pn junction (eventually followed by metal deposition)
vacuum deposition through resistive heating	alloying (combination of pn junction and metal layer)
vacuum deposition through electron beam heating	thermal diffusion
sputtering in a high frequency system	ion implantation
sputtering in a d.c. system	epitaxial deposition
plasma gun	epitaxial regrowth
"electroless plating"	deposition of an amorphous or a poly-crystalline semiconductor layer (through vacuum deposition, chemical disintegration or formation of a radiation-damaged layer)
electrolytic deposition	
deposition through chemical disintegration	
fabrication of a silicide contact, through heating of a suitable metal-silicon contact	
thermo compression-"bonding"	
ultrasonic-"bonding"	

In some cases multilayer processes are used, e.g. when it is desirable to have a layer which has good adhesion to the silicon oxide in a planar process, and also a diffusion-inhibiting layer, and then also a third layer which permits good and reliable external connections (e.g. good soldering properties).

Before the contacting process the semiconductor crystal can be exposed to many different treatments which often can change the property of the contact radically.

Preparation of the semiconductor surface

Mechanical polish	Electron or ion bombardment
Electro polish	Heat treatment
Chemical etching	Cleavage of crystal in vacuum (to get clean surface)
Sputter etching	Ground or polished

With regard to methods of investigation the properties and the mechanism of the contact we can list the following methods:

Electrical methods, such as recording I-V curves at different temperatures, I-V curves under light radiation with different wavelengths for analysis of the topography of the depletion layer, capacitance measurement (I-V curves), etc.

Photoelectric determination of the barrier height according to Fowler's method (measurement of the photocurrent as a function of wavelength), for metal semiconductor contacts.

Rutherford backscattering of ions, for analysis of the atomic composition and possibly also crystal structure, at different depths from the surface.

Aging properties (electrical properties),e.g. transition from non-injecting to injecting behaviour, because of changes in the interface, changes induced by strong current overloading etc.

Finally, a list of application and uses for contacts to semiconductors is bound to cover nearly all types of devices. We can mention the following:

Integrated circuits (silicon)
Discrete components (silicon), e.g. transistors, power components, varactors, microwave generators, photo detectors and detectors for radioactive radiation.

Discrete components of other semiconductor materials (often compound semiconductors like III-V and II-VI compounds),e.g. photoconductors such as CdS etc.

Light emitting diodes and laser diodes, such as made from the materials GaAs, GaP etc.

Microwave generators using negative resistance effects in materials like GaAs.
Peltier elements, e.g. with the material Bi_2Te_3.
Hall elements and magnetoresistive elements, e.g. made from InSb and InAs.
Electro luminiscent layers, e.g. ZnS.

In the majority of cases we are using contacts to monocrystals but in some cases contacts to polycrystalline or amorphous semiconductors are also needed. If we consider "ohmic" and "blocking" contacts as two main categories we find that the former are most often in need. The two functions are often combined so that one has a low resistance ohmic contact for one polarity and blocking for the other polarity. The contact function is then integrated with the component function itself. Metal semiconductor contacts have certain advantages over contact types where a pn junction is used if we are interested in low resistance in the forward biased case. This is because they can be designed so that a larger current can pass at a certain voltage drop than for a forward-biased pn junction. To utilize this fully it is however needed that the resistance of the crystal itself is so low that the voltage drop across it does not play any role. In cases where the resistance of the crystal is appreciable a pn junction has advantages because we can easily obtain injection of minority carriers, which can neutralize the majority carriers so that a neglible voltage drop is obtained across the crystal. The metal semiconductor contact generally gives very low minority carrier injection and works only with majority carriers. - For small contact areas the resistance of the crystal often has influence and appears as a spreading resistance.

Injection of minority carriers can thus often be used to advantage. The classical cases are the emitter-base junctions of the bipolar transistor and of the surface barrier (germanium)transistor, in which cases a high minority carrier injection ratio is essential. Another case where injection is essential is when studying the crystal properties of new semiconductors with the help of space charge limited current phenomena. The possibility of making an injecting contact is here instrumental for the success of the experiment.

In other cases injection must be avoided, e.g. from the back contact in a radiation detector where one has created a depletion layer throughout the crystal volume, by applying sufficiently high reverse voltage on a (blocking) front contact.

We have anticipated our discussion of different contact types and will now start to look into the definition of properties a little further.

2. Ohmic contacts

As a definition of an ohmic contact one often uses the property that it shall display the same (low) resistance independent of the applied voltage polarity. It is generally assumed that this resistance is so low

that it is very small compared to the resistance of the crystal itself. Ohmic contacts are also often quoted as "not changing the concentration of carriers in the semiconductor, from the thermal equilibrium value".

2a. Ohmic contact of the type "ideal metal-semiconductor" junction.

A suitable starting point for the discussion is that type of ohmic contact which can be made with an ideal metal-semiconductor transition. In figure 1 is shown the band diagrams for the contacts on both n- and p-type material. The current-voltage characteristics

$$J = A^{xx}T^2 e^{-q\phi_B/kT}(e^{qV/kT}-1)$$

is determined by the barrier height ϕ_B (= ϕ_{Bn} for n and ϕ_{Bp} for p-type, respectively) between the metal and the semiconductor while the thickness of the depletion layer

$$x = (2\varepsilon\varepsilon_0(V_D-V)/qN)^{1/2}$$

is determined by the magnitude of the band bending V_D (= "diffusion potential") in the semiconductor and by the external applied voltage V (V is positive for forward bias). The slope of the I-V-characteristics in figure 2 around origo (the ring A) can be approximated by a straight line and corresponds to a resistance that is lower, the lower ϕ_B is. If this resistance is lower than that of the crystal the contact does not change the apparent resistance of the crystal seen from outside and we then have a "good ohmic contact". The higher the crystal resistivity is, the lower the barrier height must be so that this condition shall be fulfilled.

If the current through the contact reaches values corresponding to the ring B in figure 2 we can no longer speak of an ohmic contact because different voltage drops are obtained, depending on the polarity. However, to a certain current limit this voltage drop can still be small compared with the resistance of the crystal itself. When this limit is exceeded we have a rectifying contact which is blocking or reverse biased in the fourth quadrant and conducting or forward biased in the first quadrant of the I-V-characteristics.

3. Injecting contact

The above mentioned contact works with majority carriers e.g. electrons in fig. 1a and holes in fig. 1b as long as the barrier height does not approach the bandgap too closely. If this happens we can get injection of minority carriers, see the top of fig. 3 where minority carrier

injection is indicated (a contact on n material is shown which means injection of holes). Holes can be generated in the semiconductor near the interface (near the top of the valence band) and also in the metal (mainly close to the Fermi level). Their transport to the interior of the crystal is prohibited by the high barrier (which is lower for holes generated in the semiconductor). For forward bias this barrier is decreased and a hole current is obtained x/.
For moderate forward bias this current is predominantly a diffusion current. A rough measure of its contribution to the total current (which is mainly majority (electron) current) can be obtained by the following analysis.

In fig. 4a the concentration of electrons at A is

$$n = N_c e^{(E_F - E_C)/kT}$$

where N_c is the effective density of states in the conduction band.

The hole concentration at B is

$$p = N_v e^{(q\phi_B - E_g)/kT}$$

where N_v is the effective density of states for the valence band.

At the interface the potential for electrons is higher, with the amount V_D-V (for the forward bias V) than in A. According to Bolzmann statistics the electron concentration there will then be a factor $\exp(-q(V_D-V)/kT$ lower. The same applies to the hole concentration in the interior of the crystal compared with the hole concentration at B. We can then consider the expressions

$$j_n = qD_n n_p/L_n \text{ and } j_p = qD_p p_n/L_p$$

for the diffusion currents of electrons and holes. The diffusion constants D_n and D_p for holes and electrons are of the same order of magnitude. The "exhaustion depth" for the holes (to the right of A) is equal to the diffusion length L_p (for a long diode) but the corresponding exhaustion depth for electrons (at B) is usually much smaller than L_n. L_n applies only in the limit when the band bending is extremely small in the semiconductor (e.g. very high resistivity material) and when the metal can be considered as a perfect sink for the electrons. When a band bending exists we realize that the electrons (which move against a barrier) can only originate from that region of the semiconductor at the interface over which there is a potential drop equal to the diffusion potential kT/q. For normal, low resistivities the depth Λ of this region in fact easily becomes lower than the mean free path λ of the electrons. In such cases it is obvious that we have to replace Λ with the larger

x/ We can also get a hole current for reverse bias and this consists of holes generated within a diffusion length from A. Most often this current can be totally neglected.

quantity λ. The condition $\lambda > \Delta$ is actually the Bethe criterium for the validity of the emission current model which usually applies to metal semiconductor junctions (even for resistivities somewhat above that required by the criterium [1]. The minority carrier injection ratio can thus be estimated as [2]

$$j_p/j_n \simeq \frac{\lambda}{L_p} e^{-\left[(E_g - q\phi_B) - (E_c - E_f)\right]/kT}$$

We have then also taken into account that N_c and N_v are comparable in magnitude and we have assumed that the thickness of the semiconductor from the end of the depletion region to the contact at the right side (not shown) is much longer than the diffusion length L_p (long diode). λ is of the order of 100 Å while L_p can be a few tenths of a mm. Thus we generally have $j_p/j_n \ll 1$. That means that minority carrier injection is very small in metal semiconductor contacts. However, a more detailed analysis [3] shows that j_p/j_n can increase for a larger forward bias, as the hole current then gets an increasing drift current component (we considered only diffusion current above). However, this effect is not too large. E.g. for a Au diode (with $\phi_{Bn} \simeq 0.8$ eV) on 5 ohmcm n-silicon which has an injection ratio of approximately 10^{-4} at low currents we obtain an injection ratio of approximately 5% at a current density of 350 A/cm^2 [3].

Another method of increasing minority carrier injection for forward biased diodes is to introduce an oxide layer of approximately 30 Å thickness, between the silicon crystal and the metal [1]. The layer takes up some potential drop. As seen in figure 5 the effect of this is that for increasing forward bias the potential barrier for holes (ϕ_{ho} without bias, ϕ_h with bias) decreases more than the potential barrier for electrons (V_{do} and V_D) and thus the hole current is enhanced relative to the electron current, giving an increased minority carrier injection ratio. Injection ratios of $\simeq 0.2$ have been obtained in this way.

For a pn junction the ratio between hole and electron currents is given by

$$j_p/j_n = \frac{qD_p p_n/L_p}{qD_n n_p/L_n}$$

(The case of a long diode with a length $> L_p$ and L_n is assumed; for a short diode with $L \ll L_p$, L_n which has an ohmic contact at the end of the L region, L_p and L_n are replaced by L).

Because the diffusion lengths L_p and L_n are of the same order of magnitude, and also the diffusion constants D_p and D_n, the ratio j_p/j_n

is determined by the doping ratio. E.g., if the p side is much stronger doped than the n side the current on the n side (at the border) will be nearly all hole current. This applies for both forward and reverse bias conditions.

4. n-n^+ and p-p^+ contacts

The lowest figure in fig. 3 corresponds to accumulation or formation of an n^+ layer at the surface. The existence of this layer of higher conductivity is of course no drawback, but rather an advantage when forming a low-resistive contact. The principle is often used and the n^+ (or p^+) layer is most often obtained by diffusion or alloying. One advantage of these types of contacts is that they can be made so that injection of minority carriers is avoided. E.g. for an n^+ contact this is explained by the n^+ material having so small concentration of holes (consider the relation $p \cdot n = n_i^2$) that it cannot supply holes towards the interior of the semiconductor. Avoiding injection is necessary in some cases e.g. in order not to obtain a steep current rise when the field in the depletion region reaches the contact and is of such a direction that minority carriers introduced there could be extracted by the field. (One case where this applies is the back contact of totally depleted radiation detectors).

The use of alloying to obtain n^+ or a p^+ contacts has the advantage that the remaining part of the metal that was used for the alloying process can serve as external connector.

The avoiding of minority carrier injection for an alloyed contact is shown with the help of the band diagram in fig. 6 [4]. In order to make an n^+ contact one has first deposited (by vapour deposition) a layer of gold which contains a small percentage of antimony which is n-doping. In the following heating process, to the eutectic temperature the metal layer is alloyed with the semiconductor. Alternatively, n^+n or p^+p contacts can be made by direct use of a solder which contains the desired doping atoms; this applies to the use of Al or In pellets for making p^+ contacts. Due to several reasons, such as the heat treatment, the introduction of mechanical stresses in the transition region between the metal and the semiconductor and the very high doping concentration a very large number of recombination centra are formed close to the metal border in fig. 6 so that the carrier lifetime there becomes very low. The concentration of centra in the bandgap is so large that in practice one can assume that the band structure of the semiconductor no longer exists. A little further inside the semiconductor the band structure (which infers that carrier transport is limited to the bands) resumes its importance but the lifetimes are still very low. In this region a

successive transition to the n^+ layer occurs. The concentration of holes in the n^+ layer and the diffusion length $L_p = (D_p \tau_p)^{1/2}$ there are now so small that the layer cannot supply or inject holes into the crystal even if the field there has proper direction to extract holes (to obtain extraction the polarity would have to be negative on the n crystal). If the supply was ample holes would be emptied from within a diffusion length of the layer. We assume that the n^+ layer is thicker than the extension of a possible depletion region which can exist there. - For the majority carrier current of electrons the junction presents negligible resistance in both directions. - The very low concentration of holes in the n^+ layer also decreases the hole concentration in the n layer nearby, below its normal equilibrium value. This effect is in particular noticeable in materials with small bandgaps in which case n_i becomes large, and thus the majority carrier concentration p in the expression $pn = n_i^2$ also is relatively large, even for reasonable values of the doping concentration n.

In fig. 7 is shown a case of the use of the n^+n contact principle in integrated circuit technology. The main reason for its use here is different from that discussed above. The used contact metal is aluminium. After vacuum deposition a heat treatment at approximately 600°C is made, which exceeds the eutectic temperature for the Al-Si system. Al is a p dopant and ohmic contact to p silicon (e.g. to the base or to the substrate) is obtained without problems. On the other hand, contact to the relatively low-doped n type collector is made through a n^+ layer. The n doping in this layer exceeds the maximum solubility concentration of the p dopant Al in the melt and thus there is no risk of obtaining a (rectifying) pn junction, instead of an ohmic contact.

5. Ohmic contact of the "surface-destroyed" type

If the n^+ layer in fig. 6 is left out, the contact will still give a low potential drop but injection of carriers can now easily occur. This type of contact can be obtained by common soldering technique but also if one, e.g., first grinds the crystal surface and then applies a metal layer by vacuum deposition. Another method consists of using sputter etching with relatively high power [5] (before the metal deposition). Then a very large number of defect centra are formed in the interface region which means that the incoming carriers recombine very rapidly there. The high concentration of centra also means that carriers can be generated and the contact becomes injecting. We may mention that if we etch chemically a semiconductor surface after

polishing (or grinding) we get a much more perfect semiconductor surface and the deposited metal contact can then instead become rectifying.

6. Tunneling contacts

On sufficiently low resistivity material the barrier in fig. 1 becomes so narrow (of the order of 100 Å) that carriers can pass through rather easily by quantum mechanical tunneling, and the junction resistance becomes low. This is an often used method of making low-resistance contacts [6]. Tunneling becomes important when the doping density increases above $\approx 10^{18}$ cm^{-3}. In fig. 8 is shown the contact resistance $(dV/dJ)_{V=0}$, when the current is governed by the thermal emission model (no tunneling). For two values of doping density below the tunneling region, the contact resistance is shown for some values of the barrier height which correspond to a few specific silicide contacts. In fig. 9 is shown how this resistance decreases for higher doping densities, for the specific case of a barrier height of ϕ_{Bn} = 0.71 eV on n type silicon at room temperature. Tunneling occurs in the region T-F in fig. 9 where the barrier has become narrow as a result of the lower resistivity. Carriers which have energies somewhat above the Fermi level (because of thermal excitation) hit the barrier at a position where it is even thinner than at the Fermi level (cf fig. 1) and can pass through. This form of tunneling is called "thermionic field emission". In the region T normal thermionic emission applies (Richardson's eq.). In fig. 9 are also shown some experimentally measured values of contact resistance for different metals. Although the barriers for the quoted metals are different, ϕ_B = 0.71 eV has been used as a sort of average value in the theoretical curve.

For small contact areas which are common in microelectronic circuits one also has to take into account the spreading resistance which for a disc contact with a diameter D is given by

$$R_s = \rho/2D \text{ ohm}$$

Here ρ is the bulk resistivity of the semiconductor crystal.

Tunneling works in both directions (although with a somewhat different probability) so that no protection against injection is obtained.

7. Comparison between metal-semiconductor and pn junctions

In cases where a contact with low resistance for one polarity and high resistance for the opposite polarity is desired, one can choose between the metal semiconductor contact (without tunneling) and a pn junction

(perhaps also heterojunctions). A comparison between the expressions for the current in the metal semiconductor diode

$$J = A^{xx}T^2 e^{-q\phi_B/kT}(e^{qV/kT} - 1)$$

and that for a pn junction

$$J = \left(\frac{qD_p p_n}{L_p}\right)(e^{qV/kT} - 1)$$

where

$$p_n = \frac{N_c N_v e^{-E_g/kT}}{N_D}$$

(L_p is here the diffusion length for a long diode which is replaced by the diode length L for a short diode. We assume an unsymmetric diode with the p-side more heavily doped than the n-side)

shows that the voltage drop can be considerably lower for a metal-semiconductor junction than for a pn-junction, for one and the same forward current. This is because of the exponential dependence of the current on ϕ_B in the former case, and on E_g (where $E_g > \phi_B$) in the latter case. This is in particular true if one chooses a relatively low barrier height ϕ_B. A low ϕ_B value means of course that the current in the other, blocking direction also increases but this increase can often be tolerated. - A comparison of the above current expressions also shows that the forward voltage drop is less temperature dependent for a MS junction than for a pn junction [8].

The low forward drop of a MS junction should be favourable when making power rectifiers [9]. However, this can only be utilized when one does not require high blocking voltages. The reason is that high blocking voltage requires a thick depletion region in order to avoid avalanche breakdown. The existence of this wide depletion region then gives a large voltage drop in the forward direction which can only be avoided if one uses an injecting type of contact, viz. a pn junction. One then approaches charge neutrality in the crystal when the minority carriers injected by the contact compensate the majority carriers, and a low voltage drop is obtained.

8. Current-limiting contacts

A metal-semiconductor junction can easily perform as a current-limiting contact where the current limitation is at the level determined by the Schottky saturation current in the back direction (see fig. 2). By choosing a suitable barrier height one can obtain a desired saturation current [10].

9. Edge effects at contacts

Edge effects can cause deviation from the expected ideal behaviour expressed by the different models used to explain the I-V behaviour of the junction, and can be of practical importance e.g. by giving an undesired current rise for high reverse voltages. Edge effects can also become important for forward voltages. For a simple metal contact on a semiconductor surface a field concentration is obtained at the edge of the metal desk, even if one has "flat band" conditions at the semiconductor surface. In this case the depletion region at the surface extends equally long out from the edge as inwards the crystal. If there is a tendency of accumulation at the surface this may cause the depletion width to become shorter at the surface than in the bulk and the breakdown voltage decreases. On the other hand, if the surface is inverted the depletion width can become larger along the surface (a surface "channel" is formed). In this case the breakdown voltage may become higher but the channel can give a relatively large contribution to the reverse leakage current, because surface generation in the channel can be quite high (a tendency to increased concentration of defect centra and surface states exist at a semiconductor surface). - There is a certain natural tendency to inversion at a semiconductor surface, but one can influence the conditions through external means. E.g., it has been found that a treatment of silicon in wet N_2 gas tends to give an n type surface and dry oxygen gas gives a p type surface (this is natural considering that oxygen is "electro negative" and thus corresponds to a negative surface charge). This influence of the ambient gas has been found both for p and n type material [11]. The effect on a diffused junction on p silicon is seen in fig. 10. Dry oxygen is expected to give a shift towards p-type, i.e. "accumulation" which gives low voltage breakdown but also a low current. Wet nitrogen gas is expected to give n-type surface which may cause formation of a "channel", i.e. a high current, but also a higher breakdown voltage. This tendency is shown in fig. 10(although the figure is for a pn junction the same effect can be expected for metal contacts).

To avoid effect of this type one uses surface passivation and different methods of controlling the field at the edge. For planar diodes with metal overlap, fig. 11a the surface under the overlap is kept in depletion when the diodes is reverse biased so that a low breakdown voltage is avoided, but a certain extra current contribution from the edge cannot be avoided [8]. A certain improvement can be obtained by putting the central part of the contact in a groove ("moat etching") [12]. In fig. 11b a diffused guard ring has been introduced to reduce the edge effects [13]. One now has a satellite pn junction formed by the guard ring. The current in this can be decreased if the metal does not form on ohmic contact to the p silicon but gives a barrier.

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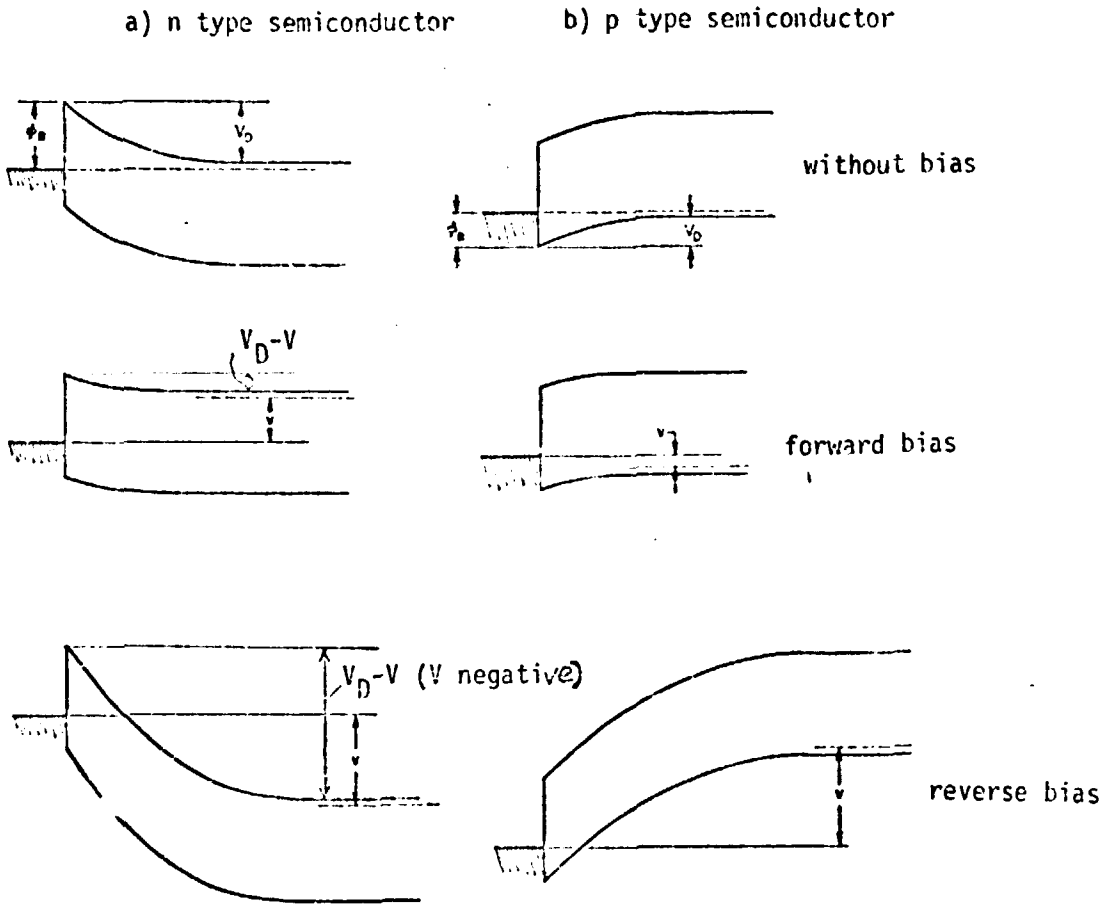


Fig. 1
(after ref. 14)

Band diagrams of metal semiconductor contacts

The barrier height ϕ_{Bn} for n material resp. ϕ_{Bp} for p material determines the voltage current characteristics according to $J = A^{xx}T^2\exp(-q\phi_B/kT)(\exp(qV/kT)-1)$ where the Richardson constant A^{xx} is about 120 A/cm^2 for electrons and about 30 A/cm^2 for holes (in silicon). The depth of the depletion region x (which determines the capacitance of the junction) is determined by V_D-V according to

$$x = \left[\frac{2\varepsilon\varepsilon_0(V_d-V)}{qN}\right]^{1/2}$$

V is positive for forward bias. N is the doping concentration.

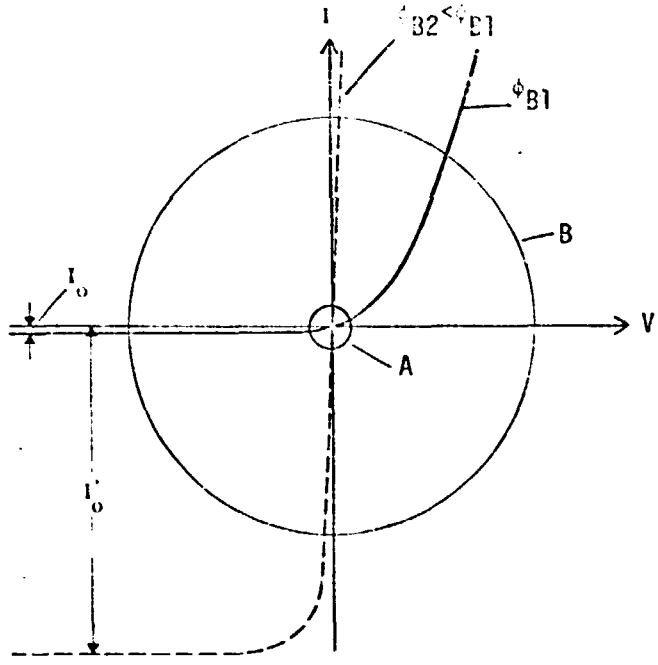


Fig. 2

Current-voltage characteristic

$$J = A^{xx}T^2 e^{-q\phi_B/kT}(e^{qV/kT}-1)$$

of a metal-semiconductor junction, for a high value of the barrier height ϕ_{B1}, and for a low value ϕ_{B2}. For contacts on n material V is positive for negative polarity on the crystal. For p material the opposite applies.

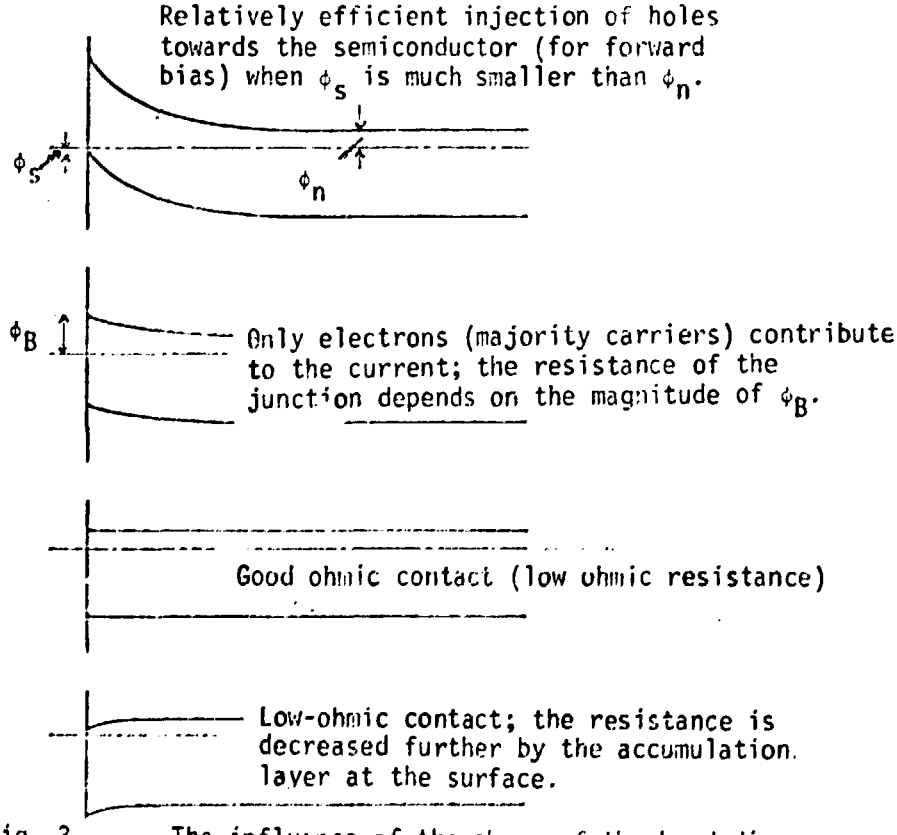


Fig. 3 The influence of the shape of the band diagram (after ref.2)on the properties of metal-semiconductor junctions.

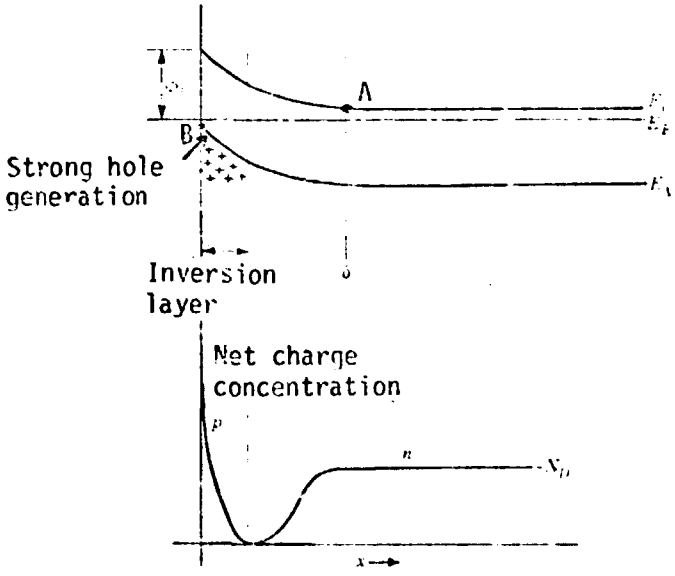


Fig.4 (after ref.2) Hole-injecting metal-semiconductor contact.

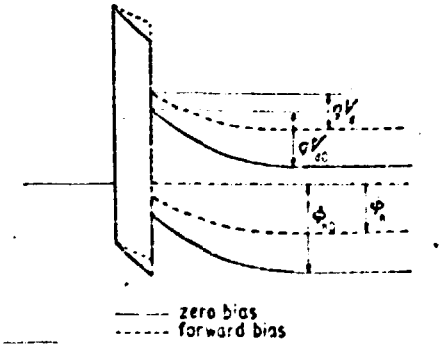


Fig. 5 (after ref.1) Band diagram for a MS diode with an oxide interface layer.

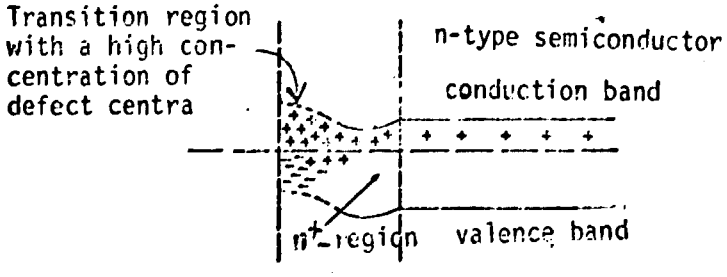


Fig. 6 (after ref.4) nn^+ contact for avoiding hole injection.

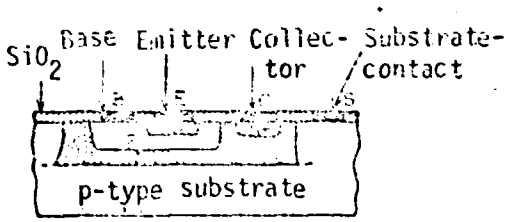


Fig. 7 Ohmic contact via an n^+ layer to the n type collector region in a bipolar transistor.

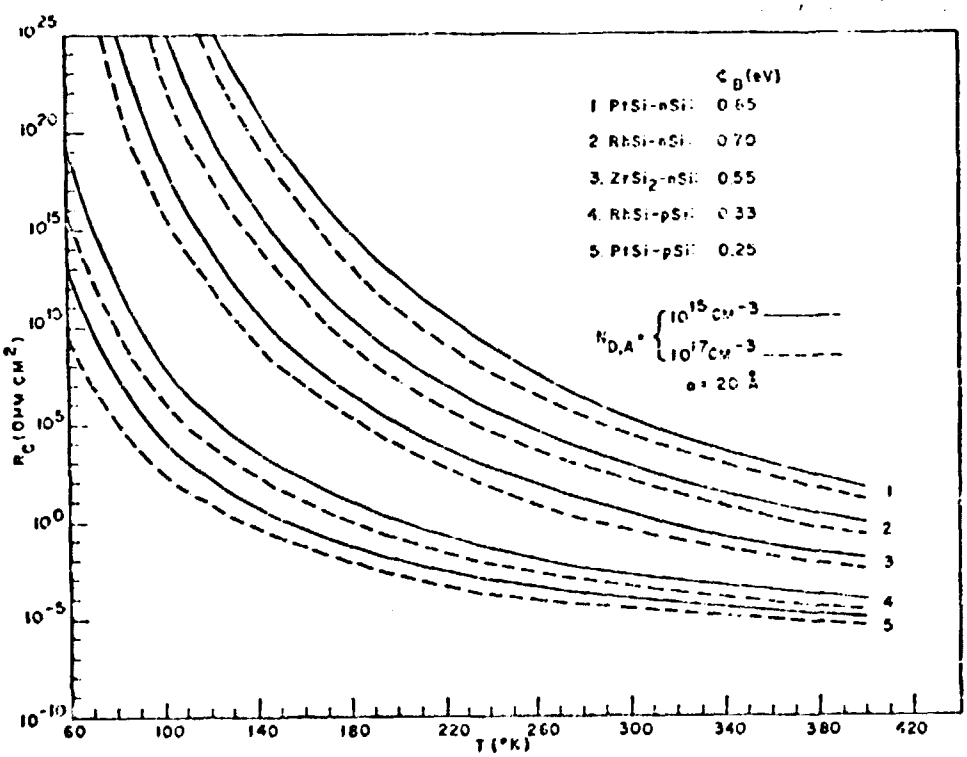


Fig. 8 (after ref.6) Specific contact resistance $(dV/dJ)_{V=0}$ for a Schottky diode where the current obeys the thermal emission current expression

$$J = A^{xx}T^2\exp(-q\phi_B/kT)(\exp(qV/kT)-1)$$

In the figure the barrier height for different silicide-silicon transitions is indicated. The resistance has a temperature dependence which can be of importance in some cases.

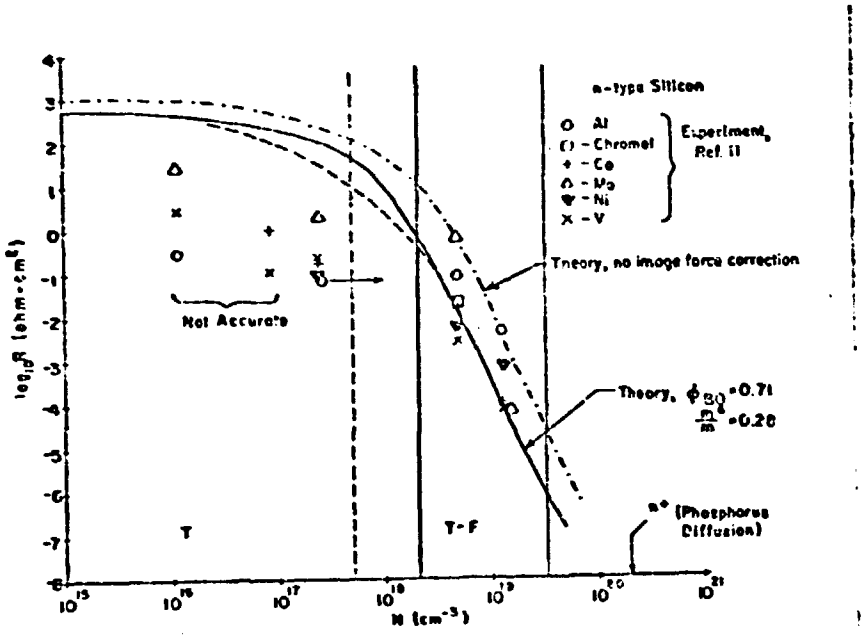


Fig. 9 (after ref.7) Contact resistance at room temperature versus doping density for a contact on n-type silicon with a barrier height of ϕ_{Bn} = 0.71 eV. Shown is the region of low doping (T) where the I-V characteristics obeys the thermionic emission law as in fig. 2,and the region T-F for higher doping where the resistance decreases because of thermionic field emission (tunneling) through the barrier. Also shown are experimental data for different metals.

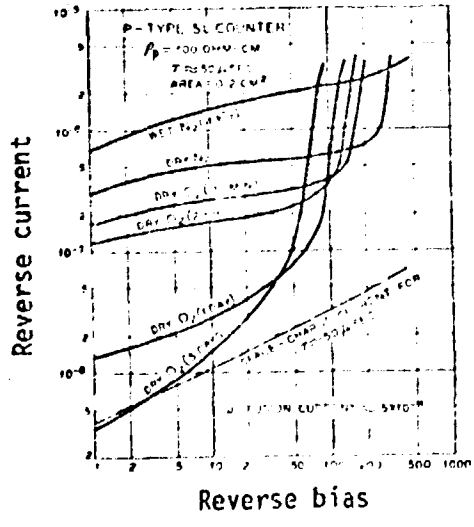
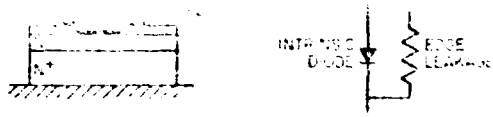


Fig. 10 (after ref.11) The influence of treatment with dry oxygen gas and wet nitrogen gas, respectively, on the reverse characteristics of a diffused diode on p silicon.

a)



b)

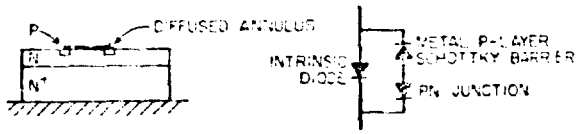


Fig. 11 (after ref. 8 and 13)

In a) is shown a planar diode with overlapping metal ring over the oxide. In b) is shown a diffused guard ring. To the right is shown the equivalent diagrams.