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PARALLEL PREPROCESSING IN A NUCLEAR DATA ACQUISITION SYSTEM

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Summary

The appearance of microprocessors and large memory chips has somewhat modified the spectrum of tools usable by the data acquisition system designer. This is particular true in the nuclear research field where the data flow has been continuously growing as a consequence of the increasing capabilities of new detectors. This paper deals with the insertion, between a data acquisition system and a computer, of a preprocessing structure based on microprocessors and large capacity high speed memories. The results shows a significant improvement on several aspects in the operation of the system with returns paying back the investments in 18 months.

Introduction

The HE 1 experimental set up described at the 1973 IEEE symposium is dedicated to electron scattering experiments with or without proton ejection. It's main characteristic is certainly the high data rate delivered by the detectors and their encoding logic. *Fig. 1* shows the earlier system *Table 1* summarizes it's capabilities as well as the on line processing capability of the computer.

It can be seen that for certain experiments, mainly (e,e'p) experiments ; there is a real limitation at the processing speed level. It has been the main goal of this project to try to overcome the speed limitation as well as to provide a limited capability real-time stand alone system to back up an aging computer, avoiding any straight data loss.

The processing of a nuclear event whichever the experiment can be seen as consisting of :

a) a mandatory real time part, acting on raw data the *"purpose"* of which is to increment a channel in a statistical distribution and to check for a certain number of validity conditions to be filled, for example proper operation of the detectors and associated electronics - allowing a feedback on the operation of the experimental set up.

b) a background task operating on sets of assembled data and delivering information more usable at the physics level. This information allows a better evaluation of the physics content of the actual results and consequently a *"physics feddback"*.

c) management programs interleaving the real-time processing task and the background task or sequencing the different processing steps or priorities inside each task. It must be pointed that all these operations implies context save and restore operations which are somewhat time costly on a PDP 15.

The earlier set up relied on a single computer and on a quite elaborate software, most of it in assembly langusge. This means an heavy dependance on computer reliability and, for any software change, on the people who wrote the programs.

It was consequently mandatory that the improvement in processing speed should not be done at any increase of the system's complexity but on the contrary should be headed towards hardware and software simplification.

Comparison of alternate possibilities

There was several alternate routes to reach these goals those which have been considered in details are :

a) use the biprocessor capability of the real time computer system eventually in a symmetrical configuration.

b) emulate the PDP 15 around fast arithmetic logic unit or microprocessor slices an then a).

c) built a dedicated fast processor.

d) use an appropriate microprocessor type in a parallel processor configuration and link it to the PDP 15. All these possibilities are sketched down on *Fig. 2*.

There sre obviously many other possibilities but they could not fit our requirements at least in terms of cost or hardware or software development.

From the description of the processing tasks it is obvious that the first move was to separate the real time foreground task from the background task. This leads to structure a), b), c), d) where the background task is left to the PDP 15/40 well equipped for this purpose with a floating arithmetic unit, several magnetic storage media, DEC Tape and interactive devices as the VT 15 display. All programs but a small nucleus are written in Fortran. In this case switching back and forth between real time and background tasks has been mostly eliminated but for transfer to the PDP 15/40 of sets of assembled data. It is an important simplification which helps to increase speed.

The next step forward is to split the real time processing task in three separate processors corresponding to the data streams from both spectrometers and the *"coincidence"* data stream. This allow simultaneous and independant processings and in turns speed increase, software simplifications and a drastic drop in context save and restore operations.

It is however to be pointed that in order to keep some feedback to the experimenter an interactive device must access to the data once processed and that the multiplicity of processors implies the multiplicity of communication links to the PDP 15.

So the choice between a), b), c), d) structures can be summarized in one question : how far to go in the independance of the differents tasks and at what cost?

In order to help decision making a number of criteria have been selected - results appears in *Table II*. Some comments are necessary to explain these results.

Speed improvement is slight in structure a but *"physics"* feed-back is much better. Speed improvement can be increased with structures b and c but at the expense of hardware complications and also software complication for c. Structure d has a better score on average, essentially in reason of its ability to increase the

speed without requiring any state of the art design. It was decided to choose the d structure to implement the preprocessing unit.

Organisation of the d) structure (*Fig. 3*)

The d) structure require three microprocessors for data processing only, a fourth one has been introduced to synchronize the tasks and sequences between the microprocessors, the PDP 15, the CAMAC... and to interact with the experimenters. This is done through a storage tube display and a teletype.

The need for a communication link between the microprocessors on one hand and the computer on the other hand has been filled by using a large multiport memory shared by all the processors. This memory is used for spectrum, counters, look-up tables, storage and mail boxes for communication. It is also used as a data path to transfer programs and look-up tables either from the "*synchronizer*" processors or the PDP 15.

The synchronizing processor can be interrupted by any of the other processors in a OR configuration. The mail boxes allowing to raise the ambiguities. In turn this processor can start or stop as well as interrupt any of the microprocessors and call the PDP 15.

Such an organisation allows a great flexibility without down grading the speed performance of each processor. A slow speed link allows data transfer to the PDP 15/10 in case of PDP 15/40 failure.

Components and modules description

Each microprocessor has been attributed 16K of memory and shares with others a common 48K memory. This memory has been sliced in three 16K banks with simultaneous acess in order to avoid accers conflicts and long waiting time for the processors. On each bank eight hierarchical ports are provided the higher priority corresponding to refresh cycles. Each microprocessor in charge of a data stream has a 2nd high priority on at least a bank where most of corresponding programs and look-up tables are implemented, this also decrease the number of conflictual situations.

Sixteen bits microprocessors have been choosen. They fit quite well the data format of the previous system. The GI CP 1600 A chips has been selected. Programs development being made on a GIMINI system.

RAM has been prefered to ROM. It has the advantage of being less costly in this applications and lend itself easily to software changes. However a small bootstrap with CMOS RAM with battery back up is implemented in each of the data stream microprocessor.

All RAM in main storage are 16K word × 1 bit chips from Mostek or Fairchild. Cycle times are between 450 ns and 600 ns depending of the cycle. Boards have been tested through the CPU/memory test program from the GIMINI library.

The design burden has been drastically reduced by using a limited number of boards types these boards are :

Board type	Number
16K.words × 16 bit RAM	4
CPU	4
Operators	4
Multiplexer	1
Interfacing unit (TTY, Display, HSR, CAMAC)	1
Data acquisition interface adapter	1

The CPU board is derived from the GIMINI'S board slight changes however have been introduced. The operator board is essentially a microprogrammed unit occupying some memory locations. It's main purpose is to allow direct increment and decrement in memory. Future extensions are planned as multiply and divide. Provision has been made for such extensions.

The multip exer boards allows the priority to be set among different requests and data to be routed to or from any of seven ports to three memory banks.

Interfacing unit to TTY and HSP is standard from GI, CAMAC will be connected through a JCAM-10 unit - 8080 processor. Display interface is quite straight forward.

Data acquisitions interface adapter simulates the previous connections to the PDP 15 on one side and on the other side delivers the proper signals on one port of the memory. Acquisition control and interface status are connected to the synchronizing microprocessor.

Program loading

Program loading can be done through two ways :

- through a high speed tape reader and the synchronizing microprocessor
- through the PDP 15 and a dump mode from the PDP 15 into the common memory.

Once in the common memory boot-straps in each microprocessor transfer it in local memory. The first mode only is used by now although the PDP 15 is used to update certain parameters.

Conclusion

The primary goals : processing speed improvement and stand alone system have been reached but additional benefits are to be pointed.

The stand alone capability allow :

- off beam : to control the status of the detectors set up, using radioactives sources for example and to point any failure.
- under beam : to set the correct bias point of the detectors but with the PDP 15.
- off line : this can now be done simultaneously for the three data streams when previously it has to be done in sequence. Beam time can be saved at a rate of two to three hours for each start up procedure.

The gains derived from the speed improvement varies with the cross-sections to be measured ; however the increase in the affordable statistics of simple events, electrons or protons, allow a better survey of the detectors efficiency and therefore a better monitoring of the experiment.

Flexibility of use

It has been shown a situation where each "*data streams*" microprocessor has a different task. However, provided that the programs have been written, it is absolutely feasible to allocate differently the preprocessing power to the tasks and so to taylor this power to the peculiar needs.

Reliability

Hardware reliability is certainly greater thanks to the modular approach - but the system's reliability is

also drastically improved. This can be shown on the different possible failures.

PDP 15/40 failure : acquisition can be continued at same speed with the loss of the background processing, preprocessed data being transfered to another computer through a slow link.

One microprocessor failure : as pointed before it is possible to remodel the tasks distribution on the two processor left with a slight loss in speed.

Unique of a kind board failure : that is memory multiplexer, interface adopter, CAMAC adopter... it is possible to get back to the earlier situation, acquisition directly on the PDP 15/40 bypassing the preprocessing system.

Simplicity

As previously mentionned the separation of the different real time tasks from the background tasks brings back to programs simplicity. It is a particularly desirable feature that any one among the users feels able to penetrate and to modify the programs.

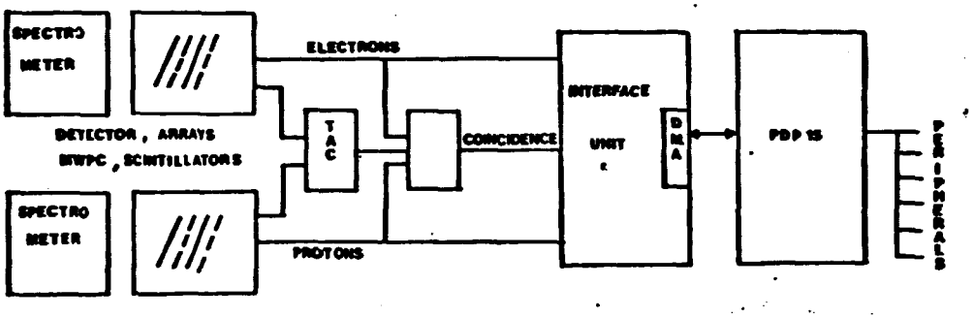

Figure 1

	DATA SIZE	MAX. EVENTS OCCURENCE	PROCESSING SYST. CAPABILITY
Electrons	8 x 16 bit words	4000/s	1000/s or
Protons	8 x 16 bit words	4000/s	1000/s or
Coincidences	16 x 16 bit words	200/s	100/s

Table I

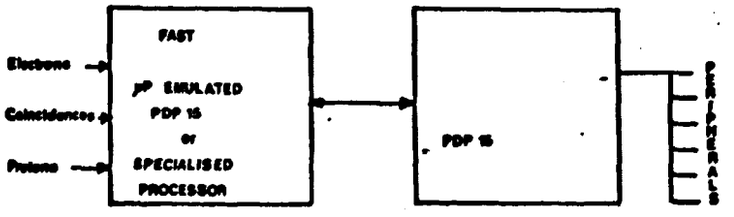

Figure 2A

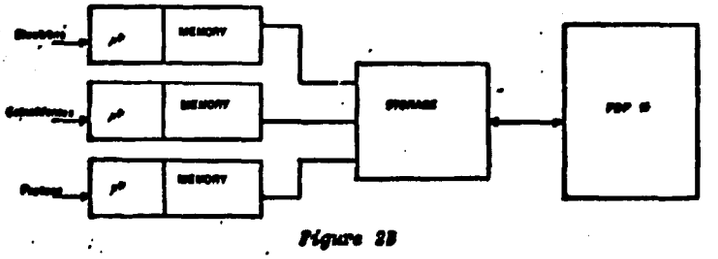

Figure 2B

	Speed increase	Stand alone	System simplification	Hardware development	Software development	System reliability improvement	Adaptability to processing changes
a	Slight	IP PDP 15/40 OK	Moderate Real time Background separation	Slight	Slight	Slight	Limited
b	3	IP PDP 15/10 OK	Moderate Real time Background separation	Important	Slight	none	Limited
c	>3	IP PDP 15/10 OK	Real time Background Separation Moderate	Important	Important	none	none
d	3	YES	Very good Task independency	Moderate	Slight to moderate	Very good	good

Table II

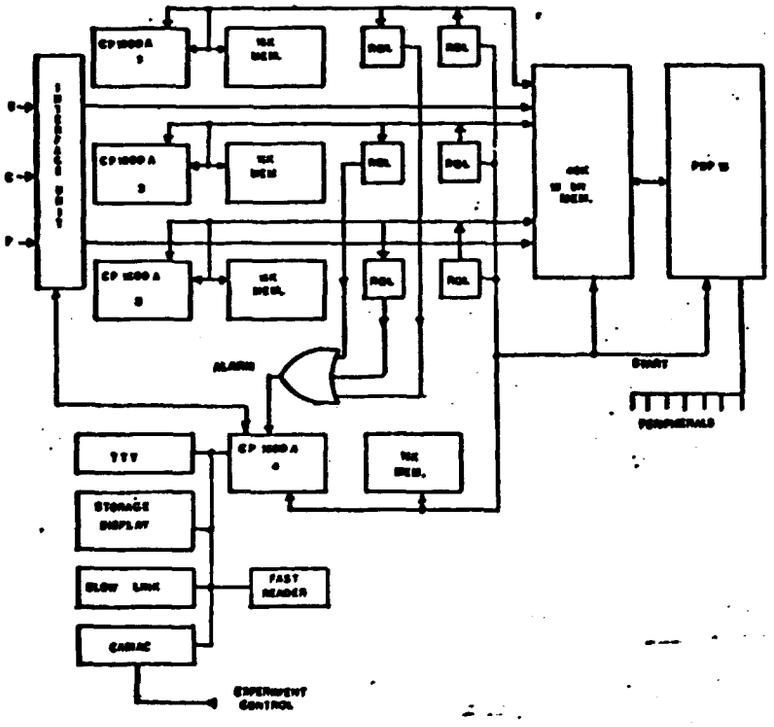

Figure 3