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Unlimited Release

Microprocessor-Controlled, Programmable Ramp Voltage Generator

J. Hopwood



Sandia Laboratories

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MICROPROCESSOR-CONTROLLED, PROGRAMMABLE
RAMP VOLTAGE GENERATOR

J. Hopwood
Model Shops and Inspection Division 3423
Sandia Laboratories, Livermore

ABSTRACT

A special-purpose voltage generator has been developed for driving the quadrupole mass filter of a residual gas analyzer. The generator is microprocessor-controlled with desired ramping parameters programmed by setting front-panel digital thumb switches. The start voltage, stop voltage, and time of each excursion are selectable. A maximum of five start-stop levels may be pre-selected for each program. The ramp voltage is 0 to 10 volts with sweep times from 0.1 to 999.99 seconds.

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MICROPROCESSOR-CONTROLLED, PROGRAMMABLE RAMP VOLTAGE GENERATOR

Introduction

The Extranuclear Laboratories Quadrupole Mass Spectrometer employs quadrupole rod assemblies with combined rf and dc electric fields to obtain ion separation for gas analyses. For a given field potential, only ions of a specific mass-to-charge ratio follow stable trajectories along the length of the rod array and ultimately reach a detector. In this way the quadrupole assembly serves as a mass filter. By ramping the voltage in a saw-toothed fashion from low to high potential, ions of increasing mass number are swept through the filter.

Since the actual voltages applied to the rods can be on the order of kilovolts, a programmable, high-voltage supply is utilized to avoid problems associated with large ramp voltages. To drive the high-voltage supply of the quadrupole residual gas analyzer at Sandia Laboratories, Livermore, a 0-10-V ramp voltage generator has been developed. It is the purpose of this report to describe the design of this microprocessor-controlled, programmable generator.

General Description

The generator produces two output voltages: Output 1, the quadrupole ramp voltage (or sweep voltage), and Output 2, called the scope ramp voltage (or scope sweep voltage), which is used to drive the horizontal axis of a recording device (oscilloscope or chart recorder). Both of these are controlled by a resident microprocessor program.

The desired ramping form of Output 1--initial and final voltages (10 V maximum) and ramping time--is selected by means of front-panel digital thumb switches. Output 2 always rises from 0 to 10 V, with a ramping time identical to that of Output 1. Activation of a store switch causes the program to read and store the digital weight of each switch, perform the necessary

calculations to determine the voltage amplitude-ramp time slope, and then store that information. A complex (but constant slope) ramp of up to five different steps is possible (see Figure 1).

Activation of a start switch causes the program to fetch and distribute stored data to appropriate registers, initiate ramp-voltage generation, and monitor the ramping process. Other front-panel controls permit repetitive or single ramping, baseline shifts, in-process angle modification, and an indefinite hold at any voltage in a pattern.

It is not necessary to use the generator for programmed ramping. When AUTO/MANUAL is set to MANUAL, and there is no program in the memory, Output 1 will be equal to the start voltage setting.

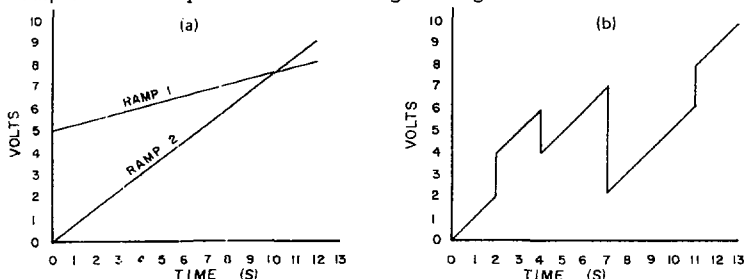


Figure 1. Ramp Program. (a) Two illustrative ramp outputs, showing that the starting voltage and ramp slope are arbitrary (within certain special limitations). (b) Example of a five-step pattern that can be programmed into the ramp voltage generator.

Front-Panel Operating Controls

Figure 2 shows a photograph of the front panel of the programmable ramp generator. The control functions, ranges, and limitations are as follows.

Reset

Places all logic in the zero state. Must be actuated prior to any programming if there is already a pattern in the RAM. Turning the generator power on is equivalent to the reset operation.

Start Voltage

The voltage level from which the ramp will start. Continuously variable from 0.00 to 10.0 V. A maximum of five voltage steps may be programmed.

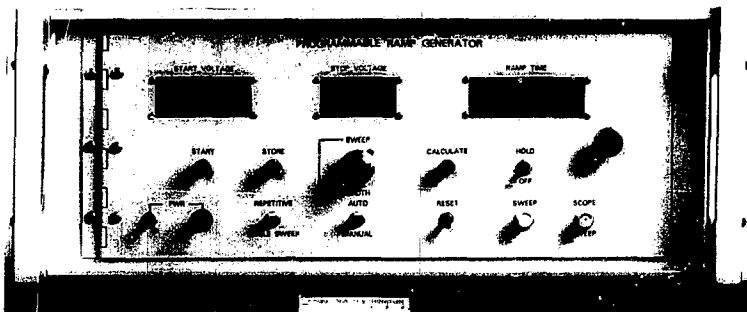


Figure 2. Front Panel of the Programmable Ramp Voltage Generator

Stop Voltage

The voltage level at which the ramp will end. Variable in 10 mV increments from 0.00 to 9.99 V (but see Ramp Time description for limitations).

Ramp Time

The total time the generator will take to reach the stop voltage level from the start voltage level. Continuously variable from 0.1 to 999.99 seconds, with the following limitations:

<u>Ramp Time</u>	<u>Max Stop Voltage</u>
0.1 sec	5.00 V
0.2 sec	6.00 V

Ramp times of 0.01 to 0.09 sec are not possible; the program will treat these times as 1.0 to 9.0 sec if there is an attempt to produce them.

If multiple steps are programmed, the ramp angle is calculated from the initial time. No additional time settings are necessary or possible.

Store

Causes the program to read all front-panel thumb switches, store voltage levels, and calculate the ramp angle. Five start-stop voltage levels can be programmed. The ramp angle is calculated from the initial setting and remains constant throughout program execution. RESET should be used prior to STORE to clear the logic.

Start

Initiates voltage ramp (sweep) generation. Will not function unless a ramp angle is programmed (see Store).

Sweep Width

Permits a $\pm 5\%$ change in the programmed ramp time. Continuously variable as the setting is changed from 0.00 to 9.99. When set at 5.00, the sweep time will be the programmed (or dialed) ramp time (see Auto/Manual below).

Calculate

A nonfunctional switch (its functions were taken over by STORE during program development).

Hold/Off

When switched to the HOLD position, the program is stopped and the voltage stays constant at the level it reached. The program will continue when the switch is returned to the OFF position.

Repetitive/Single Sweep

Repetitive Mode--The program is repeated continuously (see Figure 3a).

Single Sweep Mode--The program is executed once for each activation of the START switch. When AUTO is selected, the sweep voltage will remain constant once it reaches the stop voltage level. When MANUAL is chosen, the sweep voltage will return to the start voltage level as soon as it reaches the stop voltage (see Figure 3b).

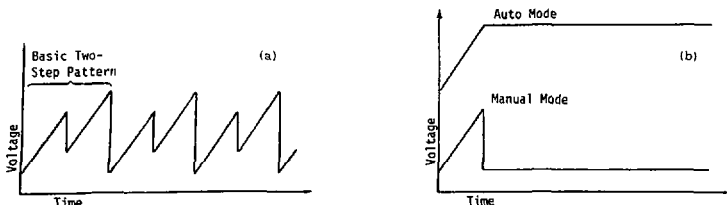


Figure 3. Ramp Generator Output for Repetitive/Single Sweep Modes. (a) Two-step pattern in the repetitive mode. (b) Single sweep mode. The top trace shows a single, one-step ramp in the auto mode. The bottom trace shows the same ramp, but in the manual mode.

Auto/Manual

Auto Mode--The sweep voltage follows the program without modification, repeating the programmed pattern when Repetitive is chosen and remaining constant if Single Sweep is selected.

Manual Mode--If no pattern has been programmed, the sweep output will follow the indicated start voltage. If a pattern has been programmed, the sweep voltage follows the programmed pattern, repeating the programmed pattern if Repetitive is chosen and returning to the start voltage level as soon as it reaches the stop voltage when Single Sweep is selected. If the start voltage is changed (but the change is not stored), the baseline will shift accordingly. For example, if the original start and stop voltages were 1 and 6 V, respectively, and the start voltage is changed to 3 V, then the generator will ramp from 3 to 8 V. Thus, the sum of the start and stop voltages can never exceed 10 V (see Figure 4). Changes (other than programmed changes) in stop voltage or ramp time do not affect the ramp pattern.

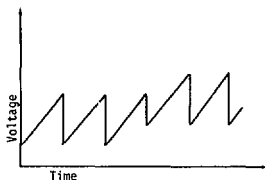


Figure 4. Ramp Generator Output for One-Step Pattern. In the Repetitive Mode with AUTO/MANUAL set to MANUAL. During the third sweep the start voltage was increased, causing baseline to shift to new start voltage.

Int/Ext

A switch located inside the generator (see Figure 5), accessed by opening the front panel (use knob on the right-hand side of the front panel). In the INT position the ramp voltage is controlled by the program. In the EXT position the ramp voltage can be controlled by a 0-10-V analog signal supplied through a rear-panel BNC.



Pushing START will now initiate ramp generation. If SINGLE SWEEP has been set, the generator will produce the above pattern once each time START is pushed.

NOTE: The SCOPE SWEEP output always ramps from 0 to 10 V (or whatever the gain setting happens to be) in the ramp time programmed at the first step. Thus, when a voltage excursion in any step after Step 1 is greater than the initial voltage excursion, the scope output will ramp up to 10 V before the quad ramp is finished, return to 0 V, and begin ramping again. If a voltage step following the first is smaller, the scope ramp will terminate before it has reached 10 V and begin a new excursion at the beginning of the next quad step output (a desirable condition).

Program Description

There are three major program branches, called Manual, Store, and Start. The following is a brief description of each branch. By referring to the flow chart (Figure 6) and the program manuscript in Appendix A, detailed operation will be apparent.

Program Branches

Manual--The program initially enters a loop and sense routine, waiting for a front-panel switch activation. If manual operation is commanded, the positions of each of the start voltage switches are read and the data are immediately deposited in the start level register, A6, causing the dc output voltage to the quadrupole tube to follow the commanded voltage. Start-switch sensing and register depositing are continuous as long as the manual mode switch is activated.

Store--When the store switch is activated, the program reads the front-panel start voltage, stop voltage, and ramp time switches and stores the data in the on-board random-access memory (RAM). The location in the RAM is determined by the number of store-switch operations. RAM data locations are shown on the RAM register maps, Figures 7a and 7b. After storing all switch data, the Floating Point Arithmetic unit (FPAR) calculates ΔV by subtracting the stop level from the start level and stores the results in RAM. The FPAR then calculates the cotangent by dividing the ramp time by ΔV , and this result is also stored in the RAM. (An outline description of how the FPAR works is given at the end of this section.)

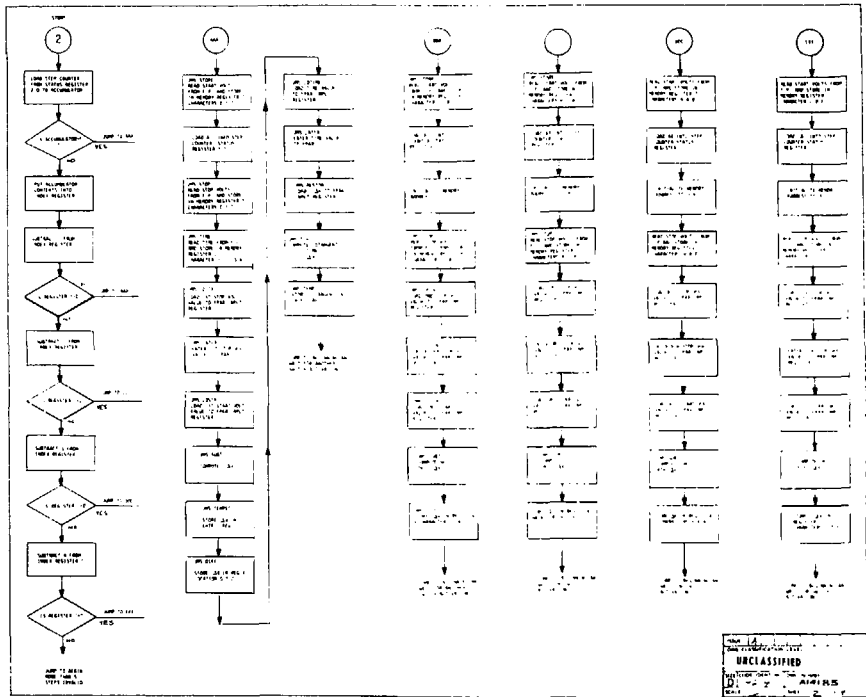


Figure 6 (cont.)

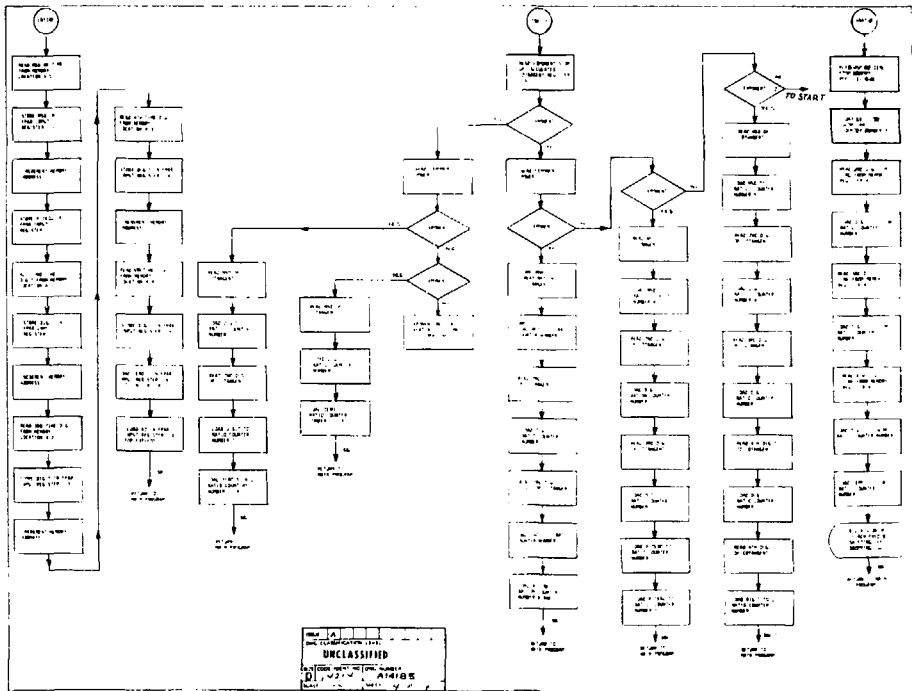
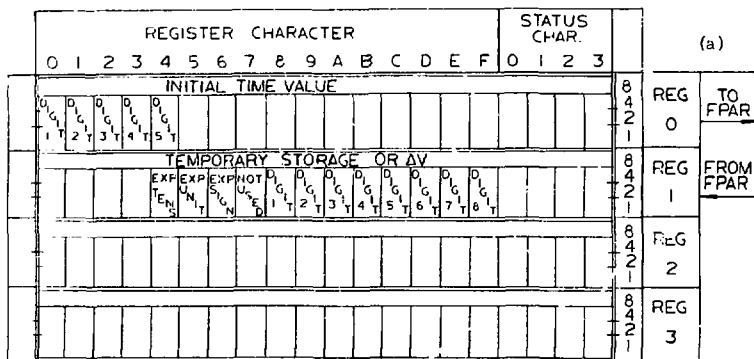
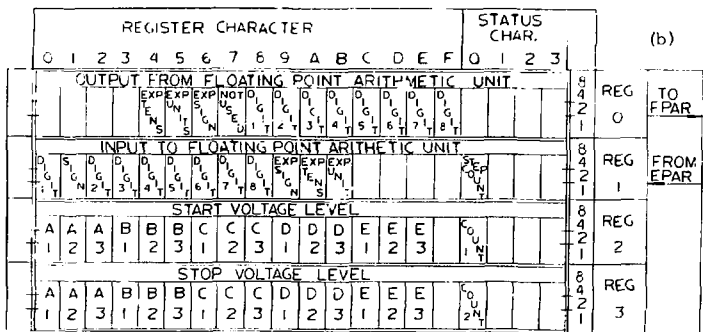


Figure 6 (cont.)



INTEL 4002-1 RAM REGISTER MAP #1



INTEL 4002-1 RAM REGISTER MAP #2

Figure 7. RAM Register Maps for Programmable Ramp Generator

Angle information for driving the quadrupole tube at the desired ramp angle is now stored. The program then returns to the loop and sense routine, awaiting further commands. If the STORE switch is again activated, the preceding will be repeated but the RAM locations will be different.

Start--When the START switch is activated, the program first calculates the angle cotangent for the scope ramp output. The FPAR does this by dividing the ramp time (read from the RAM) by the GAIN setting (nominally 10 V), the maximum amplitude of the scope output. The result is placed in scope ramp register, A8, which the program accomplishes by placing a data digit at Output 2 and then activating the appropriate load line (L10-L14). A load line is activated by placement of the correct number at Output 3, which causes the corresponding line from the load line selector, A4, to be energized. The same technique is used for loading all other registers.

Next, the quad ratio register, A5, is loaded with the cotangent previously stored in the RAM. The quad start voltage level is subsequently extracted from the RAM and deposited in the start level register, A6. Finally, the start level for the scope ramp is placed in A9. With all registers loaded, a pulse is issued which dumps the register contents of A5 and A8 into mating counters, the clock is turned on, and ramping commences. During the ramping, the program counts each 10-mV increment in output voltage. For a one-step ramp, when the stop voltage has been reached and the REPETITIVE/SINGLE switch is in the single mode, the clock is turned off and the loop and sense routine is again entered. However, if a multiple-step ramp is programmed, the next start level is fetched from RAM and is properly deposited and the ramp output continues from the new level until the second stop level is reached. This process is continuous until the program is completed, after which the REPETITIVE/SINGLE switch is interrogated. If it is in the single mode, the clock is turned off and the program awaits further commands; if it is in the repetitive mode, the entire program is repeated.

FPAR--The FPAR operates broadly as follows:* Upon ac power turn-on or manual reset, the program enters a subroutine CALRDY which initializes the FPAR by first manipulating the hold line and then waiting for certain timing relationships between RDYI and RDYO signals. A series of three commands subsequently enters, a master clear code followed by an error clear and a code which specifies that the FPAR work with data in scientific notation. Eight digits, sign, exponent, and exponent signs must be presented to the FPAR fixed format (Figure 7a, Register 0). The RAM Register 0 is always used as input to the FPAR. Prior to an entry function or arithmetic operation, the 12 digits are first arranged in a correct format under program format control. After an operation, the result is removed by an

*For complete details see D. C. Macmillan, "A Floating Point Arithmetic Unit for Pro-Log Based Control Systems," Sandia Laboratories, SAND77-8041, January 1978.

output subroutine and placed in RAM Register 2 in the format and location shown on the RAM register map (Figure 7a); however, the number in the FPAR is retained. Because of the FPAR timing constraints, the number is placed as the FPAR offers it in RAM Register 3. Other subroutines then unscramble Register 3 contents and move them to other registers.

Circuit Description

The programmable RAM generator block diagram shown in Figure 8 contains ten plug-in printed wiring boards, A1 through A13 (three boards required two spaces each). The circuits are a hybrid design of CMOS and TTL integrated-circuit packages. The following is a description of each board.

A1--The Program Logic System (Prolog Model PLS-441)--Contains the Intel 4040 microprocessor, the Intel 1702 programmable read-only memories for program storage (1280 words by 8 bits), the Intel P4001 RAMs (80 words x 4 bits), and the input/output ports (four each). Figure 9 illustrates the microprocessor port assignments.

A2--Floating Point Arithmetic Unit--Contains the National Semiconductor Model No. 57109 FPAR and associated control logic and performs all calculations.

A3--Clock and Switch Control--All front-panel switch controls are interfaced through this board for debouncing before connecting to the microprocessor. The 100-kHz system clock is also designed into this board. The square-wave output from the clock is formed by interconnecting three CMOS gates. In order to allow a slight modification of the analog output ramp angle, a front-panel ten-turn digital potentiometer provides $\pm 5\%$ change in clock frequency. Control lines are wired to the microprocessor Output 0 to control the on/off time of the clock.

A4--Load Line Selector--Contains the 4- to 16-line decoder. Decodes four BCD inputs from the microprocessor Output 3 to 1 of 16 mutually exclusive outputs. Each output line is connected to a load input on a data register. There is a common data line to all registers, with the program selecting what register receives which data. The program thus acts primarily as a data distributor and controller, sequentially removing data from the RAM or front-panel switches, placing it in a particular storage register, and then turning on the 100-kHz oscillator.

A5--Quadrupole Ramp Cotangent Register and Counter--A five-stage register and counter. The register is loaded initially with the calculated ratio of the time and the start/stop voltage difference. Under program control, the register is loaded into the five-stage counter, which then counts

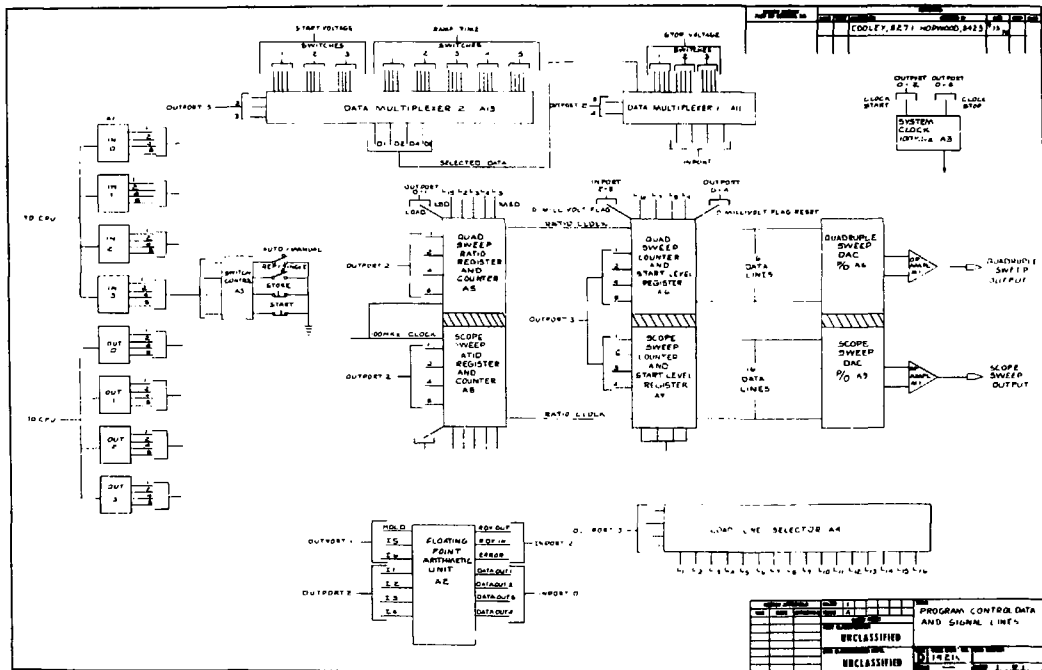


Figure 8. Block Diagram for Programmable Ramp Generator

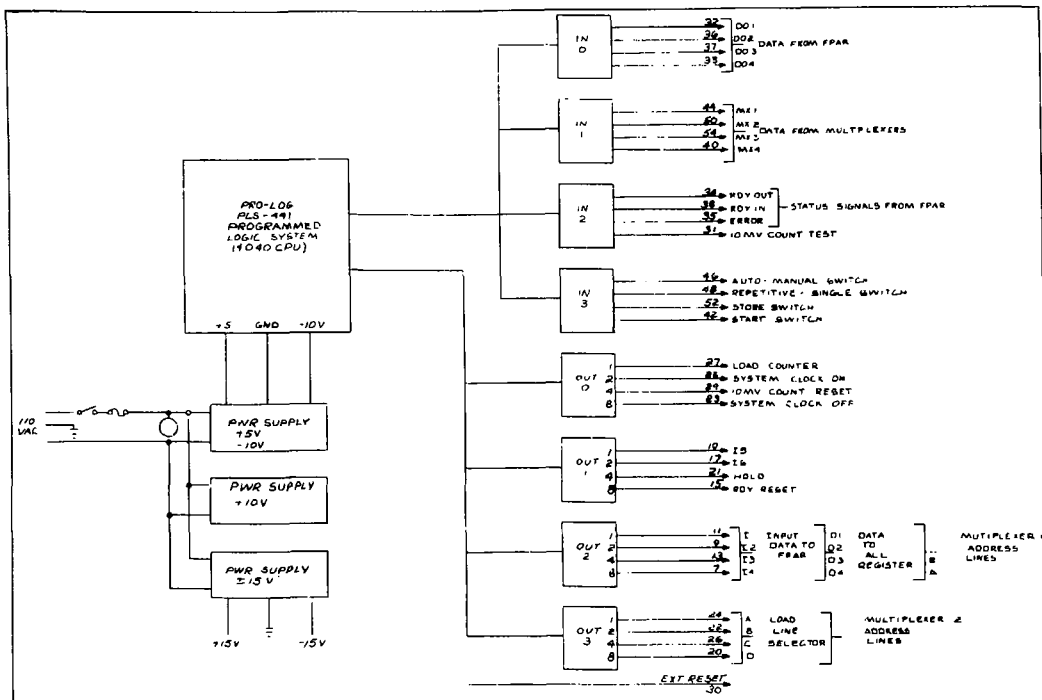


Figure 9. Microprocessor Port Assignments

down to 0 at a 100-kHz rate. On reaching 0 count a pulse is produced by a mono-stable multivibrator located on A5, which is connected to other circuits and eventually increments the analog ramp output voltage by 10 mV. In addition, the pulse causes the counter to be reloaded with the cotangent stored in the register. This process is continuous until the program stop voltage is reached.

A6--Quadrupole Ramp Counter and Start Level Register--A combined four-stage register, counter, and digital-to-analog converter. The 16 BCD output lines from the counter are connected to the inputs of a four-digit D/A converter. A counter state of zero results in 0 V, whereas the maximum counter state of 9999 results in -9.99 V from the D/A converter. Prior to the counting action, the initial start voltage is loaded from RAM under program control, resulting in an instantaneous change in the analog output voltage. The clock input for the counter is from the pulse produced from the cotangent counter previously described. Each clock input produces an output voltage change of 10 mV. Thus, for example, if an excursion of 10 V in 400.00 seconds is programmed, then the cotangent register contains the number 5000,

$$500.00 \text{ (sec)}/10 \text{ (V)} = 50.00 \text{ ,}$$

but 50.00 is read as 5000 by the register. The total time needed to empty the register for each 10-mV pulse is then (the clock period being 10 microseconds)

$$(5000)(10) = 50,000 \text{ microseconds .}$$

10,000 counts are required to the D/A converter for a 10-V output. The microprocessor reads and records each 10-mV increment and stops the 100-kHz clock when the stop voltage has been reached.

A7--An unused connector slot.

A8--Scope Sweep Cotangent Register and Counter--Operates identically to A6.

A9--Scope Ramp Counter and Start Level Register--Operates identically to A6, except that all load lines of the counter are common. Separate load lines are unnecessary since the start voltage is always zero.

A10--An unused connector slot.

A11--Data Multiplexer Number One and Output Amplifier--Consists of a 16-line to 4-line data selector. Data are selected by two address lines from the microprocessor Output 2. Input data to the multiplexer are from the panel stop voltage switch and data from Multiplexer 2. The two output

buffer amplifiers are connected in an inverting configuration to supply a ramp voltage of +10 V (nominal maximum) to the quadrupole tube of an oscilloscope horizontal axis. A gain adjustment located behind the front panel and accessible by the operator permits a change of $\pm 50\%$ in scope-drive output voltage.

A12--Data Multiplexer Number 2--This circuit utilizes four each, 8-line to 1-line data selectors, forming a 32-line to 4-line selector. Data are selected by three address lines of the microprocessor Output 3. Data input to the multiplexer is from the front-panel start voltage switches and ramp time switches. The output is connected directly to the microprocessor Input 1.

The detailed schematic, wiring list, and chassis mechanical drawings are included in Appendix B.

APPENDIX A
PROGRAM FOR THE RAMP GENERATOR

```

2 001000      NOP
3 001001      INITI   JMS      CALRDY
4 001003      BEGINI  FIM      0,0,0
5 001005      SRC      0,
6 001006      LDH      0,
7 001007      WRR
8 001010      CLB
9 001011      WRR
10 01012      FIM      3,3,0
11 01014      SRC      3
12 01015      RDR
13 01016      RAL
14 01017      JCN      C0,ST
15 01021      JUN      STAPT
16 01023      STI     RAL
17 01024      JCN      C0,MANU
18 01026      JUN      DEBOUC
19 01030      HANUI   ROR
20 01031      RAR
21 01032      JCN      C1,BEGIN
22 01034      JMS      STORL1
23 01036      JMS      STRLEV
24 01040      JUN      BEGIN
25 01042      DEBOUC1 CLB
26 01043      ROR
27 01044      RAL
28 01045      RAL
29 01046      JCN      C1,DEBOUC
30 01050      JUN      STORL
31 01052      STARTI FIM      2,2,0      /SAVE ORIGINAL STATUS COUNTERX
32 01054      FIM      3,3,0
33 01056      SRC      2
34 01057      RDB
35 01060      SRC      1
36 01061      WR0
37 01062      JMS      TIME      /FETCH THE FINAL TIME SWITCH SETTI
38 01064      JMS      SRATIO   /LOAD THE SCOPE RATIO INTO COUNTER
39 01066      JMS      TRATIO   /LOAD RATIO INTO QUAD COUNTERX
40 01070      JMS      STRLEV   /LOAD START LEVEL
41 01072      JMS      SCPLV    /LOAD 0 IN SCOPE D/A COUNTER
42 01074      FIM      0,0,0
43 01076      SRC      0
44 01077      LUM      1
45 01100      WRK
46 01101      CLB
47 01102      WRR      /INITIAL LOAD PULSE FOR RATIO COUN
48 01103      LUM      2
49 01104      WRR
50 01105      CLB
51 01106      WRK      /START CLOCK OSCILLATOR
52 01107      FIM      1,1,0      /INITIALIZE STEP STATUS REG
53 01111      LDH      3
54 01112      SRC      1
55 01113      WR0
56 01114      FIM      2,3,0
57 01116      MATT:   FIM      0,0,0      /REGISTER 0,1,2 WILL HOLD STDP VOL
58 01120      FIM      1,0,0
59 01122      FIM      3,0,0
60 01124      SRC      2
61 01125      ROM
62 01126      XCH      2
63 01127      INC      5
64 01130      SRC      2
65 01131      ROM

```


66	01152	XCH	1	
67	01153	INC	5	
68	01134	SRC	2	
69	01135	RDM		
70	01136	XCH	0	
71	01137	FIM	2,2,0	
72	01141	COUNT1: SRC	2	!WAIT FOR COUNTER FLIP=FLOP
73	01142	RDR		
74	01143	RAL		
75	01144	JCN	C0,COUNT	
76	01146	GO1: SRC	3	
77	01147	LDM	4	
78	01150	WRR		!RESET COUNT FLIP=FLOP
79	01151	CLB		
80	01152	WRR		
81	01153	SRC	2	
82	01154	RDR		
83	01155	RAL		
84	01156	JCN	C1,GO	!WAIT UNTIL CHANGE
85	01160	LD	0	
86	01161	JCN	A1,RED	
87	01163	LDM	9.	!REG2 IS 0 LSD<
88	01164	XCH	0	!PUT A 9 IN REG 2
89	01165	LD	1	
90	01166	JCN	A1,REDA	
91	01170	LDM	9.	
92	01171	XCH	1	
93	01172	LD	2	
94	01173	JCN	A1,REDB	
95	01175	JUN	0E	!ALL ZEROS HAVE BEEN REACHED
96	01177	RED1: DAC		
97	01200	XCH	0	
98	01201	JUN	COUNT	
99	01203	REDA1: DAC		
100	1204	XCH	1	
101	1205	JUN	COUNT	
102	1207	REDB1: DAC		
103	1210	XCH	2	
104	1211	JUN	COUNT	
105	1213	ULT: FIM	2,2,0	!STOP VOLTAGE HAS BEEN REACHED
106	1215	SRC	2	
107	1216	R00		
108	1217	DAC		
109	1220	JCN	A1,HOP	
110	1222	JUN	DONE	
111	1224	HOP1: WR0		
112	1225	FIM	0,2,0	
113	1227	FIM	1,1,0	
114	1231	SRC	1	
115	1232	WR0		
116	1233	XCH	1	
117	1234	JMS	STLEVA	
118	1236	FIM	2,3,0	
119	1240	FIM	1,1,0	
120	1242	SRC	1	
121	1243	R00		
122	1244	XCH	5	
123	1245	R00		
124	1246	IAC		
125	1247	IAC		
126	1250	IAC		
127	1251	WR0		
128	1252	JMS	SCPLEV	
129	1254	JUN	MATT	
130	1256	DONE1: FIM	2,2,0	
131	1260	FIM	3,3,0	
132	1262	SRC	3	

133	1263	R00		
134	1264	SRC	2	
135	1265	WR0		RESTORE STATUS REGISTER BEFORE LE
136	1266	FIM	3,3,0	ICHECK TO SEE POSITION OF REP-8ING
137	1270	SRC	3	
138	1271	CLB		
139	1272	RDR		
140	1273	RAR		
141	1274	RAR		
142	1275	JCN	CO,DEB	
143	1277	FIM	0,3,0	ICHECK FOR MANUAL OPER.
144	1301	SRC	0	
145	1302	RDR		
146	1303	RAR		
147	1304	JCN	CO,MANUAL	
148	1306	JUN	START	
149	1310	MANUAL: JMS	STORE1	
150	1312	JUN	START	ISWITCH IS IN REP POSITION
151	1314	DEB: JUN	MEGIN	ISWITCH IS IN SINGLE POSITIONX
152	1316	LOSTR: FIM	2,2,0.	FLOAD STOP VALUE IN FPAR REGISTER
153	1320	FIM	0,3,0	ISTOP ADDRESS IN RAM
154	1322	FIM	1,1,3	
155	1324	LOSTR: SRC	0	
156	1325	RDM		
157	1326	SRC	1	
158	1327	WRM		
159	1330	FIM	1,1,1	
160	1332	CLB		
161	1333	SRC	1	
162	1334	WRM		ISIGN IS PLUS
163	1335	INC	1	
164	1336	INC	3	
165	1337	SRC	0	
166	1340	RDM		
167	1341	SRC	1	
168	1342	WRM		
169	1343	INC	1	
170	1344	FIM	1,1,0	
171	1346	SRC	0	
172	1347	RDM		
173	1350	SRC	1	
174	1351	WRM		
175	1352	FIM	1,1,3	
176	1354	ZERO: INC	3	
177	1355	CLB		
178	1356	SRC	1	
179	1357	WRM		
180	1360	ISZ	5,ZERO	ILOAD 0 ZEROS
181	1362	BBL	0	
182	1363	LOSTR: FIM	2,2,0.	ILOAD FIRST START VALUE IN FPAR RE
183	1365	FIM	0,2,0	
184	1367	FIM	1,1,3	
185	1371	JMS	LOSTR1	
186	1373	BBL	0	
187	1374	TEMPST: FIM	0,0,4	IOUTPUT FROM FPAR ADDRESS
188	1376	FIM	1,5,4	
189	1400	FIM	2,0,4	
190	1402	TRANS: SRC	0	
191	1403	RDM		
192	1404	SRC	1	
193	1405	WRM		
194	1406	INC	1	
195	1407	INC	3	
196	1410	ISZ	5,TRANS	
197	1412	BBL	0	
198	1413	RESTOR: FIM	0,1,0	
199	1415	FIM	1,5,8.	

200	1417		FIM	0,9.	
201	1421		SRC	.	
202	1422		MDM		
203	1423		SRC	0	
204	1424		WRM		
205	1425		INC	1	
206	1426		CLB		
207	1427		SRC	0	
208	1430		WRM		1* SIGN
209	1431	ZERUBI	INC	1	
210	1432		INC	3	
211	1433		SRC	1	
212	1434		RDM		
213	1435		SRC	0	
214	1436		WRM		
215	1437		ISZ	5,ZERUB	TRANSFER 7 DIGITS
216	1441		FIM	1,5,6	
217	1443		SRC	1	
218	1444		RDM		
219	1445		RAM		
220	1446		JCN	U1,MINUS	
221	1450		FIM	0,1,9.	
222	1452		CLB		
223	1453		SRC	0	
224	1454		WRM		78 # 0
225	1455		JUN	PLU	
226	1457	MINUS:	FIM	0,1,4.	
227	1461		LDM	F	
228	1462		SWL	0	
229	1463		WRM		MINUS # F
230	1464	PLUS:	FIM	1,5,4	
231	1466		INC	1	
232	1467		SRC	1	
233	1470		RDM		
234	1471		SRC	0	
235	1472		WRM		WRITE TENS EXPONENT
236	1473		INC	1	
237	1474		INC	3	
238	1475		SRC	1	
239	1476		RDM		
240	1477		SRC	0	
241	1500		WRM		
242	1501		BBL	0	TRANSFER COMPLETE
243	1502	STHLEV:	FIM	0,2,0	FROM ADDRESS
244	1504	STLEVA:	FIM	1,1,0	
245	1506		FIM	2,2,0	
246	1510		FIM	3,3,0	
247	1512		CLB		
248	1513		SRC	2	
249	1514		WRM		
250	1515		LDM	5	
251	1516		JMS	FILL	LOAD LSD IN LEVEL COUNTER
252	1520		SRC	0	
253	1521		RDM		READ MSB OF START VOLTAGE
254	1522		SRC	2	
255	1523		WRM		INPUT TO PORT 2
256	1524		LDM	6	
257	1525		JMS	FILL	LOAD LSD OF START VOLTAGE
258	1527		INC	1	
259	1530		SRC	0	
260	1531		RDM		
261	1532		SRC	2	
262	1533		WRM		
263	1534		LDM	7	
264	1535		JMS	FILL	LOAD SECOND DIGIT
265	1537		INC	1	
266	1540		SRC	0	

267	1541		RDM		
268	1542		SRC	2	
269	1543		WRR		
270	1544		LDM	0	
271	1545		JMS	FILL	LOAD THIRD DIGIT
272	1547		BBL	0	
273	1550	STORE1	CLB		
274	1551		FIM	0,2,0	
275	1553		SRC	0	
276	1554		R00		LOAD STATUS REGISTER
277	1555		JCN	A1,AA	
278	1557		JUN	AAA	
279	1561	AAI	XCM	1	
280	1562		LDM	1	
281	1563		SUB	1	
282	1564		JCN	A1,BB	
283	1566		JUN	BBB	
284	1570	BBI	LDM	2	
285	1571		SUB	1	
286	1572		JCN	A1,CC	
287	1574		JUN	CCC	
288	1576	CCI	LDM	3	
289	1577		SUB	1	
290	1600		JCN	A1,DD	
291	1602		JUN	DDD	
292	1604	OUI	LDM	4	
293	1605		SUB	1	
294	1606		JCN	A1,EE	
295	1610		JUN	EEE	
296	1612	EEI	JUN	BEGIN	
297	1614	AAAA	JMS	STORE1	
298	1616		FIM	0,2,0	
299	1620		LDM	1	
300	1621		SRC	0	
301	1622		NR0		PUT A L INTO STATUS REG
302	1623		JMS	STOP	FETCH AND STORE STOP VALUE
303	1625		JMS	TIME	FETCH AND STORE TIME VALUE
304	1627		JMS	LOSTP	LOAD STOP VALUE IN FPAR REG
305	1631		JMS	ENTER	
306	1633		JMS	LDSTR	LOAD START VALUE IN FPAR REG
307	1635		JMS	SUBT	
308	1637		JMS	TEMPST	TEMPORARILY STORE DIFF
309	1641		FIM	3,3,0	
310	1643		JMS	UIFF	RELOAD DIFFERENCE INTO CHIP 3,3,0
311	1645		JMS	LDTIME	LOAD TIME INTO FPAR
312	1647		JMS	ENTER	
313	1651		JMS	RESTDUR	LOAD DIFFERENCE INTO FPAR
314	1653		JMS	UIV	
315	1655		JMS	TEMPST	STORE 0 RATIO IN 1 REG 2
316	1657		JUN	BEGIN	
317	1661	BBBB	FIM	2,2,3	
318	1663		JMS	STORE2	
319	1665		FIM	0,2,0	
320	1667		LDM	2	
321	1670		SRC	0	
322	1671		NR0		
323	1672		FIM	3,3,3	
324	1674		JMS	STOP2	FETCH AND STORE SECOND STOP VALUE
325	1676		FIM	2,2,0	
326	1700		FIM	0,3,3	STOP ADDRESS IN RAM
327	1702		JMS	CVCC	
328	1704		FIM	0,2,3	
329	1706		FIM	1,1,3	
330	1710		JMS	LOSTR1	LOAD SECOND START VALUE IN FPAR
331	1712		JMS	SUBT	
332	1714		FIM	3,3,3	

333	1716	JMS	DIFF	STORE DIFFERENCE IN RAM 0,3,4,5
334	1720	JUN	BEGIN	
335	1722	FIM	4,2,6	
336	1724	JMS	STORE2	
337	1726	FIM	0,2,0	
338	1730	LDM	5	
339	1731	SRC	0	
340	1732	WR0		STORE A 3 IN STATUS REGISTERX
341	1735	FIM	3,3,6	
342	1735	JMS	STOP2	STORE THIRD STOP VALUE
343	1737	FIM	2,2,8.	
344	1741	FIM	0,3,6	
345	1743	JMS	CVCC	
346	1745	FIM	0,2,6	
347	1747	FIM	1,1,3	
348	1751	JMS	LDSTR1	
349	1753	JMS	SUBT	
350	1755	FIM	3,3,6	
351	1757	JMS	UIFF	
352	1761	JUN	BEGIN	
353	1763	FIM	2,2,9.	
354	1765	JMS	STORE2	STORE FOURTH STOP VALUE
355	1767	FIM	0,2,0	
356	1771	LDM	4	
357	1772	SRC	0	
358	1773	WR0		
359	1774	FIM	3,3,9.	
360	1776	JMS	STOP2	
361	2000	FIM	2,2,8.	
362	2002	FIM	0,3,9.	
363	2004	JMS	CVCC	
364	2006	FIM	0,2,9.	
365	2010	FIM	1,1,3	
366	2012	JMS	LDSTR1	
367	2014	JMS	SUBT	
368	2016	FIM	3,3,9.	
369	2020	JMS	DIFF	
370	2022	JUN	BEGIN	
371	2024	FIM	2,2,C	
372	2026	JMS	STORE2	STORE FIFTH STOP VALUE
373	2030	FIM	0,2,0	
374	2032	LDM	5	
375	2033	SRC	0	
376	2034	WR0		LOAD A 5 IN STATUS REGISTER
377	2035	FIM	3,3,C	
378	2037	JMS	STOP2	
379	2041	FIM	2,2,8.	
380	2043	FIM	0,3,C	
381	2045	JMS	CVCC	
382	2047	FIM	0,2,C	
383	2051	FIM	1,1,3	
384	2053	JMS	LDSTR1	
385	2055	JMS	SUBT	
386	2057	FIM	3,3,C	
387	2061	JMS	UIFF	
388	2063	JUN	BEGIN	CALL DIFFERENCE CALCULATED AND STO
389	2065	FIM	1,1,3	
390	2067	JMS	LDSTR1	
391	2071	JMS	ENTEM	
392	2073	FIM	2,2,0.	
393	2075	BBL	0	
394	2076	FIM	3,3,0	REGISTER 1 # MPX1 ADDRESS
395	2100	FIM	2,2,0	
396	2102	FIM	1,1,0	
397	2104	LDM	8.	
398	2105	SRC	2	
399	2106	WRM		MPX1 # 1X
400	2107	SRL	1	

401	2110	KOM			
402	2111	SRC			
403	2112	WRM			JSTORE FIRST DIGIT OF STP=1 IN
404	2113	INC		7	JCHIP 0 REGISTER 3 CHR0
405	2114	LDM		4	
406	2115	SRC		2	
407	2116	WRM			JMPX1 # 2X
408	2117	SRC		1	
409	2120	RDR			
410	2121	SRC		3	
411	2122	WRM			JSTORE STP=2
412	2123	INC		7	
413	2124	LDM		C	
414	2125	SRC		2	
415	2126	WRM			
416	2127	SRC		1	
417	2130	RDR			
418	2131	SRC		3	
419	2132	WRM			JSTORE STP=3
420	2133	DBL		0	
421	2134	TIME1 FIM		3,3,7	JSTORE TIME VALUE
422	2136	FIM		0,4,0	JRAM ADDRESS
423	2140	FIM		1,1,0	
424	2142	FIM		2,2,C	
425	2144	CLD			
426	2145	SRC		2	
427	2146	WRM			JMPX1 ADDRESS # 0
428	2147	LD		7	
429	2150	SRC		3	
430	2151	WRM			JMPX2 ADDRESS # 3
431	2152	SRC		1	
432	2153	RDM			JREAD FIRST DIGIT
433	2154	SRC		0	
434	2155	WRM			JSTORE FIRST TIME DIGIT,MSC
435	2156	TIMEA1 KCH		7	
436	2157	DAC			
437	2160	KCH		7	
438	2161	LD		7	
439	2162	INC		1	
440	2163	SRC		3	
441	2164	WRM			JMPX2 ADDRESS # 4
442	2165	SRC		1	
443	2166	HUR			
444	2167	SRC		0	
445	2170	WRM			JSTORE SECOND TIME DIGIT
446	2171	ISZ		5,TIMEA	JSTORE FIFTH DIGIT
447	2173	DBL		0	
448	2174	STORE11 FIM		2,2,0	JMPX1 ADDRESS
449	2176	STORE21 FIM		1,1,0	JMPX2 ADDRESS,
450	2200	FIM		0,0,0	JRAM ADDRESS
451	2202	FIM		3,3,0	
452	2204	LD		1	
453	2205	SRC		2	
454	2206	WRM			JMPX1 ADDRESS # 0
455	2207	LD		3	
456	2210	SRC		3	
457	2211	WRM			JMPX2 ADDRESS # 0
458	2212	SPC		1	
459	2213	KDM			JREAD STR=1
460	2214	SRC		2	
461	2215	WRM			JSTORE STR=1 IN CHIP 0 REG 2 CHAR
462	2216	INC		5	
463	2217	INC		3	
464	2220	LD		3	
465	2221	SRC		3	
466	2222	WRM			JMPX2 ADDRESS # 1
467	2223	SRC		1	

466	2224		RDF		JHEAD STR=2
469	2225		SWC	2	
470	2226		WRM		JSTORE STR=2
471	2227		INC	5	
472	2230		INC	3	
473	2231		LD	1	
474	2232		SWC	3	
475	2233		WRM		JMPX=2 ADDRESS # 2
476	2234		SWC	1	
477	2235		RDR		JHEAD STR=3
478	2236		SWC	2	
479	2237		WRM		JSTORE STR=2
480	2240		BBL	0	
481	2241	LDTIME1	FIM	0,1,0	
482	2243		FIM	1,4,0	
483	2245		FIM	2,0,0	
484	2247		SRC	1	
485	2250		RDM		
486	2251		SWC	0	
487	2252		WRM		
488	2253		INC	1	
489	2254		CLB		
490	2255		SRC	0	
491	2256		WRM		J6
492	2257		INC	1	
493	2260		INC	3	
494	2261		SRC	1	
495	2262		RDM		J02
496	2263		SWC	0	
497	2264		WRM		
498	2265		INC	1	
499	2266		INC	3	
500	2267		SRC	1	
501	2270		RDM		J03
502	2271		SWC	0	
503	2272		WRM		
504	2273		INC	1	
505	2274		INC	3	
506	2275		SWC	1	
507	2276		RDM		J04
508	2277		SRC	0	
509	2500		WRM		
510	2301		INC	1	
511	2302		INC	3	
512	2303		SWC	1	
513	2304		RDM		
514	2305		SWC	0	
515	2306		WRM		J05
516	2307	ZERU2	INC	1	
517	2310		CLB		
518	2311		SWC	0	
519	2312		WRM		
520	2313		ISZ	5,ZERU2	
521	2315		INC	1	
522	2316		COM	2	
523	2317		SWC	0	
524	2320		WRM		JLOAD 2 IN 103 EXPONENT
525	2321		BBL	0	
526	2322	SCPLEV1	FIM	7,2,0	JLOAD ZEROS IN SCOPE 0/A FOR START
527	2324		FIM	3,3,0	
528	2326		SRC	7	
529	2327		CLB		
530	2330		WRM		
531	2331		LDM	F	
532	2332		JMS	FILL	JLOAD SECOND STAGE
533	2334		BBL	0	
534	2335	DIFF1	FIM	0,0,5	

535	2337	SRC	0	
536	2340	RDM		IHEAD FIRST EXPONENT
537	2341	JLN	A0,NOEXP	
538	2343	JUN	SHIFT	
539	2345	FIM	0,0,8,	
540	2347	SRC	0	
541	2350	RDM		
542	2351	SRC	3	I DIFFERENCE RAM ADDRESS
543	2352	WRM		
544	2353	INC	7	I INCREMENT RAM DIFF ADDRESS
545	2354	INC	1	
546	2355	SRC	0	
547	2356	RDM		
548	2357	SRC	3	I STORE SECOND DIGIT OF DIFF
549	2360	WRM		
550	2361	INC	7	
551	2362	INC	1	
552	2363	SRC	0	
553	2364	RDM		
554	2365	SRC	3	I STORE THIRD DIGIT OF DIFF
555	2366	WRM		
556	2367	BBL	0	
557	2370	SHIFT1	RAR	
558	2371	JCN	A0,ONEEXP	
559	2373	JUN	SHIFT2	
560	2375	ONEEXP1	FIM	0,0,8,
561	2377	CLB		
562	2400	SRC	3	
563	2401	WRM		I PUT 0 IN FIRST DIGIT
564	2402	INC	7	I INC RAM DIFF ADDRESS
565	2403	SRC	0	
566	2404	RDM		I READ 01
567	2405	SRC	3	
568	2406	WRM		I WRITE SECOND DIGIT OF DIFF
569	2407	INC	7	
570	2410	INC	1	
571	2411	SRC	0	
572	2412	RDM		
573	2413	SRC	3	
574	2414	WRM		I WRITE THIRD DIGIT OF DIFF
575	2415	BBL	0	
576	2416	SHIFT21	FIM	0,0,8,
577	2420	CLB		
578	2421	SRC	3	
579	2422	WRM		I PUT 0 IN FIRST DIFF DIGIT
580	2423	INC	7	
581	2424	SRC	3	
582	2425	WRM		I PUT 0 IN SECOND DIFF DIGIT
583	2426	INC	7	
584	2427	SRC	0	
585	2430	RDM		I HEAD 01 FROM PPAR
586	2431	SRC	3	
587	2432	WRM		I WRITE THIRD DIFF DIGIT
588	2433	BBL	0	
589	2434	THATIU1	FIM	0,5,6
590	2436	FIM	2,2,0	I LOAD RATIO INTO COUNTER
591	2440	FIM	3,3,0	
592	2442	SRC	0	
593	2443	RDM		I HEAD SIGN OF EXPONENT
594	2444	RAR		
595	2445	JCN	C0,PLSEXP	
596	2447	CLB		
597	2450	JUN	MINEXP	
598	2452	FIM	0,5,5	
599	2454	SRC	0	
600	2455	RDM		I READ ONE'S EXPONENT
601	2456	JCN	A0,PZEN	

602	2460		HAR			
603	2461		JCN	A0,PUNE		
604	2463		JUN	PTWO		
605	2465	PZLN1	FIM	0,5,7		
606	2467		JMS	NOM		JHEAD MSBX
607	2471		LOM	2		
608	2472		JMS	FILL		
609	2474		JMS	NOM		JHEAD SECOND DIGIT
610	2476		LOM	1		
611	2477		JMS	FILL		
612	2501		JMS	NOM		
613	2503		LOM	E		
614	2504		JMS	FILL		
615	2506		CLB			
616	2507		SRC	2		
617	2510		HRR			
618	2511		JMS	FILLC		JPUT 0 IN LC,LD
619	2513		BBL	0		
620	2514	PTWU1	FIM	0,5,0.		
621	2516		JMS	PTW		
622	2520		FIM	0,5,7		
623	2522		JMS	NOM		
624	2524		LOM	4		
625	2525		JMS	FILL		
626	2527		BBL	0		
627	2530	PUNE1	FIM	0,5,7		JEXP = 001, CANNOT BE GREATER
628	2532	PTW:	JMS	NOM		
629	2534		LOM	3		
630	2535		JMS	FILL		
631	2537		JMS	NOM		JHEAD SECOND DIGIT
632	2541		LOM	2		
633	2542		JMS	FILL		
634	2544		JMS	NOM		
635	2546		LOM	1		
636	2547		JMS	FILL		
637	2551		CLB			
638	2552		SRC	2		
639	2553		HRR			
640	2554		LOM	4		
641	2555		JMS	FILL		
642	2557		LOM	E		
643	2560		JMS	FILL		
644	2562		BBL	0		
645	2563	MINEXP1	FIM	0,5,5		JMINUS EXPONENT
646	2565		SRC	0		
647	2566		RDM			
648	2567		HAR			
649	2570		JCN	A0,MONE		
650	2572		RAR			
651	2573		JCN	A1,MUNE JEXP==3, ILLEGAL,TREAT AS EXP==1		
652	2575		JUN	MTWO		
653	2577	MDNE1	FIM	0,5,7		JEXP = 001
654	2621		JMS	NOM		
655	2623		LOM	1		
656	2624		JMS	FILL		
657	2626		JMS	NOM		
658	2610		LOM	E		
659	2611		JMS	FILL		
660	2613		CLB			
661	2614		SRC	2		
662	2615		HRR			
663	2616		JMS	FILLB		
664	2620		BBL	0		
665	2621	MTWU1	FIM	0,5,7		JEXP = 002
666	2623		JMS	NOM		
667	2625		LOM	E		
668	2626		JMS	FILL		

669	2630	CLB		
670	2631	SRC	<	
671	2632	WMM		
672	2633	FILLA:	LDM	1
673	2634		JMS	FILL
674	2636	FILLB:	LDM	2
675	2637		JMS	FILL
676	2641	FILLC:	LDM	3
677	2642		JMS	FILL
678	2644	FILLD:	LDM	4
679	2645		JMS	FILL
680	2647		BBL	0
681	2650	FILL:	SRC	3
682	2651		WMM	
683	2652		CLB	
684	2653		WMM	
685	2654		BBL	0
686	2655	RDHI:	INC	1
687	2656		SRC	0
688	2657		RDM	
689	2660		SRC	2
690	2661		WMM	
691	2662		BBL	0
692	2663	SHATIO:	FIM	0,4,0
693	2665		FIM	2,2,0
694	2667		FIM	3,3,0
695	2671		SRC	0
696	2672		RDM	
697	2673		SRC	2
698	2674	WRR		
699	2675		LDM	0
700	2676		JMS	FILL
701	2700		INC	1
702	2701		SRC	0
703	2702		RDM	
704	2703		SRC	2
705	2704		WMM	
706	2705		LDM	0
707	2706		JMS	FILL
708	2710		INC	1
709	2711		SRC	0
710	2712		RDM	
711	2713		SRC	2
712	2714	WRR		
713	2715		LDM	4
714	2716		JMS	FILL
715	2720		INC	1
716	2721		SRC	0
717	2722		RDM	
718	2723		SRC	2
719	2724	WRR		
720	2725		LDM	4
721	2726		JMS	FILL
722	2730		CLB	
723	2731		SRC	2
724	2732		WMM	
725	2733		LDM	0
726	2734		JMS	FILL
727	2736		BBL	0
728	2737	CALWDY:	JMS	DELAY
729	2741		FIM	3,2,2
730	2743		FIM	2,1,0
731	2745		SRC	3
732	2746	READ1:	RDM	
733	2747		AND	2
734	2750		JCN	AD,READ1
735	2752	READ2:	ROR	

ISTROBE DATA INTO SELECTED REGISTE
ISTROBE L LINE

INCREMENT MEM ADDRESS AND HEAD

INREAD CHARACTER

INWRITE DATA TO OUTPUT 2

INDROP LSD TO EFFECT A DIVISION OF

INLOAD 02 IN LSD

INPUT A 0 IN MS0

INREAD PORT 2

INAND 2

INAD,READ1 INWHEN ROY1 = 1 THEN CONTINUE

736 2753	AN7		TANQ BIT 2
737 2754	JCN	A1,HEAD2	
738 2756	LDM	4	
739 2757	SRC	2	
740 2760	HRH		FSET HOLDX
741 2761	SAC	3	
742 2762	HEAD3:	RDM	
743 2765	AN7		
744 2766	JCN	A0,HEAD3	JWHEN RDUYI = 1 THEN CONTINUE
745 2766	FIM	5,2,F	
746 2770	JMS	LOAD	FSEND MASTER CLEAR
747 2772	FIM	5,2,3	
748 2774	JMS	LOAD	FSEND ERROR CLEAR
749 2776	FIM	5,2,2	
750 2800	JMS	LOAD	FSEND SCIENTIFIC NOTATION
751 2802	BBL	0	
752 2803	DELAY:	FIM	0,0,0
753 2805		FIM	1,0,0
754 2807	WAIT:	ISZ	0,WAIT
755 2811		ISZ	1,WAIT
756 2813		ISZ	2,WAIT
757 2815		ISZ	3,WAIT
758 2817		BBL	0
759 2820	SUBT:	JMS	LDRAM
760 2822		FIM	5,5,A
761 2824		JMS	LOAD
762 2826		JMS	OUTPUT
763 2828		BBL	0
764 2831	LOAD:	FIM	2,2,4
765 2833		FIM	1,1,0
766 2835		SAC	2
767 2836		LD	0
768 2837		HRH	
769 2840		SRC	1
770 2841		LD	A
771 2842		HRH	
772 2843		SRC	2
773 2844	RDYA:	RDM	
774 2845		RAR	
775 2846		RAH	
776 2847		JCN	C1,RDYA
777 2851		LD	A
778 2852		DR3	
779 2853		SRC	1
780 2854		HRH	
781 2855		SAC	2
782 2856	RDYB:	CLB	
783 2857		RDR	
784 2860		RAR	
785 2861		RAR	
786 2862		JCN	C0,RDYB
787 2864		CLB	
788 2865		BBL	0
789 2866	OUTPUT:	FIM	5,1,6
790 2870		JMS	LOAD
791 2872		Sb1	
792 2875		FIM	1,1,0
793 2875		FIM	2,2,0
794 2877		SRC	1
795 2880		LDM	4
796 2881		HRH	
797 2882		LDM	L
798 2883		HRH	
799 2884		LDM	4
800 2885		HRH	
801 2886		CLB	
802 2887		HRH	

803	3110		SRC	2	
804	3111	REZY1	CLD		
805	3112		RDR		
806	3113		RAR		
807	3114		RAR		
808	3115		JCN	C1, REZY	
809	3117		SRC	1	
810	3120		LDM	4	
811	3121		WRR		
812	3122		FIM	2,0,4	
813	3124		FIM	3,2,1	
814	3126	STRT1	SRC	3	
815	3127	AGN11	RDN		
816	3130		ANT		
817	3131		JCN	A0,AGN1	
818	3133		SRC	2	
819	3134		RDR		
820	3135		WRM		
821	3136		INC	5	
822	3137		SRC	3	
823	3140	AGN21	RDR		
824	3141		ANT		
825	3142		JCN	A1,AGN2	
826	3144		SRC	2	
827	3145		RDR		
828	3146		WRM		
829	3147		ISZ	5,STRT	
830	3151		SRC	3	
831	3152	AGN31	RDR		
832	3153		JCN	A0,AGN3	
833	3155		FIM	2,1,0	
834	3157		FIM	3,2,0	
835	3161		LDM	4	
836	3162		SRC	2	
837	3163		WRR		
838	3164		LDM	C	
839	3165		WRR		
840	3166		LDM	4	
841	3167		WRR		
842	3170		SRC	5	
843	3171	COMPI	RDR		
844	3172		RAR		
845	3173		RAW		
846	3174		JCN	C1,COMP	
847	3176		CLB		
848	3177		DBL		
849	3200	LOHAM: FIM	FIM	5,5,0	;OP CODE ADDR
850	3202		FIM	1,1,0	IRAM ADDRESS REGISTER
851	3204		SRC	7	
852	3205		KUM		
853	3206		XCH	B	LOAD OP CODE INTO RB FIRST HALF
854	3207		CLB		
855	3210		XCH	A	LOAD OP CODE INTO RA SECOND HALF
856	3211		JMS	LOAD	
857	3213		INC	F	
858	3214		SRC	7	
859	3215		FIM	5,0,A	DECIMAL POINT OP CODE
860	3217		JMS	LOAD	
861	3221		INC	F	INCREMENT MEMORY A2
862	3222		SRC	F	
863	3223		RDM		IRHEAD 02
864	3224		XCH	B	LOAD OP CODE FIRST HALF
865	3225		LDM	0	
866	3226		XCH	A	LOAD OP CODE SECOND HALF
867	3227		JMS	LOAD	
868	3231		INC	F	
869	32		SRC	7	

870 3233	RDM		JKFAD D2
871 3234	XCM	0	
872 3235	LDM	0	
873 3236	XCM	A	
874 3237	JMS	LOAD	
875 3241	INC	F	IA4
876 3242	SRC	7	
877 3243	RDM		IHEAD D4
878 3244	XCM	0	
879 3245	LDM	0	
880 3246	XCM	A	
881 3247	JMS	LOAD	
882 3251	INC	F	IA5
883 3252	SWC	7	
884 3253	RDM		IHEAD D5
885 3254	XCM	0	
886 3255	LDM	0	
887 3256	XCM	A	
888 3257	JMS	LOAD	
889 3261	INC	F	IA6
890 3262	SRC	7	
891 3263	RDM		IHEAD D6
892 3264	XCM	0	
893 3265	LDM	0	
894 3266	XCM	A	
895 3267	JMS	LOAD	
896 3271	INC	F	IA7
897 3272	SWC	7	
898 3273	RDM		IHEAD D7
899 3274	XCM	0	
900 3275	LDM	0	
901 3276	XCM	A	
902 3277	JMS	LOAD	
903 3301	INC	F	IA8
904 3302	SWC	7	
905 3303	RDM		IHEAD D8
906 3304	XCM	0	
907 3305	LDM	0	
908 3306	XCM	A	
909 3307	JMS	LOAD	
910 3311	FIM	5,0,H	IEXPONENT OP CODE
911 3313	JMS	LOAD	
912 3315	INC	F	IA9
913 3316	SWC	7	
914 3317	RDM		IO9
915 3320	JCN	AB,EXP	F 0 IS + F IS -
916 3322	FIM	5,0,C	
917 3324	JMS	LOAD	
918 3326	INC	F	IAA
919 3327	SWC	7	
920 3330	RDM		IHEAD EXPONENT 10
921 3331	XCM	0	
922 3332	LDM	0	
923 3333	XCM	A	
924 3334	JMS	LOAD	
925 3336	INC	F	IAB
926 3337	SRC	7	
927 3340	RDM		IHEAD EXPONENT 1
928 3341	XCM	0	
929 3342	LDM	0	
930 3343	XCM	A	
931 3344	JMS	LOAD	
932 3346	BBL	0	
933 3347	JMS	LORAM	IENTER OP CODE
934 3351	FIM	5,2,1	
935 3353	JMS	LOAD	
936 3355	BBL	0	

EXPJ

ENTERI

937	3356	CLRI	FIM	5,2,F	MAST OF CLEAR OP CODE
938	3360		JMS	LOAD	
939	3362		BBL	0	
940	3363	DIV:	JMS	LDRAM	
941	3365		FIM	5,5,C	DIVIDE OP CODE
942	3367		JMS	LOAD	
943	3371		JMS	OUTPUT	
944	3373		BBL	0	
945		000001*,END			

#INTEL=4040 MACHO DEFINITIONS
SYMBOL TABLE

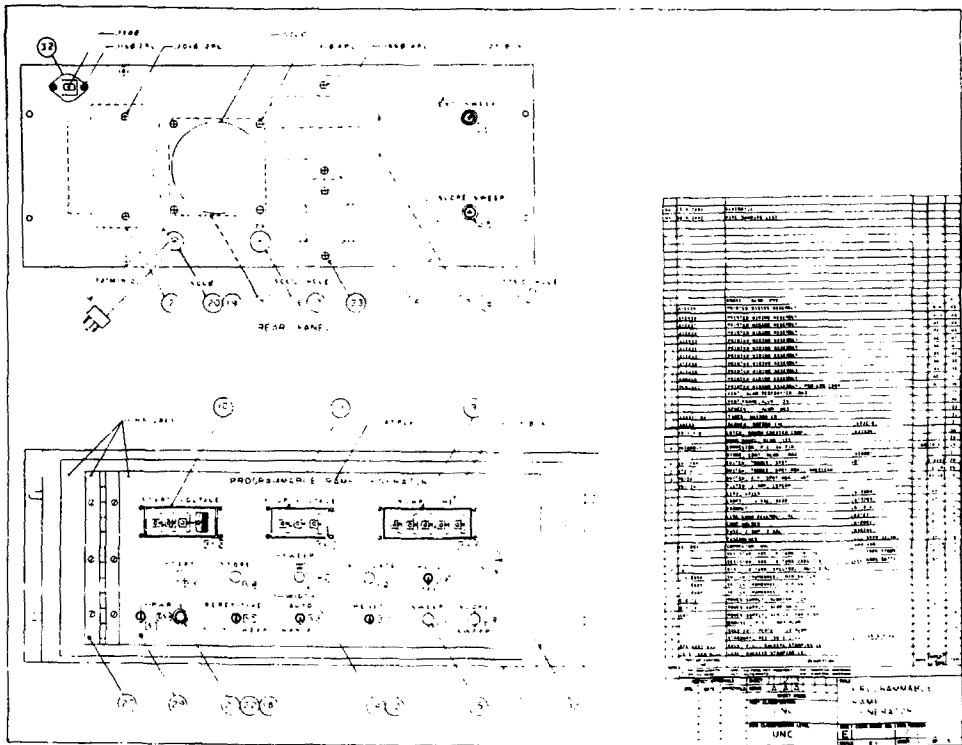
A	000012	AA	001561	AAA	001614
AGN1	003127	AGN2	003140	AGNS	003152
A0	000004	A1	000014	B	000013
BB	001570	BBB	001661	BEGIN	001003
C	000014	CALRDY	002737	CC	001576
CCC	001722	CLR	003356	COMP	003171
COUN1	001141	CVCC	002065	C0	000012
CSA1	000016	C1	000002	D	000015
DD	001604	DDD	001763	DE	001213
DEB	001314	DEBOUC	001042	DELAY	003003
DIFF	002335	DIV	003363	DONE	001256
E	000016	EE	001012	EEE	002024
ENTEN	003547	EXP	003326	F	000017
FILL	002650	FILLA	002633	FILLB	002636
FILLC	002641	FILLD	002644	GU	001146
HOP	001224	INIT	001001	J	*****
LDRAM	003200	LDSTP	001316	LOSTR	001363
LDSTN1	001324	LDTIME	002241	LOAD	003031
MANU	001030	MANUAL	001310	MATT	001116
MINEXP	002563	MINUS	001457	MUNE	002577
MW0	002621	NDEXP	002345	ONEEXP	002375
OUTPUT	005066	PL0EXP	002452	PLU	001464
PONE	002530	PTW	002532	PTW0	002514
PZER	002465	ROM	002655	RDYA	003044
RDYB	005056	HEAD1	002746	READ2	002752
READ3	002762	KED	001177	READA	001203
REDB	001207	REDY	003111	RESTOR	001413
SCPLV	002322	SHIFT	002110	SHIFT2	002416
SRATIO	002663	ST	001043	START	001052
STLEVA	001504	STOP	002676	STOP2	002100
STORE	001550	STORE1	002174	STORE2	002176
STR	001502	STR	003126	SUBT	003020
SWNLST	000001	SW4040	000001	TEMPST	001374
TIME	002134	TIMEA	002156	THANS	001402
TRATIO	002434	T0	000001	T1	000011
TIA1	000015	TIC0	000013	TIC0A1	000017
UN	000010	WAIT	003007	ZEND	001354
ZEROB	001431	ZERD2	002307		
, ABS,	011000				
	000000				
	000000				

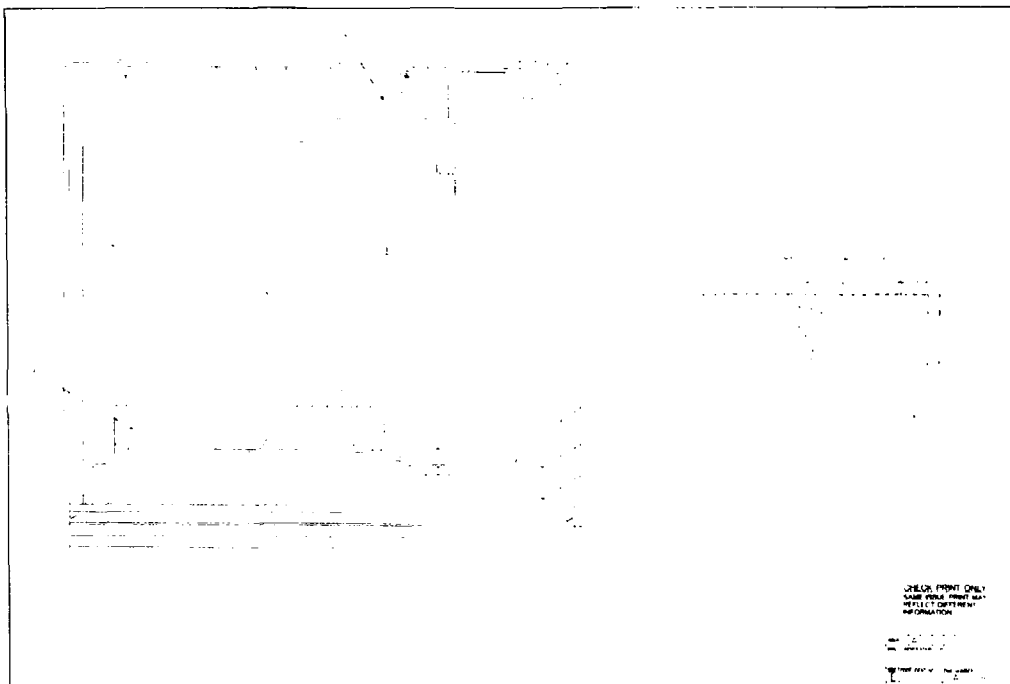
ERRORS DETECTED: 0
FREE CORE: 16192. WORDS

QUAD,LP: #MCS40,QUAD/NIME8

APPENDIX B

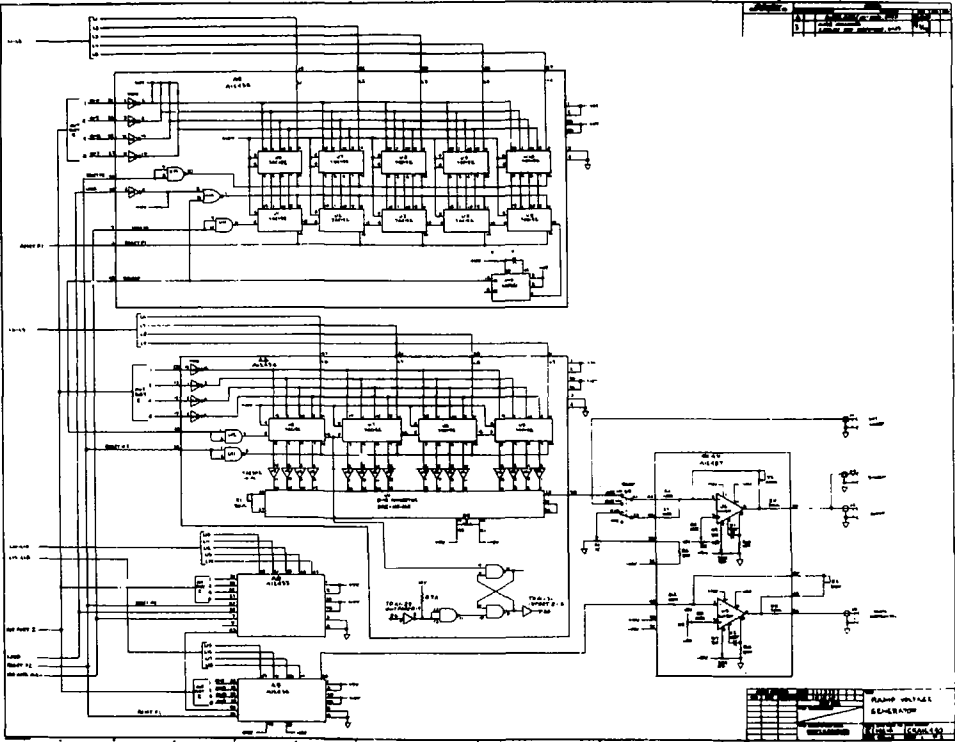
DETAILED SCHEMATIC, WIRING LIST, AND CHASSIS MECHANICAL DRAWINGS FOR THE RAMP GENERATOR

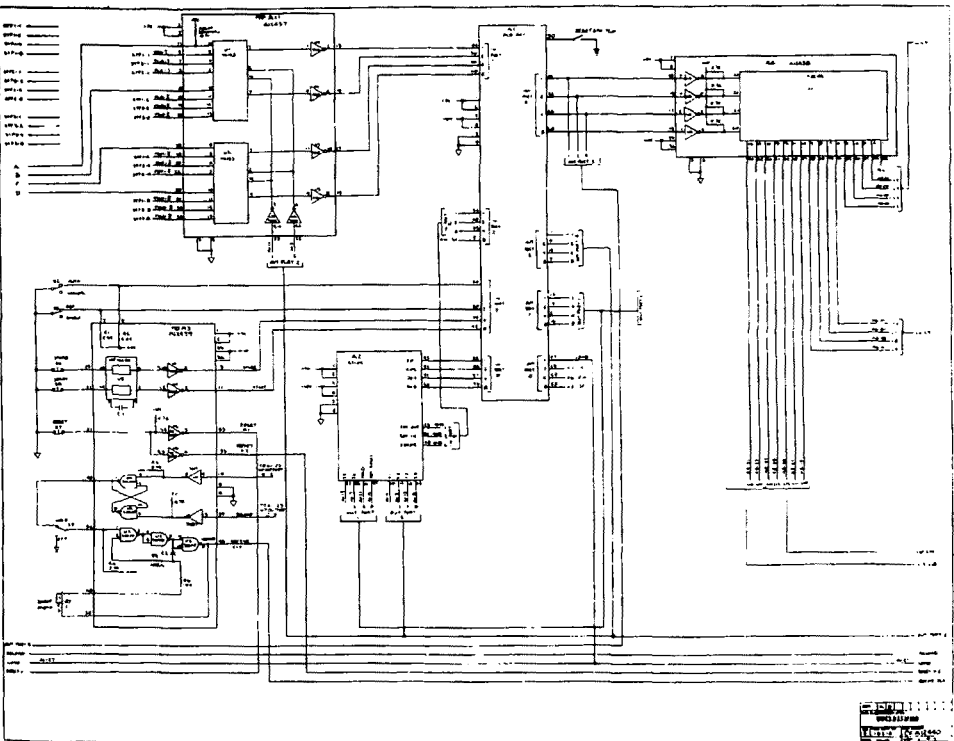




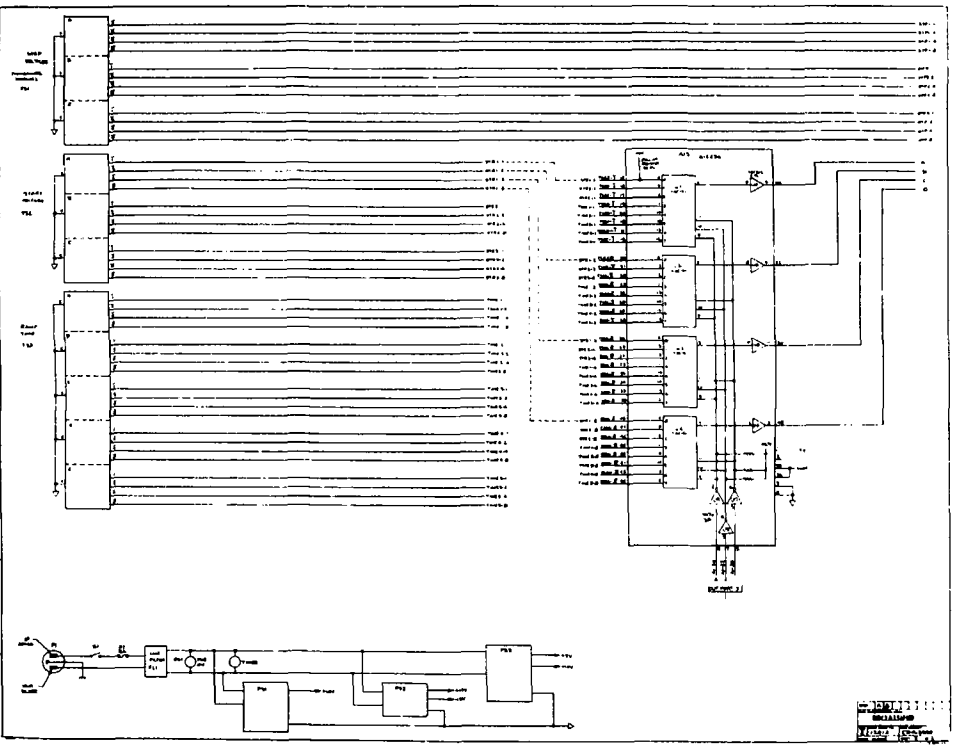
CHECK FRONT ONLY
 MAKE YOUR FIRST COPY
 REFLECT DIFFERENT
 INFORMATION

10/10/10
 10/10/10
 10/10/10





1. MOTOR
 2. SWITCH
 3. RELAY



100 KHZ
 211.0.0
 211.0.1
 211.0.2
 211.0.3
 211.0.4
 211.0.5
 211.0.6
 211.0.7
 211.0.8
 211.0.9
 211.0.10
 211.0.11
 211.0.12
 211.0.13
 211.0.14
 211.0.15

FROM		TO		TO		TO		TO		TO		TO		REF:			
	PIN		PIN		PIN		PIN		PIN		PIN		PIN		PIN		
2	XAI	44	XAI1	13											IN PORT 1	1	
3	▲	50	XAI1	15											▲	2	
4		54	XAI1	17											▼	4	
5	▼	40	XAI1	19											IN PORT 1	4	
6	XAI	12,62	XA2	1,2	XA3	1,2	XA4	1,2	XA5	1,2	X	1,2	XA8	1,2	XA9	1,2	GO TO LINE #7
7	XAI1	1,2	XAI3	1,2			PS 3	+5V									+5V
8	XAI	3,4	XA2	3,4	XA3	3,4	XA4	3,4	XA5	3,4	X	3,4	XA8	3,4	XA9	3,4	GO TO LINE #9
9	XAI1	3,4	XA3	3,4			GND		R1								GND
10	XAI	5,6	XA2	5,6	XA3	5,6	XAI1	2,9	PS 3	-10V R3							10V
11	▲	34	XA2	45													IMPORT 2
12		38	XA2	51													2
13		35	XA2	49													IMPORT 2
14		46	XA3	9	S2	N/C	[AUTO]										IMPORT 3
15		48	XA3	7	S3	N/C	[REP]										2
16		52	XA3	13													3
17		42	XA3	11,10,9													IMPORT 3
18		32	XA2	33													IMPORT 0
19		36	XA2	35													2
20		37	XA2	37													4
21		33	XA2	30													IMPORT 0
22		24	XA4	13	XAI3	5											EXPORT 3
23		22	XA4	15	XAI3	7											2
24	▼	26	XA4	17	XAI3	9											4
25	XAI	20	XA4	19													EXPORT 3
26																	
27																	
28																	

NOTES:

ASSEMBLY APPROVAL #		SHEET		TITLE	
OPD	DATE	INITIALS	MARK	RAMP VOLTAGE GENERATOR	
PART CLASSIFICATION				DRAWING NO.	
UNCLASSIFIED				14214	
DRAWING CLASSIFICATION LEVEL				DRAW NUMBER	
UNCLASSIFIED				WD-A12440	
SCALE				SHEET 1 OF 6	

	FROM	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	REF:	
	PIN		PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN		
2	XA1	11	XA2	10	XA5	31	XA6	23	XA8	31	XA4	23	XA11	33		OUT PORT 2 1	
3	↑	9	↑	14	↑	29	↑	29	↑	29	↑	13	XA11	25		2	
4		13		12	↓	25	↓	15	↓	25	↓	15				4	
5		7		28	XA5	27	XA6	19	XA8							OUT PORT 2 8	
6		19		22	XA3	6										OUT PORT 1	
7		17		26	XA3	10										2	
8		21	↓	16												4	
9	↓	15	XA2	47												OUT PORT 1 8	
10	XA1	27	XA5	33	XA8	33	XA14	6									
11																	
12	XA3	27	S4	0	*O	GND										STORE SW	
13	↑	31	S5	0	O											START SW	
14		29	S6	0	O											CALCULATE SW	
15		21	S7	0	C	GND										RESET SW	
16		43	S8	COM												HOLD/OFF SW	
17		54	S8	N C												HOLD/OFF SW	
18		48	R2	12												SWEEP WIDTH POT	
19		52	R2	3												SWEEP WIDTH POT	
20																	
21		33	XA5	5												RESET 1	
22		35	XA5	41	XA6	35	XA9	41	XA9	35						RESET 2	
23		39	XA5	43												RELOAD	
24		46	XA5	7	XA8	7										100 KHZ CLOCK	
25																	
26		8	XA9	25												L17	
27	↓	12	XA9	11												L18	
28	XA3	5556	XA4	5556	XA5	5556	XA9	5556	XA8	5556	XA8	5556	XA13	5556	XA14	5556	+ 10V P.S.I

NOTES

UNCLASSIFIED

B 14214 WD-A12440

	FROM		TO		TO		TO		REF:
		PIN		PIN		PIN		PIN	
1									
2	XA 4	30	XA 9	41					L16
3	↑	32	XA 9	47					L15
4		54	XA 8	47					L14
5		51	XA 8	45					L13
6		53	XA 8	35					L12
7		49	XA 8	21					L11
8		47	XA 8	19					L10
9		48	XA 6	11					L9
10		45	XA 6	23					L8
11		43	XA 6	41					L7
12		41	XA 6	47					L6
13		39	XA 5	47					L5
14		40	XA 5	45					L4
15		37	XA 5	35					L3
16	↓	35	XA 5	21					L2
17	XA 4	33	XA 5	19					L1
18									
19	XA 6	43							
20	↑	53	S9	N/C	INT				RAMP SA
21	↓	49	XA 9	49	XA 11	49	PS 2	+15V	+15V
22	XA 6	51	XA 9	51	XA 11	51	PS 2	-5V	-5V
23									
24									
25									
26									
27									
28									

NOTES:

DATE: 11/11/66
WD-A12440
 REV: 3 OF 6

	FROM	TO	TO	REF:
	PIN	PIN	PIN	
1				
2	XAI1	44 S9	COM1	RAMP SW
3	▲	46 S9	COM2	
4		39 RI	I	
5		48 XA9	53	RAMP SW
6		43 J2	C/C	J4 C/C SWEEP BNL
7		54 J3	C/C	SCOPE HORIZONTAL
8		11 XAI3	54	A
9		9 TSI A	T	STP 1 - 1
10		7 TSI B	T	STP 2 - 1
11		5 TSI C	T	STP 3 - 1
12		18 XAI3	52	B
13		16 TSI A	2	STP 1 - 2
14		14 TSI B	2	STP 2 - 2
15		20 TSI C	2	STP 3 - 2
16		28 XAI3	50	
17		26 TSI A	4	STP 1 4
18		24 TSI B	4	STP 2 4
19		22 TSI C	4	STP 3 4
20		30 XAI3	48	
21		31 TSI A	8	STP 1 8
22	▼	32 TSI B	8	STP 2 8
23	XAI1	3633 TSI C	8	STP 3 8
24			23	
25			1	
26				
27				
28				

NOTES:

WD A12440
4 of 6

	FROM	TO		REF:
	PIN		PIN	
1				
2	XAI3	14 TS2A	T	STR 1
3	▲	15 TS2B	T	STR2 1
4		17 TS2C	T	STR3 1
5		19 TS3A	T	TIME 1-1
6		20 TS3B	T	▲ 2-1
7		18 TS3C	T	3-1
8		11 TS3D	T	▼ 4-1
9		13 TS3E	T	TIME 5-1
10		23 TS2A	2	STR1 2
11		21 TS2B	2	STR2 2
12		24 TS2C	2	STR3 2
13		22 TS3A	2	TIME 1-2
14		32 TS3B	2	▲ 2-2
15		28 TS3C	2	3-2
16		25 TS3D	2	▼ 4-2
17		26 TS3E	2	TIME 5-2
18		36 TS2A	4	STR1 4
19		29 TS2B	4	STR2 4
20		27 TS2C	4	STR3 4
21		34 TS3A	4	TIME 1-4
22		37 TS3B	4	▲ 2-4
23		35 TS3C	4	3-4
24		33 TS3D	4	▼ 4-4
25		38 TS3E	4	TIME 5-4
26		45 TS2A	8	STR1 8
27	▼	47 TS2B	8	STR2 8
28	XAI3	42 TS2C	8	STR3 8

NOTES:

DWG NUMBER

WD-A12440

DATE 5 66

	FROM	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	TO	REF:		
	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN	PIN			
1																	
2	X A 13	40	TS 2A	B											TIME 1-B		
3	↑	39	TS 3B	B											2-A		
4	↓	41	TS 3C	B											3-B		
5		43	TS 3D	B											4-B		
6	X A 13	46	TS 3E	B											TIME 5-b		
7																	
8	TS 1A	C	TS 1B														
9	TS 3C	C	TS 3D	C	TS 3E	C	TS 2A	C	TS 2B	C	TS 2C	C	TS 3A	C	TS 3B	C	GO TO LINE #4
10	S 2	C	GND	C	TS 3E	C	GND										GND
11	S 3	C	GND														AUTO MANUAL SW
12	J 1	C/C	S 9	N/O 1	[FXT]												REP SINGLE SW
13	R 1	J	S 9	N/C 2													EXT SWEEP
14																	
15																	
16	P 1	B	S 1	C	F 1	FL 1	AC	DS 1		PS 1	AC	PS 2	AC	PS 3	AC		AC PWR , HOT
17	P 1	N	FL 1	AC	DS 1	PS 1	AC	PS 2	AC	PS 3	AC						AC PWR NEUT
18	P 1	GND	PS 1	-10V	PS 2	COM	PS 3	COM	GND								AC PWR , GND
19																	
20																	
21																	
22																	
23																	
24																	
25																	
26																	
27																	
28																	

NOTES: *TIMER

FORM	A								
UNCLASSIFIED									
NO	B	FORM NO.	14214	REV		ISS. DATE		ISS. NO.	WD-A12440
DATE		BY		CHKD		APP'D		CLASS	

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