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(72) Inventor DEREK COLMAN

(19)

(54) TRANSISTOR AND INTEGRATED CIRCUIT MANUFACTURE

(71) We, TEXAS INSTRUMENTS LIMITED, a British Company, of Manton Lane, Bedford, do hereby declare the invention, for which we pray that a patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to the manufacture of transistors and integrated circuits and is particularly, but not exclusively, of value in the manufacture of so-called integrated injection logic circuitry (I²L).

A well-known difficulty encountered in the manufacture of high speed switching transistors and bipolar integrated circuits is the phenomenon of minority carrier storage in base regions. In order to obtain satisfactory transistor action it is necessary for the semiconductor material of a base region to be such as to ensure that minority carriers injected into it through, for example, an emitter-base junction, have a long lifetime so that most of the carriers reach a collector-base junction. However, an effect of this long lifetime is that the carriers in the base region remain for a significant period of time after the end of injection of carriers into the region, and can cause conduction across the collector-base or emitter-base junction to continue until the carriers have been recombined or collected. This minority carrier storage shows itself in the slow turning off of a transistor after it has been in saturation.

It is an object of the present invention to overcome this difficulty at least partially.

According to one aspect of the present invention there is provided a method of reducing the minority carrier storage time of a bipolar transistor having emitter, base and collector regions, the base region consisting of an intrinsic part through which the minority carriers have substantially the shortest paths to pass from the emitter to the collector, and an extrinsic part forming the remainder of the base region, wherein at least the major part of the extrinsic part, and substantially none of any other part or region, is subjected to bombardment by ions or neutral atomic particles through a surface of the transistor, so as to reduce minority carrier lifetime in the extrinsic part.

Where the following description refers to ion bombardment it is to be understood that this term includes bombardment by neutral atomic particles.

The bombardment introduces recombination centres into the extrinsic region and thereby reduces minority carrier lifetime in that part of the base region. Thus the minority carriers which enter the extrinsic region, say from the emitter-base junction, which would otherwise contribute to the minority carrier storage, are recombined and the storage time is usefully reduced.

The invention is of particular value in an integrated injection logic type of structure which contains an inverted planar transistor (the substrate provides the emitter connection instead of the collector connection), because the base region of that transistor has a considerable extrinsic volume.

The ion bombardment is limited to the extrinsic region because damage in the vicinity of the junctions will result in increased leakage.

It is desirable not to let the temperature of a device during or after ion bombardment rise sufficiently to cause annealing of the bombarded material as the effect of the bombardment in producing recombination centres will be reduced.

The invention also provides a transistor or integrated circuit produced by a method as described above.

The use of ion bombardment to reduce minority carrier storage is applicable to any bipolar transistor structure in which there is a significant extrinsic base volume.

In order that the invention may be fully understood and readily carried into effect it will now be described in greater detail with reference to the single figure of the accompanying drawing, which shows in diagrammatic form the cross-section of an integrated injection logic circuit.

The circuit shown in the Figure has a silicon substrate 1 of N^+ type conductivity on which is deposited an epitaxial silicon layer 2 of N type conductivity. In the surface of the layer 2 two regions 3 and 4 of P type conductivity are produced by diffusion or ion implantation, for example, and in the region 4 a region 5 of N type conductivity is formed. The techniques used to fabricate the structure may differ in several ways from those referred to, and the alternatives possible will be known to those skilled in the art. The structure itself as thus far described is that proposed for an integrated injection logic circuit and consists of a lateral P-N-P transistor formed by the region 3, the layer 2 and the region 4, and an inverted N-P-N transistor formed by the layer 2, the region 4 and the region 5. The region 4 acts both as the collector of the P-N-P transistor and the base of the N-P-N transistor, with the result that carriers passing from the region 3 into the layer cause carriers to be injected into the region 4 from the layer 2 which carriers in turn can produce by transistor action a flow of carriers from the region 4 to the region 5. In most cases more than one collector region 5 would be provided to give fan out.

The region 4 has an intrinsic part 6 where carriers entering the region 4 from the layer 2 have the shortest distance to travel to reach the junction between the region 4 and the region 5 and therefore contribute most to the transistor action. The region 4 also has an extrinsic part 7 which is the part of the region other than the part 6, and carriers entering the part 7 contribute little to the transistor action.

Contacts 8, 9 and 10 are also shown in the Figure and provide ohmic connections respectively to the region 3, the region 4 and the region 5.

In accordance with one example of the invention the extrinsic part 7 of the region 4 is subjected to bombardment by an ion beam 11 so as to damage the crystal structure and introduce defects which act as recombination centres to reduce the lifetime of minority carriers in the part 7. It has been found possible to obtain differing amounts of damage and to vary the depth of the damage by altering the bombardment dose and its energy. The restriction of the area of the surface which is bombarded may be achieved by depositing a film of aluminium on the surface and then etching away the part of the film covering the part of the surface to be bombarded.

In a specific example an integrated injection logic circuit similar to that shown in the Figure was bombarded with boron ions at 200 keV through a base oxide layer of 0.45 microns thickness and its performance was then compared with that of an untreated circuit. The switching time of an untreated circuit was 30 ns for a 3-collector structure and 20 ns for a single collector structure. The switching time of a bombarded circuit was 10.5 ns for a 3-collector structure and 8 ns for a single collector structure. The actual implantation dose resulting from the bombardment was 10^{15} ions per square cm.

It was found that prolongation of the bombardment resulted in a slight slowing down of the switching speed compared with the highest speed achieved and this is thought to be due to annealing of the damaged crystal structure resulting from the heating caused by the bombardment. A certain amount of annealing is likely to occur in any case because of the heating in subsequent processing of the circuit following the bombardment; but it is believed to be desirable that such annealing should be kept to a minimum.

As a consequence of the bombardment it is possible that leakage current across the junctions of the circuit will tend to increase due to some of the implanted ions reaching the junction. In addition the junction breakdown voltage may be reduced. In some examples the leakage current increased from 10^{-14} to from 10^{-11} to 10^{-7} amps. However, such an increase in leakage current could probably be tolerated because, generally speaking, high speed circuits tend to use high currents and low speed circuits low currents. Therefore the increase in leakage current is matched by an increase in operating current because of the high speed nature of the circuit. Low speed circuits operating at low current would not need to be bombarded. Any reduction in junction breakdown voltage would probably not be of significance because high breakdown voltages are usually required only at input and output interfaces of an integrated circuit where a lower operating speed could possibly be tolerated.

Although boron has been referred to above as the material of the ions, other materials could be used such as, for example, hydrogen which has the advantage of being the lightest ion and consequently has the deepest penetration for a given energy. Whereas heavier ions produce more damage for a given dose than lighter ions, such damage is concentrated near the surface, whereas the lighter ions penetrate more deeply into the material being bombarded

for the same energy. As stated above the amount of damage resulting from a bombardment depends on its dose, although it is important to avoid the annealing due to the heating of a heavy dose. The ion, energy and dose may be chosen to provide the damage required. Neutral particles may be used instead of ions but they are less convenient to form into a beam.

An aluminium film was referred to above as being suitable to form a mask delineating the area or areas to be bombarded. In one example a film thickness of 1.4 microns was found to be satisfactory. Any other material having suitable ion-stopping ability may be used.

The bombardment may be carried out through an oxide film as described, the film serving to protect the surface of the circuit. If desired, however, the bombardment could be applied directly to the surface of the circuit.

The method of the invention is applicable to transistors and integrated circuits other than integrated injection logic circuits with respect to which it has been described. It is necessary that transistors and integrated circuits to be suitable for treatment should have significant amounts of extrinsic base region. It is desirable that the extrinsic parts should be able to be bombarded without bombardment of a junction.

WHAT WE CLAIM IS:—

1. A method of reducing the minority carrier storage time of a bipolar transistor having emitter, base and collector regions, the base region consisting of an intrinsic part through which the minority carriers have substantially the shortest paths to pass from the emitter to the collector, and an extrinsic part forming the remainder of the base region, wherein at least the major part of the extrinsic part, and substantially none of any other part or region, is subjected to bombardment by ions or neutral atomic particles through a surface of the transistor, so as to reduce minority carrier lifetime in the extrinsic part.

2. A method according to claim 1 including forming a mask of an ion stopping material over the surface of the transistor, the mask having a window or windows exposing only the extrinsic base region to bombardment.

3. A method according to claim 1 or 2 wherein the surface is covered by a film of oxide during bombardment.

4. A method according to any of claims 1 to 3 wherein the bombardment is of boron ions or hydrogen ions.

5. A method according to any preceding claim wherein the transistor is included in an integrated circuit.

6. A method according to claim 5 wherein the integrated circuit is an integrated injection logic circuit.

7. A method of reducing the minority carrier storage time of a bipolar transistor substantially as herein described with reference to the single Figure of the accompanying drawing.

8. A transistor or integrated circuit treated by a method according to any preceding claim.

9. An integrated injection logic circuit treated by a method according to any of claims 1 to 7.

ABEL & IMRAY,
Chartered Patent Agents,
Northumberland House,
303-306 High Holborn,
London, WC1V 7LH.

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