PATENT SPECIFICATION (11) 1 548 128

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(21) Application No. 6377/78 (22) Filed 17 Feb. 1978

(31) Convention Application No. 783245 (32) Filed 31 Mar. 1977 in

(33) United States of America (US)

(44) Complete Specification Published 4 Jul. 1979

(51) INT. CL.² H01L 21/04 21/265 29/70

(52) Index at Acceptance
H1K 11B1 11B4 11D3 11D 2S1B 2S20 2S2D 2S2P 3E5A 3T1C 3T2 5B2 5C3A 5C3G 9B1 9B1A 9N2 9N3

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(54) SEMICONDUCTOR INTEGRATED CIRCUITS

(71) We, INTERNATIONAL BUSINESS MACHINES CORPORATION, a Corporation organized and existing under the laws of the State of New York in the United States of America, of Armonk, New York 10504, United States of America do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The present invention relates to a method of making semiconductor integrated circuits.

For the last decade, planar, vertical bipolar transistor integrated circuits have been produced predominantly by a conventional epitaxial deposition method which first involves the formation in a substrate of a highly doped surface region which in the final device usually functions as a low resistance subcollector. Then, an epitaxial layer of silicon is deposited on the such a silicon substrate and base and emitter regions are formed in this epitaxial layer by the subsequent introduction of impurities by either diffusion or ion implantation. Although it has been recognized that from a processing viewpoint it would have been desirable to form the collector, base and emitter of such bipolar devices directly in the substrate without an epitaxial layer, the problem which moved the art in the direction of epitaxial methods was that devices formed by the direct introduction of collector, base and emitter regions into the substrate did not exhibit a relatively low resistance path from the collector terminal down to the collector base junction. Since the epitaxial approach permitted the formation of a heavily doped, low resistance subcollector which ensured such low resistance collector terminal path, the art predominantly used epitaxial techniques in forming vertical bipolar integrated circuitry, particularly in the high performance integrated circuitry, particularly in the high performance integrated circuitry required in highspeed digital computers.

While the bipolar integrated circuit art did find some limited usage for non-epitaxial or "epi-less" structures, i.e. structures formed by the triple diffusion of collector, base and emitter directly into a substrate, such structures were never considered to be feasible for high speed, high performance integrated circuits.

With the development of ion implantation methods of forming non-epitaxial integrated circuits were evolved which involved forming the collector region by ion implantation followed by the formation of base and emitter regions in the conventional manner. In such methods, the collector dopant or impurity was introduced at the surface of the silicon substrate and then distributed or driven deeper into the substrate by a thermal distribution diffusion heating cycle. Such a method is described in the article, "Improved Triple Diffusion Means Densest ICs Yet", J. Buie, *Electronics*, August 7, 1975, pp. 101-106. While such an ion implantation step solved one of the problems of the wholly diffused collector, i.e. more uniform and consistent impurity distribution in the collector, it did not offer a solution to the above mentioned problem of providing the low resistance collector path required in high-performance integrated circuitry.

Other ion implanted collector techniques, e.g. "Self-Isolating Bathtub Collector for a Planar Transistor", J.E. Ziegler et al, *IBM Technical Disclosure Bulletin*, Vol. 14, No. 5, October 1971, pp. 1635 - 1636, involved the formation of a highly doped, low resistivity collector by a high energy ion implantation step. However, in order to carry out such a high energy ion implantation step using the disclosed surface masking techniques a very thick layer of ion blocking masking material, about three to four microns in thickness, had to be used in order

to prevent the penetration of the ions into the masked areas of the silicon substrate. For example, when using a silicon dioxide mask, its thickness must be about four microns in order to prevent the penetration of the high energy ions. With such thick masks, it is very difficult to achieve sharp mask edge definition, since the mask edge would be sloped. With such a sloped mask edge, the high energy ions will penetrate to varying degrees into the substrate through the mask edge depending on the thickness of the sloped edge at a particular penetration point, thus producing an undesirable sloped PN collector base junction extending from the surface into the substrate. This sloped collector-base junction has a significantly greater slope than collector-base junctions of transistors produced by conventional epitaxial methods. As a result, there is an undesirable increase in lateral collector base junction capacitances which will tend to slow down the operation of the device.

While the problems associated with the production of a non-epitaxial planar vertical bipolar integrated circuit have been described with respect to standard transistors wherein the emitter region is uppermost, very similar problems are encountered in the production of non-epitaxial bipolar integrated circuits using inverted transistors, i.e., transistors wherein the collector region is uppermost and the emitter is lowermost. For example, when non-epitaxial methods are used to form such inverted transistors, there is a similar problem with respect to providing a high doping level in the lowermost emitter region.

Accordingly, it is an object of the present invention to provide an improved method involving ion implantation to form non-epitaxial semiconductor integrated circuits.

Accordingly, the present invention provides a method of forming a semiconductor integrated circuit comprising forming in a silicon dioxide region extending into the substrate from the surface thereof and laterally enclosing a portion of the silicon substrate, directing a beam of ions of opposite conductivity type impurity at the substrate at an energy and dosage level sufficient to form a first region of opposite conductivity type within and laterally defined by the recessed silicon dioxide region, the opposite conductivity type impurity having a concentration peak below the surface of the substrate, forming a region of the one conductivity type which extends from the substrate surface into the first opposite conductivity type region to a depth between the concentration peak and the surface, and forming a second region of opposite conductivity type extending from the substrate surface into the region of one conductivity type to a depth less than the depth of the latter region.

Preferably, the beam of ions of opposite-type conductivity impurity used to form the first region is a high-energy beam having an energy level of at least one MeV, and the concentration peak is at least one micron below the surface. It is also desirable that the energy and dosage levels of the beam are selected so that the opposite-type conductivity impurity in the first region has a more gradual concentration gradient between the peak and the substrate surface than between the peak and the junction of the first region with the substrate.

The method of the present invention may be used for the production of vertical bipolar integrated circuits wherein said first opposite type conductivity region will function as a collector as well as for the fabrication of integrated circuits with inverted bipolar devices wherein the first opposite-type conductivity region will function as a "buried" emitter region.

An embodiment of the invention will now be described with reference to the accompanying drawings, in which:

FIGS. 1A-1E are diagrammatic enlarged fragmentary cross-sectional views of a portion of an integrated circuit illustrating the steps involved in the formation of an embodiment of a vertical bipolar transistor made in accordance with the present invention; and

FIG. 2 is an enlarged cross-sectional view of the bipolar vertical transistor of FIGURE 1E with a graph showing the impurity distribution.

Referring first to FIG. 1A, regions of recessed silicon dioxide such as that shown at 11 are formed in a silicon substrate which is P- and has a resistivity of about 10 ohm-cm. Recessed silicon dioxide regions 11, each of which laterally encloses a portion of the substrate 10, extend into substrate 10 by about 5 microns. The recessed silicon dioxide regions may be formed by any of a number of conventional techniques for forming silicon dioxide regions embedded in a silicon substrate. Preferably, they are formed by techniques which involve the oxidation of the silicon substrate in these regions to form the silicon dioxide. Because it is desirable that the sidewalls of recessed silicon dioxide regions 11 be as vertical as possible, these regions are most preferably formed by a method which involves first rendering porous these portions of the silicon substrate which are to be converted into silicon dioxide regions 11 followed by selectively oxidizing the porous silicon portions to silicon dioxide, such methods are described in U.S. Patents 3,640,806 and 3,919,060. In accordance with the methods described in these U.S. patents, the portions of the silicon substrate to be converted to regions 11 is first heavily doped

to a P+ level by the introduction of an impurity such as boron to a surface concentration (C_0) of about 2×10^{20} atoms/cm^3, followed by anodically etching the substrate to selectively convert the P+ regions to porous silicon. Then, the porous silicon is converted into silicon dioxide under conditions wherein the porous silicon is selectively oxidized.

Of course, any other conventional method for forming recessed silicon dioxide may be alternatively used, e.g. the method of U.S. Patent 3,858,231 which involves etching recesses in the substrate and then subsequently thermally oxidizing to form silicon dioxide in such recesses. Also, if substantially vertical walls are desired, with the etch and thermal oxidation technique described in the last mentioned U.S. patent, then the recesses etched in the silicon may be formed by the vertical-walled etching technique described in the article entitled, "The Etching of Deep Vertical-Walled Patterns in Silicon", A.I. Stoller, *RCA Review*, June 1970, pp. 271-275. The recessed silicon dioxide region may also be formed by a combination of reactive ion etching using sputter-etching to form relatively narrow deep trenches in the silicon followed by depositing silicon dioxide in the trenches.

Next, FIG. 1B, the surface of the substrate is subjected to a blanket (non-selective) ion implantation of phosphorus ions at an energy level of 2.5 MeV and a dosage of 3×10^{15} cm^{-2}. The ion implantation is carried out using standard techniques for making high energy ion implantations at energy levels in excess of 1 MeV as described, for example, in the article, "Experimental Evaluation of High Energy Ion Implantation Gradients for Possible Fabrication of a Transistor Pedestal Collector", J.F. Ziegler, et al, IBM Journal of Research and Development, Vol. 15, No. 6, November 1971.

Such high energy ion implantations may be accomplished using conventional ion implantation equipment as described for example, in U.S. Patent 3,756,862, except that as set forth in the Ziegler et al article the accelerator used must be one capable of providing a high energy beam and the accelerator stage is carried out prior to the mass analysis in the conventional manner. This ion implantation step produces an N-type region 12, which is laterally defined and enclosed by the recessed silicon dioxide region 11, which together with junction 13 electrically isolates region 12. When the ion implantation is carried out under the conditions described above, region 12 will have the impurity distribution profile, shown in the graph of FIG. 2. Region 12, which will function as the collector region in a vertical bipolar transistor, includes a highly doped N+ buried region 14, about two microns below the substrate surface and having a peak concentration, of at least 10^{18} atoms/cm^3, and preferably 10^{20} atoms/cm^3, as in the present example.

In addition, in order to reduce the possibility of inversion at the surface of collector region 12, it is desirable that the impurity distribution profile of region 12, be such that the N-type impurity have a surface concentration (C_0) of at least 10^{15} atoms/cm^3, as indicated in FIG. 2. The distribution of the high energy implanted impurities consists of a main Gaussian peak and an exponential tail extending to the surface of the wafer. The concentration level of this exponential tail depends upon the dose and energy of the N-type impurity implant. When the ion implantation is carried out, at the energy and dosage level described above, the impurity distribution profile, of region 12 will have a "tail portion" 15 as the surface is approached, which ensures a C_0 of at least 10^{15} atoms/cm^3. In this tail portion of the impurity distribution profile, the distribution gradient becomes more gradual as the surface is approached.

When using the conventional phosphene source for the phosphorus ion in the present implantation, modification of the gradient of the exponential tail region can be achieved through adjustment of the phosphene ion source. By increase of the concentration of singly charged tetramers $(^{31}P)_4^+$ in the ion source, phosphorus ions with energies equal to one-fourth of the accelerating potential (i.e., the tetramers) as well as those with energies equal to the full accelerating potential (i.e., $^{31}P^+$) are implanted into the silicon wafer. The lower energy phosphorus ions produce a shoulder which elevates "tail" 15 (FIG. 2) on the surface side of the main Gaussian peak 29; this increases the concentration of phosphorus impurity at the substrate surface (C_0). Of course, the formation of these lower energy tetramers $(^{31}P)_4^+$ will occur only when the mass analysis is carried out so as to pass the $^{31}P^+$ species of ion and then remove the other species such as $^{32}(PH)^+$. Also, when desirable, by adjustment of the analyzing magnet of the ion implantation apparatus to produce a beam of the phosphorus ion species $^{32}(PH)^+$ available from the phosphene source, thereby removing the $^{31}P^+$ species and consequently the lower energy tetramers thereof, the shoulder elevation of tail portion 15 can be eliminated.

In any event, where the $^{31}P^+$ species is used, the level of the shoulder of tail portion 15 and thus C_0 may be controlled by controlling the source to vary the tendency toward tetramer formation, e.g. increased pressure on the source favours tetramer formation.

It should be noted that the profile, shown

in FIG. 2, for N region 12, represents the distribution after a conventional anneal cycle carried out at a temperature in the order of 1000°C for about 60 minutes. This anneal cycle is carried out after the last region, the emitter is formed.

The collector region 12 may be formed by implanting directly onto the substrate or, as shown in FIG. 1B, through a thin layer 16 of insulating material such as silicon dioxide about 1000 A thick. This layer may be formed by any conventional technique such as sputter deposition, chemical vapor deposition or preferably by thermal oxidation. While in the present example, conditions have been given for achieving N regions with impurity distribution profiles having a peak at about two microns below the surface, the method may be used to produce implanted regions with varying distribution profiles, and advantageously to produce regions with an impurity distribution with a peak concentration at a distance of 1 micron and greater from the surface.

For example, with an ion dosage of about 10^{15} cm^{-2} from a conventional phosphorus source, and an anneal cycle of 30 minutes at 1000°C an energy level of 1 MeV will provide impurity distribution profile with a peak concentration of 10^{19} atoms/cm^3 at a distance of about 1 micron from the surface while an energy level of 3 MeV will produce a distribution profile with a peak at about 2.4 microns from the surface. In both cases the ion implantation may be carried out through a thin silicon dioxide (1000A) screen which may be provided by subjecting the substrate surface to a conventional thermal oxidation prior to the implantation step.

After the formation of collector region 12, the vertical bipolar integrated circuit may be completed by forming base, emitter, collector contact and (if desired) resistor regions by conventional integrated circuit fabrication techniques such as those described in U.S. Patent 3,539,876. In addition, conventional insulative layers, metallic contacts and circuit interconnection metallurgy may also be provided in accordance with the techniques described in U.S. Patent 3,539,876. Alternatively, to the diffusion techniques described in U.S. Patent 3,539,876 for the formation of emitter, base and resistor regions, conventional ion implantation techniques may also be used for the formation of these regions. Conventionally, these are not the high energy techniques described above but rather low to moderate energy ion implantation which may be practised on conventional equipment as that described in U.S. Patent 3,756,862.

In the present embodiment, emitter and base region are formed by ion implantation techniques. With reference to FIGURE 1C, the layer of silicon dioxide 16 remains intact, and an ion implantation blocking mask 17 is formed. This mask may conveniently be a photoresist type of blocking mask formed in accordance with the method of U.S. Patent 3,920,483. The photoresist mask preferably has a thickness of about 1.5 microns. The photoresist mask 17 will define one edge of the base region to be ion implanted while the other edge will abut and be defined by the recessed silicon dioxide region 11. P region 18 which will serve as the base region is ion implanted from a boron source using the conventional equipment described in U.S. Patent 3,756,862 at room temperature preferably in two steps: 50 KeV and dosage of 1 x 10^{14} ions/cm^2 followed by 150 KeV and dosage of 3 x 10^{13} ions/cm^2. P. region 18 will have an impurity concentration profile as shown in the graph of FIG. 2 after the final post emitter anneal cycle.

Next, FIG. 1D, using conventional photolithographic etching techniques, emitter, base electrode and collector contact region openings 19, 20 and 21 are respectively opened in silicon dioxide layer 16, after which base electrode opening 20 is masked with an ion implantation blocking material such as photoresist layer 22 which may be formed in the manner described above, and a very low energy ion implantation is carried out at an energy level of 40 KeV and dosage level of 1 x 10^{16} ions/cm^2 of arsenic ions to form emitter region 23 and collector contact region 24. While the collector contact region may be formed as described above, it may be desirable to form the collector contact region 24 as a complete conventional "reach-through" to low resistance buried collector region 14. This may be accomplished by carrying out a preliminary implant into contact region 24 prior to this arsenic implant. This preliminary implant may be conveniently carried out either before or after the formation of base region 18. This implant is preferably of an N type material such as phosphorus which has a greater diffusivity rate than arsenic. For example, it may consist of a conventional phosphorus implant at an energy level of 150 KeV and a dosage of 5 x 10^{15} cm^{-2}. The energy level is insufficient to penetrate through silicon dioxide layer 16. Photoresist layer 22 is now removed and the structure is subjected to the anneal cycle for about 60 minutes at a temperature of about 1000°C after which emitter region 23 has the impurity distribution profile shown in FIG. 2.

Finally, using the conventional integrated circuit fabrication techniques described in U.S. Patent 3,539,876, metal emitter electrode 25, base electrode 26 and collector electrode 27 are formed. Electrodes 25, 26 and 27 are connected to an form part of a metallization pattern (not shown) formed on layer 16 which interconnects the devices in

the integrated circuit. The resulting final structure is shown in FIGURE 1E and enlarged in FIG. 2. While the specific example has been described with respect to an NPN-type vertical transistor, it will be obvious that pNP transistors, a P type impurity such as boron will be used to form the region with the buried high concentration portion. When an impurity such as boron which has a greater diffusivity rate than that of phosphorus is used to form the buried high concentration region, lower implantation energies in the order of 500 KeV may be used to form a buried region with a peak concentration at least 1 micron below the surface. In addition, the method of the present invention may be used to fabricate inverted transistors wherein the lowermost region such as region 12 serves as the emitter region and the uppermost region such as region 23 serves as the collector region. In the operation of the transistors fabricated in accordance with the present invention in either the conventional or inverted transistor mode, suitable voltage levels would be applied to contact regions 25, 26 and 27 to permit the transistor to operate in the selected mode.

WHAT WE CLAIM IS:-

1. A method of forming a semiconductor integrated circuit comprising forming a silicon substrate of one conductivity type a recessed silicon dioxide region extending into the substrate from the surface thereof and laterally enclosing a portion of the silicon substrate, directing a beam of ions of opposite conductivity type impurity at the substrate at an energy and dosage level sufficient to form a first region of opposite conductivity type within and laterally defined by the recessed silicon dioxide region, the opposite conductivity type impurity having a concentration peak below the surface of the substrate, forming a region of the one conductivity type which extends from the substrate surface into the first opposite conductivity type region to a depth between the concentration peak and the surface, and forming a second region of opposite conductivity type extending from the substrate surface into the region of one conductivity type to a depth less than the depth of the latter region.

2. The method of claim 1, wherein the concentration peak is at least one micron below the substrate surface.

3. The method of claim 2, wherein the beam energy is at least 1 MeV.

4. The method of claim 3, wherein the energy and dosage level of the beam of ions are selected so that the opposite conductivity type impurity has a more gradual concentration gradient between the peak and the substrate surface than between the peak and the junction of the first region with the underlying portion of the substrate.

5. The method of claim 4, wherein the opposite conductivity type impurity has a surface concentration of at least 10^{15} atoms/cm^3 in the completed integrated circuit.

6. The method of claim 5, wherein the peak has an impurity concentration of at least 10^{18} atoms/cm^3 in the completed integrated circuit.

7. The method of any preceding claim, wherein the recessed silicon dioxide region is formed by first converting corresponding silicon substrate regions to porous silicon and then oxidizing the porous silicon to silicon dioxide.

8. The method of claim 1, substantially as described with reference to the accompanying drawings.

9. A semiconductor integrated circuit made by the method claimed in any preceding claim.

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Chartered Patent Agent

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1979.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from
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2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

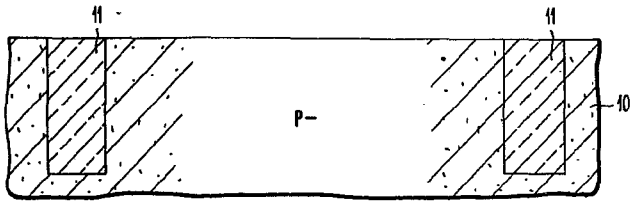

FIG. 1A

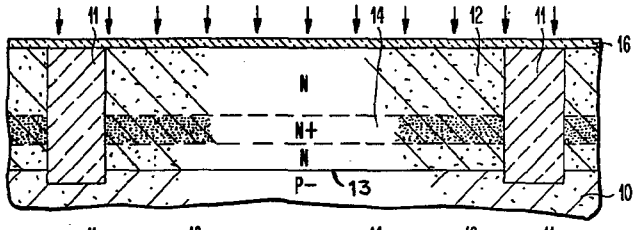

FIG. 1B

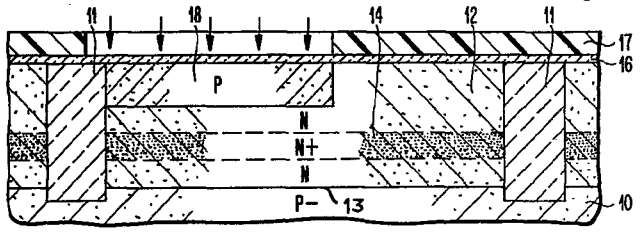

FIG. 1C

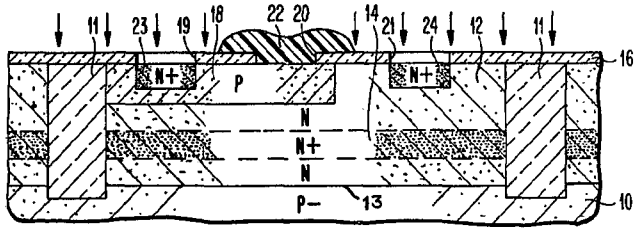

FIG. 1D

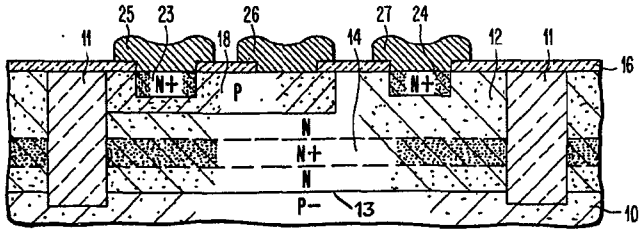

FIG. 1E

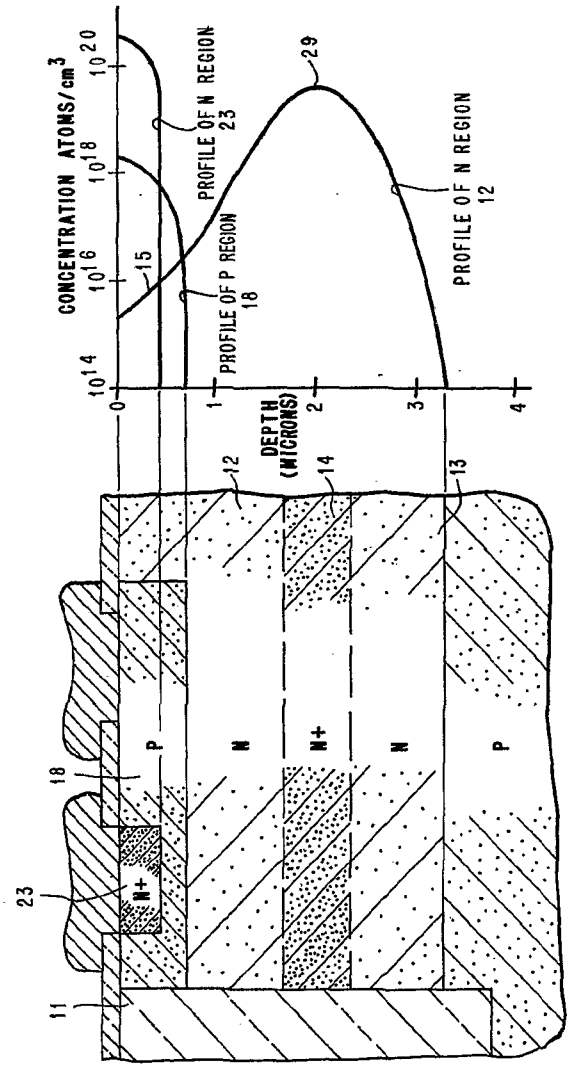
CONCENTRATION ATOMS/cm3
10 20
10 18
10 16
10 14
PROFILE OF N REGION 23
PROFILE OF P REGION 18
PROFILE OF N REGION 12
29
15
0
1
2
3
4
DEPTH (MICRONS)
12
14
13
P
N
N+
N
P
18
23
N+
11

FIG. 2