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SAR* : A FAST COMPUTER FOR CAMAC DATA ACQUISITION

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INTRODUCTION

This paper describes a special data acquisition and processing facility developed for Nuclear Physics experiments at intermediate energy installed at SATURNE (France) and at CERN (Geneva, Switzerland).

Previously, we used a PDP 11/45 computer which was connected to the experiments through a Camac Branch highway. In a typical experiment (340 words per event), the computer limited the data acquisition rate at 4 µsec for each 16-bit transfer and the on-line data reduction at 20 events per second only. The initial goal of this project was to increase these two performances.

Previous known acquisition processors were limited by the memory capacity these systems could support. Most of the time the data reduction was done on the host mini computer. Higher memory size can be designed with new fast RAM (Intel 2147) and the data processing can now take place on the front end processor.

WORKING ENVIRONMENT

Each nuclear experiment needs its own processing unit for experimental set-up, on-line data acquisition and off-line data reduction. But several satellite computers can share common resources (large mass memories, tape units, card reader, fast line printers,...) available on our PDP 11/45.

This host computer will be the central node of a multi-processor network. Up to six SAR will be connected to it during this year. Programs are loaded into SAR memory at a rate of 1 megabaud through a Camac serial link. SAR software development (edition, assembling, compilation) is done on the PDP 11 operated by a multi-console system.

HARDWAVE ARCHITECTURE

The computer is realized in a 19" × 6U crate with a separated power supply. The crate contains 26 slots which are interconnected through a 140 lines bus : 32 lines for data path, 20 lines for data address,32 lines for instructions, 18 lines for program address, etc... This modular design allows easy module replacement and installation of future specific operators. All signals are transmitted to the bus through a 74S240 line receiver driver.

The system, with one program memory block and one data memory block, occupies 16 slots.

The Program memory is loaded with the 32 bit long instructions divided in several fields :

- Return bit = 1 bit
- Interrupt inhibition bit = 1 bit
- Operation code = 4 bits
- Data source address = 5 bits
- Index bit = 1 bit
- Address = 20 bits

The address field defines

- either a program or data memory address = 18/20 bits
- either a CAMAC (F,B,C,N,A) address = 20 bits
- either a AMD 2901 micro-instruction = 18 bits

Each memory block needs 4 slots and has a capacity of 32k - 32 bit words.

The resident monitor is stored in one permanent memory card which occupies 1 slot, with a capacity of 2k - 32 bit words.

The Data memory is an independent unit and is organized in 8-bit bytes. Specific read/write instructions enable to access characters (8 bits), half-words (16 bits) or words (32 bits).

Each memory block needs 4 slots and has a capacity of 32k - 32 bit words.

The Arithmetic Logic Unit, which occupies 1 slot, uses 8 AMD 2901 4-bit slices and performs the full instruction set at a rate of 5 megacycles.

The index unit (1 slot) contains the index register and calculates the effective working address from the address field of the instruction according to the index bit state and the working data type defined by the operation code.

The sequencer (1 slot) generates the next instruction address and stores the return address in a 256-levels stack if necessary.

A fast multiplier performs 16 * 16 bit multiplications in less than 2 cycles.

INPUT - OUTPUT

The operator console is a RS-232 alphanumeric display directly connected to the SAR.

From this console managed by the resident monitor, the operator can

- examine or deposit 1) data in the Data memory or ; 2) instructions in the Program memory
- load programs from the PDP 11 into SAR memory
- hald or start programs.

The console interface and the fas. multiplier share one slot.

Several Branch highways can be connected to the processor. Each branch interface needs 1 slot.

A Camac transfer is activated by a single SAR instruction (200 ns). The data take is limited by the Branch highway cycle only (∿ 1.4 µs). This dead-time can be used for processing data or for preparing the next transfer.

Any LAM request can take control of the processor when all higher priority requests are served. A 3 µs elapsed time is necessary before starting the specific interrupt routine.

The Camac module priority is software determined.

PROGRAM SUSPENSION

External signals can suspend the execution of a program by forcing instructions on the bus.

Ten hierarchized levels have been designed, allowing any peripheral to take control of the computer.

Interrupt subroutines are started by forcing a CALL instruction.

Direct memory access is done by forcing a READ or WRITE instruction.

All Camac requests use one suspension level.

SOFTWARE

The SAR resident monitor is stored in a 2K PROM and allows one user to work in a multi-task environment.

Software development is completely done with the PDP 11. Edition is using the DEC EDIT program. An assembler and a Fortran compiler have been written and generate the proper object code used by the SAR.

SAR Programs LOADER is full-part of the resident monitor and generates the memory image of the program by linking the different routines used.

RESULTS

The data acquisition rate is now limited by the CAMAC branch at 1.4 µsec for each transfer instead of 4 µsec with the PDP 11/45. The SAR can process data five times faster than PDP 11/45 with MOS memory.