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## HIGH TEMPERATURE, RADIATION HARDENED ELECTRONICS FOR APPLICATION TO NUCLEAR POWER PLANTS

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## I. Introduction

Electronic circuits have been developed and built at Sandia for many aerospace and energy systems applications. Among recent developments have been high temperature electronics for geothermal well logging and radiation hardened electronics for a variety of aerospace applications. Sandia has also been active in technology transfer to commercial industry in both of these areas.

## II. High Temperature Electronics

### A. Overview

The current state-of-the-art in high temperature electronics is summarized in Table I.[1] Military electronics are usually capable of operation up to 125°C. Above this temperature components fail because they have low melting points or are subject to chemical attack or decomposition. Commercial, high-temperature electronics have been available for the last one or two years but normally are restricted to the temperature range between 175°C and 225°C.

Sandia has done extensive work in developing electronics capable of operation in the temperature range of 275°C to 300°C for application to geothermal well logging.[2] This temperature range is at the upper limit of conventional silicon devices. The high temperature circuits built at Sandia have employed commercial JFETs and specially designed CMOS devices manufactured

in Sandia's Semiconductor Processing Laboratory.[3,4] An extensive survey of commercial active devices did not yield acceptable alternatives.

Standard silicon devices are not capable of operating in the next temperature regime shown in Table I, 350°C - 450°C. It is expected that III-V Compound transistors would be required for this temperature region, e.g., gallium arsenide technology. Industrial development of III-V Compound semiconductors has been for applications other than high temperature; alternative metalizations, passivations and device design are required for high temperature application. Sandia has a limited exploratory development program in this temperature range; however, it is expected that such technology will be available in four years. The delayed time scale is predicted due to the construction of critical laboratory facilities which will be available in about three years. Acceleration of laboratory construction activities could result in this technology being available within two years.

Semiconductor technology is less likely to be applicable above 500°C. Two alternatives are potentially available, magnetic circuits[5] and integrated thermionic devices. Magnetic circuits are not adaptable to miniaturization whereas integrated thermionic devices are at this time being studied at Los Alamos Scientific Laboratory.

Table I: Temperature Regimes for High Temperature Electronics

| UPPER TEMPERATURE LIMIT | APPLICATIONS | COMMENTS |
|---|---|---|
| 125°C<br>257°F | • STANDARD MILITARY SPECIFICATION | |
| 175 - 225°C<br>347 - 437°F | • HOT OIL AND GAS WELL LOGGING<br>• LOW TEMPERATURE GEOTHERMAL | • USES SELECTED 125°C ELECTRONICS |
| 275 - 300°C<br>527 - 572°F | • GEOTHERMAL<br>• JET ENGINES | • UPPER LIMIT OF CONVENTIONAL SILICON DEVICES<br>• JFET/MOS TECHNOLOGY |
| 350 - 450°C<br>662 - 842°F | • GEOTHERMAL | • III - V COMPOUND TRANSISTORS |
| >500°C<br>>932°F | • MAGMA AND NEAR MAGMA EXPLORATION | • INTEGRATED THERMIONIC DEVICES<br>• MAGNETICS |

B. High Temperature Electronics Development at Sandia

Sandia's development efforts in high temperature electronics have been done in support of geothermal well logging activities. Well logging is complicated by severe noise pick-up in cables which may be 15,000 ft or greater in length. For this reason it is standard practice in logging lower temperature oil and gas wells to (1) provide for down hole amplification, and (2) convert the analog signal from the transducers to a digital signal for transmission up hole. Flow, temperature and pressure tools have been developed at Sandia and tested in the field to 275°C.

1. Flow Tool

A turbine type flow sensor capable of measuring flow velocities in the region between 0.3 feet/minute and 200 feet/minute has been developed. The signal conditioning electronics located within a few inches of the turbine blades provides a digital output in the frequency range between 0.1 and 10 kHz. The resolution achieved at the recording instrument is 0.15% of full scale.

2. Temperature Tool

The temperature tool employs a platinum resistance sensor to measure temperatures up to 275°C. The voltage output of this sensor is compared to the output of a voltage reference, converted to a series of pulses by a voltage to frequency converter and then fed to line driver circuitry. All of the circuits are located within a few inches of the sensors. The up hole recording instrument counts the number of pulses received in a given time band to determine the frequency of the digital signal output which is proportional to the temperature at the sensor. Circuits developed to date provide a digital output up to a maximum frequency of 50 kHz. Temperature is measured at the recording instrument to an accuracy of 0.5°C with a resolution of 0.1°C.

3. Pressure Tool

The pressure tool employs a Bourdon type sensor to achieve an analog voltage output proportional to pressure. Signal conditioning electronics identical to that employed for the temperature tool are used

to achieve a resolution at the recording instrument of 0,3% of full scale over the pressure range between 0 and 5,000 psi. A quartz crystal pressure sensor capable of a maximum pressure of 10,000 psi and 0.05 psi resolution is currently being developed. This sensor will operate at several MHz.

4. Circuit Technology

The electronics for the flow, temperature and pressure tools use multilayer thick film hybrid technology. The typical size of the 96% alumina substrate of the circuit is 1 inch x 2 inches, with three substrates per tool. Conductors are fritless plague free gold made from Dupont 9910 or AVX 3520 inks. Thick film resistors are deposited on the microcircuits; their compositions were adjusted to achieve the minimum temperature coefficient of resistance at 150°C. Some capacitors are commercially available and some are printed on the microcircuits. The dielectric for the printed capacitors is ESL 4515 fired at 925°C. Thick film to thick film interconnections were made with gold ribbon. Thermocompression bonds are used for gold beam leaded transistors and ultrasonic bonds of aluminum wire are employed to interconnect the transistor chips to the conductor pattern. Silicon JFET chips made by Motorola and silicon CMOS chips made at Sandia's Semiconductor Processing Laboratory are active devices. The electronic circuits and sensors are mounted in a K MONEL housing for logging application.

The circuits were designed to operate over the entire temperature range from 25°C to 300°C by accommodating the variation in electrical properties of the components through circuit design. Variations of several orders of magnitude are encountered in the reverse bias resistance of p-n junctions in transistors, while the resistance of thick film resistors printed from specifically designed inks are less than 1% over their temperature range.

The initial design objective of the program was an electronics technology with a lifetime of 100 hours at 300°C. Improvements have resulted in most components and processes having lives of 1000 hours or longer. There appears to be no fundamental impediment to much longer lifetimes. Circuits have typically been cycled several times without noticeable deterioration.

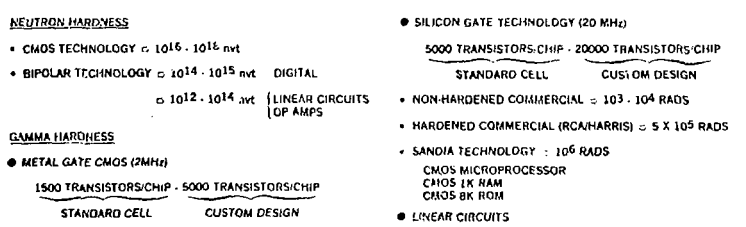
## III. Radiation Hardened Electronics

Sandia has developed a variety of radiation hardened linear and digital circuits for application to aerospace systems. These applications have frequently required radiation tolerance of semiconductor components significantly higher than is available on the commercial market. Sandia built a fully qualified microelectronics processing laboratory five years ago to advance the state-of-the-art of hardened microelectronics to be compatible with radiation tolerant aerospace system's requirements. During this time period, we have been actively involved in hardened circuit and device development as well as transfer of processing technology to the commercial semiconductor industry.

### A. State-of-the-Art of Hardened Microelectronics

The general radiation hardness capability of microelectronics circuits are summarized in Table II.

Table II: Overview of Radiation Hardened Semiconductor Technology




One may note that neutron hardness capability of CMOS technology is generally two to three orders of magnitude higher than bipolar technology and that the neutron hardness capability of digital circuits is roughly two orders of magnitude higher than linear circuits.[6]

The gamma hardness capability of microelectronics circuits is shown in more detail in Table II where metal gate technology is compared to silicon gate technology.

Present metal gate technology at Sandia is radiation tolerant to $10^7$ rads but high production parts are qualified to only $10^6$ rads.[7] Hardened commercial silicon gate technology is capable of higher frequency switching and has higher transistor density than metal gate technology; however, it has only 50% of the radiation tolerance. Latch-up is avoided in CMOS circuits with high gamma dose rate requirements by neutron irradiation burn in to reduce the gain of parasitic bipolar transistors. Note the one to two orders of magnitude difference between the gamma hardness of hardened and nonhardened commercial technology.

In the commercial area radiation hardened linear circuits are generally an order of magnitude more sensitive to gamma radiation than digital circuits. Sandia is developing a CMOS analog to digital converter and a bipolar operational amplifier which are expected to have a proven radiation hardness tolerance of $10^6$ rads. Sandia has not developed any circuits capable of operating up to $10^8$ rads gamma dose; however, an aluminum metal gate CMOS discrete transistor with a thin gate oxide insulator has been built that was radiation tolerant to $10^8$ rads gamma dose.[8] This device probably lacks the reliability required for most applications; however, high reliability will likely be achieved while maintaining $10^8$ rads hardness by employing tungsten metal gates.

B. Sandia Integrated Circuit Activities

Sandia has traditionally developed microelectronics integrated circuits for the Department of Energy; however, in recent years we have been asked to develop radiation hardened circuits for agencies outside of DOE and transfer the technology to commercial vendors. Integrated circuit development activities at Sandia are summarized in Table III.

Table III: Integrated Circuit (LSI) Development at Sandia and Technology Transfer Activities

DEPARTMENT OF ENERGY

- 40 Custom Metal Gate Circuits for Random Logic Applications
- 4 MNOS Non-volatile Memory Circuits
- 5 Silicon Gate Circuits for Random Logic and Data Encryption Applications
- Second Source Capability
  Metal Gate Technology
  Silicon Gate Technology
  MNOS Technology

Table III (con't)

SAMSO

- Radiation-Hardened Bulk Silicon Gate Technology (transfer to Harris Semiconductor)
- Fault-Tolerant Spaceborne Computer, 8 bit ALU, 1K RAM, 8K ROM (transfer to Harris Semiconductor and Raytheon Company)
- Defense Satellite Program Bulk CMOS RAM Evaluation
- High Performance Non-Volatile MNOS RAM

NATIONAL SECURITY AGENCY

- Sanchez Qualification Program (Motorola)
- Keesee Field Oxide (Harris)
- Secure, Terrorist Proof CMOS Memory
- MNOS Electrically Alterable ROM--for Code Storage

DEFENSE NUCLEAR AGENCY

- Hardened Field Oxide
- High-Performance CMOS Technology

NASA-JPL

- Consult on Galileo Semiconductor Procurement
- Supply Hardened Parts (Microprocessors, RAMS, custom chips)

NAVAL RESEARCH LAB

- Supply Hardened RAMS for Naval Satellite Program

## IV. High Temperature, Radiation Hardened Electronics

Development activities at Sandia to date have not required electronics to survive both high temperature and radiation environments. However, in a high temperature environment one would expect some annealing of the radiation damage especially at low dose rates and irradiation for long periods. In other ways the two environmental requirements oppose each other. For example, radiation hardness in CMOS technology is achieved by close control of processing chemistry and in some cases by altering the physical design. Thinning the gate oxide layer to achieve hardness would generally make CMOS technology more susceptible to thermal stressing at high temperatures.

One of the high temperature CMOS development activities at Sandia involves the study, testing and evaluation of CMOS technology in SSI/MSI configurations to determine processing, geometric, operating characteristics and stability parameters.[9] After more than 1000 hours at 300°C this technology shows good stability, reliability and operating characteristics. These devices have not been radiation tested; however, they were built in Sandia's Semiconductor Processing Laboratory and employed similar processing steps as are used for radiation hardened CMOS. Thus a gamma hardness capability of $10^6$ rads would not be unexpected. It is clear that high temperature and radiation hardness can be merged in CMOS technology. Whether this merging could result in a 300°C, $10^8$ rads technology base is uncertain.

## V. Application of High Temperature, Radiation Hardened Electronics to Nuclear Power Plants

It is beyond the scope of this paper to precisely outline the utility of high temperature, radiation hardened electronics to nuclear power plant monitor and control instrumentation. However, several observations of a general, qualitative nature may be made.

Close proximity between sensors that monitor the safety status of a nuclear power plant and the signal conditioning electronics has several attributes. First, if analog data are converted to digital data close to the sensor, then noise pick-up is minimized. Secondly, the digital data from several sensors may be multiplexed and the data carried to instruments located in the control room of the reactor. Thus data from many sensors would require a single cable penetration of the containment wall. This must be a desirable safety feature and has cost advantages as well. Third, such a design approach is amenable to standardization. One analog to digital conversion circuit and one multiplexing circuit could be applicable to many types of sensors. Thus the cost of qualifying the circuits to the environmental requirements of the containment building would be minimized.

Advanced high temperature semiconductor electronics are compatible with containment atmosphere requirements in the range of 40°F (4°C) to 400°F (205°C) and high range containment area radiation requirements of $10^7$ rads/hour for gamma rays.[10] It is presumed that beta radiation could be effectively shielded from the electronics at low cost. The gamma radiation dose rate requirement compares to a rate of $6 \times 10^3$ rads/hour measured in the containment dome at TMI-2 five hours into the accident.[11] The ability of electronics to survive the gamma environment for an acceptable period of time depends upon the accident history. For example, a

10-hour exposure at a rate of $10^7$ rads/hour would introduce a dose of $10^8$ rads which is at the upper limit of any solid state electronics known to have been built. Thus employment of solid state electronics in the containment building would likely require some shielding to reduce the total gamma dose to a tolerable level and a precise definition of the radiation environment.

Other possibilities exist for application of high temperature, radiation hardened electronics. For example, core conditions during and after SCRAM could be monitored with an electronics package containing sensors and signal conditioning electronics that were inserted in the reactor core during SCRAM. Such a package could measure and process (through analog to digital conversion) data on radioactivity level, water height and coolant temperature in the core. Under conditions of a fast neutron flux of $10^{14}$ neutrons/cm$^2$/sec, such a package could be made to have a lifetime of 10,000 seconds or slightly less than 3 hours. However, under the proposed application (SCRAM conditions) the electronics would only be exposed to a high neutron flux for a short time period during each SCRAM (roughly 1 minute). The remainder of the time (during normal operation) the electronics would not be located in the core. A post SCRAM gamma environment of $10^8$ rads/hour[12] would fail the hardest electronics in about 1 hour unless shielding were employed.

## VI. Summary

High temperature, radiation hardened electronics have potential application to the monitor and control systems of nuclear power plants. A containment temperature of 400°F is easily met by high temperature electronics; however, a containment dose rate of $10^7$ rads/hour existing for 1 hour would push the state-of-the-art of hardened electronics. Nevertheless, high temperature, partially shielded, radiation hardened electronics could be developed that would survive the thermal and radiation requirements of the containment building under accident conditions. Electronics that could survive periodic insertion in the core of a nuclear reactor could also be developed. In addition to economic payoff, radiation hardened, high temperature electronics could impact reactor safety by reducing the number of cable penetrations through the containment wall permitting noise free, high quality data to be brought to the control room.

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