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Manual

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Savannah River Plant Californium-252 Shuffler

Electronics Manual

MASTER

University of California

LOS ALAMOS SCIENTIFIC LABORATORY

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SAVANNAH RIVER PLANT CALIFORNIUM-252 SHUFFLER ELECTRONICS MANUAL

by

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ABSTRACT

Detailed information is presented in this report, an electronics manual for the Savannah River Plant Shuffler, about the electronics associated with the various control and data acquisition functions of the Shuffler subsystems. Circuit diagrams, interconnection information, and details about computer control and programming are included.

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1. INTRODUCTION

The Savannah River Plant (SRP) Shuffler is an instrument that performs nondestructive analysis of SRP scrap materials. The amount of the fissile uranium isotope ^{235}U is measured by an active assay technique consisting of neutron interrogation of the material with a 0.8-mg ^{252}Cf source followed by detection, after removal of the source, of the delayed neutrons emitted by the ^{235}U fission products. The cyclic process of sample interrogation followed by counting continues until adequate precision for the assay is achieved.

This report is an electronics manual for the Shuffler. Detailed information is presented about the electronics associated with the peripheral and environmental hardware, the computer system, and the neutron detection system. Additional sources of information, including a print package available from the Technical Information Center, Oak Ridge, Tennessee, are listed in the Appendix.

2. GENERAL DESIGN

Except for a few custom-designed interface modules, the electronics used in the Shuffler to collect data and to control the assay sequence are available commercially. The use, where possible, of commercial units permitted fabrication of the instrument with a minimum leadtime and facilitates duplication by outside vendors.

Operation of the Shuffler is controlled by a Digital Equipment Corp. (DEC) LSI-11 microcomputer with 28k 16-bit words of random access memory. Operator-computer communication is effected with a hard-copy terminal (DEC LA-36 DEC-writer and a cathode-ray tube (CRT) terminal with a detachable keyboard (Research, Inc. 3741D Teleray). A Data Systems Design, Inc. 210 dual diskette drive unit permits storage and retrieval of programs and data. Interfacing to the Shuffler assay hardware is accomplished through the LSI-11 Q-BUS.

The electronics are enclosed in a sealed rack whose temperature and humidity are controlled by an air conditioner. A line regulator maintains the ac voltage at a constant level. Circuit breakers and temperature sensors shut down the electronics in the event of serious malfunction. The electronics block diagram for the Shuffler is shown in Fig. 1.

The control functions of the electronics include transfer of the ^{252}Cf source between the source storage and sample irradiation positions, rotation of the sample, and placement of the sample on (and removal from) the load cells for weight measurement. To limit hazardous radiation conditions, the source transfer and sample positioning electronics are interlocked.

The primary data collected by the electronics are the delayed neutron counts observed in various ^{3}He-filled proportional counters. From the count rates, which are recorded in a scaler bank, the software deduces the amount of ^{235}U in the material being assayed. Auxilliary data collected include the sample weight (obtained from load cells), the temperatures inside the LSI-11 chassis and inside and outside the electronics rack (obtained from thermocouples), and the humidity inside the rack (obtained from a dew-point hygrometer).

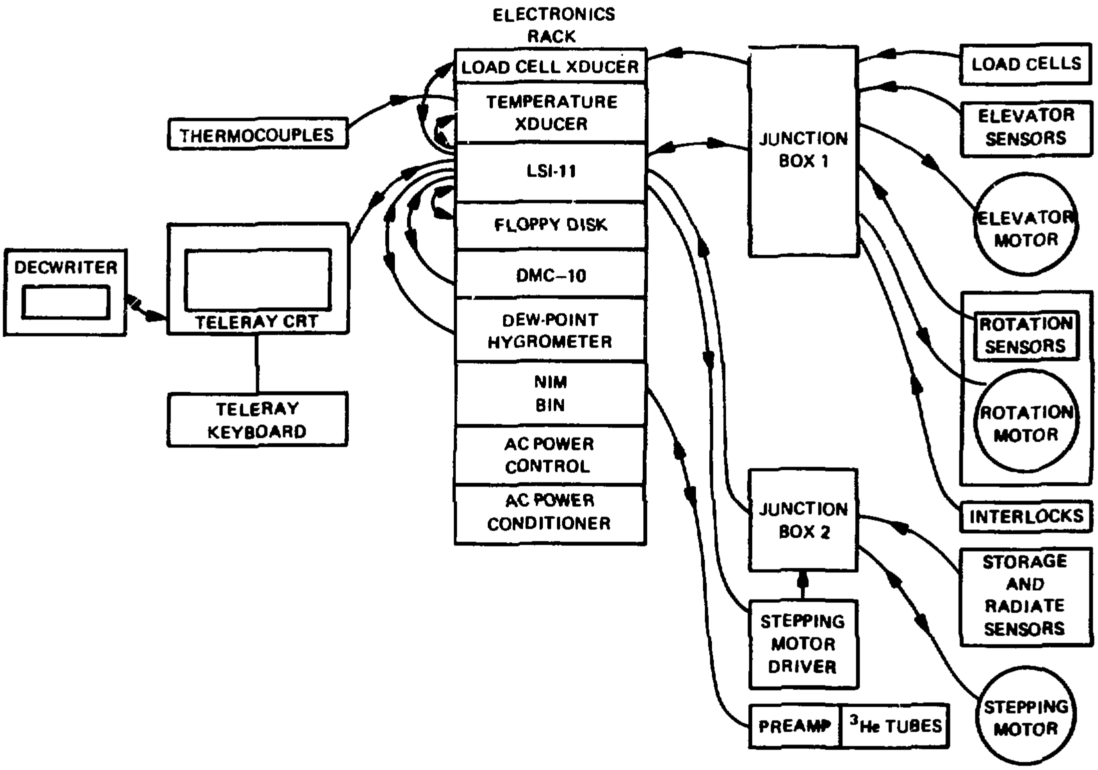

Fig. 1. Electronics block diagram for the SRP Shuffler.

3. PERIPHERAL HARDWARE

3.1. Computer Terminals

The Shuffler system has two computer terminals, a Research, Inc. 3741D Teleray with a detachable keyboard and a DEC LA-36 DECwriter. Figure 2 shows a block diagram of the two terminals, the LSI-11, and connecting cables.

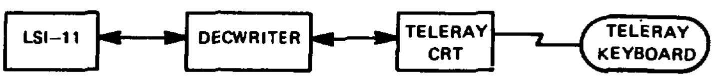

Fig. 2. Block diagram of the computer terminals and the microcomputer.

Local control and hard copy of the assay data are provided by the DECwriter located near the computer. The detached keyboard of the Teleray provides remote control from the scrap storage vault. The CRT of the Teleray is located outside the storage vault and is viewed through a window. This separation minimizes the amount of electronics that might become contaminated in the storage vault. The large character display of the Teleray facilitates viewing at a distance.

The two terminals are linked in series to the DEC DLV-11 serial line interface. Figure 3 shows the cable pin assignments. Current loop transmission at 300 bits/s was selected to allow use of optical isolation. The character frame is one start bit, eight data bits, and two stop bits.

3.2. Floppy Disk

The Shuffler system uses a Data Systems Design, Inc. 210 dual floppy disk drive unit for program loading and assay data storage.* Table I lists the floppy disk specifications. The only modification to the unit was to label the two drives with the identification used by the DEC RT-11 software (DX0 and DX1). The operation diskette containing the ASSAY and TEST programs, calibration and reference data, and a small portion of the RT-11 software is loaded into the drive labled DX0. The assay data are written onto the data diskette in the drive labled DX1.

3.3. Sample Weight Measurement Hardware

The outputs of the three Interface, Inc. MB-75-4 load cells located under the turntable are summed and sent to a Doric Scientific DS-300-T2 digital transducer. The binary-coded decimal (BCD) output of the transducer is sent to an ADAC Corporation 1632 input/output (I/O) board (see Sec. 4.2.4) to be input to the LSI-11 at addresses 167702 and 167704. Input to the computer is in grams and has a maximum value of 39 999 g.

3.4. Sample Motion Hardware

The material to be assayed is placed on a turntable that is lowered to and raised from the load cells by an ac elevator motor. Two optical sensors (HEI Inc. OS-591S-200LW) determine the position of the turntable. When neither sensor is blocked, the turntable is in the down position and the material can be weighed. When both sensors are blocked, the turntable is in the up

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*A complete discussion of the Shuffler software is given in "Savannah River Plant Californium-252 Shuffler Software Manual" by Susan S. Johnson, Thomas W. Crane, and George W. Eccleston, Los Alamos Scientific Laboratory report LA-7717-M (March 1979).

TABLE I

DUAL FLOPPY DISK DRIVE UNIT[a]

SPECIFICATIONS

Storage Medium	Type: IBM diskette or certified equivalent Number of Tracks: 77 Tracks per Inch: 48 Track Width: 0.3048 mm (0.012 in.) Track-to-Track Spacing: 0.508 mm (0.020 in.)
Recording Technology	Recording Mode: double frequency Bit Density (inner track) 3200 bits/in. Bit Transfer Rate: 250k bits/s Read/Write Head: ceramic
Maximum Capacity (unformatted)	Drive: 3.2 megabits Track: 41.7 kilobits
Maximum Capacity (formatted)	Drive: 256 256 bytes System: 768 768 bytes
Disk Speed	Rotation Speed: 360 rpm ± 2% Rotation Time: 166 ms Average Latency: 83 ms
Head Positioning (access) Time	Head Positioning: 8 ms track-to-track Head Loading Time: 40 ms
Environmental Characteristics	Operating Temperature: 15.5°C (60°F) to 32°C (90°F) Maximum Rate of Change: 8.3°C/h (15°F/h) Relative Humidity: 20% to 80% at 29.4°C (85°F) Storage Temperature: -40°C (-40°F) to 51.6°C (125°F)
Power Requirements (dual drive)	Standard: 115 V ac, 60 Hz at 2.5 A Optional: 115 V ac, 60 Hz or 230 V ac, 60 Hz or 230 V ac, 50 Hz
Physical Characteristics	Height: 266.7 mm (10.5 in.) Width: 431.8 mm (17 in.) Depth: 571.5 mm (22.5 in.) Weight (dual drive): 24.5 kg (54 lb)

[a]Manufactured by Data Systems Design, Inc.

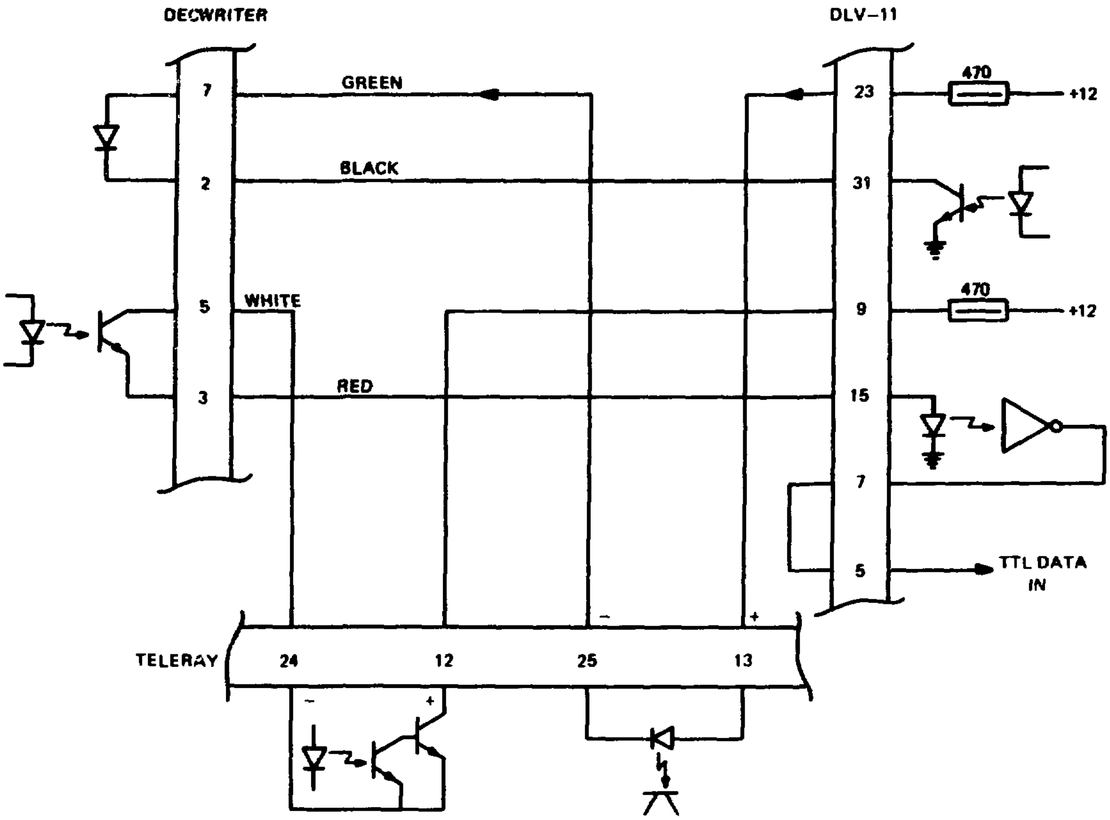

Fig. 3 Pin assignments of the DECwriter and Teleray connections to the DLV-11 serial line interface.

position and the turntable can be rotated. An optical sensor on the turntable (also HEI Inc. OS-591S-200LW) detects each rotation cycle.

Interlocking circuitry provides that the elevator motor will operate (upon request) only (a) if the assay chamber plug is in place or (b) if the plug is removed when the turntable is down. In the latter case, the turntable is raised automatically. Interlocking circuitry also provides that the rotation motor will operate (upon request) only if the plug is in place and the turntable is up.

LED lamps on the LSI-11 front panel (see Sec. 4.1.4) indicate power to the elevator and rotation motors, turntable up and down positions, weight on the load cells, rotation cycle completed, and rotation motor off.

The elevator and rotation motors can be controlled either by the computer or with the switches on the LSI-11 front panel (see Sec. 4.1.4). Each ac motor is controlled through a zero-crossing, optically isolated solid state relay to provide noise immunity for the LSI-11.

All turntable sensor outputs are sent to the encoder and I/O board (see Sec. 4.2.2) for entry into the LSI-11. The rotation motor automatic controls come from the encoder and I/O board through the status logic board (see Sec. 4.1.3) to the solid state ac motor driver relays.

3.5. Source Transfer Hardware

3.5.1. Automatic Control. The ^{252}Cf neutron source is moved on the end of a teleflex cable by a Sigma Instruments, Inc. 21-3450D-23821 stepping motor. A Sigma Industries, Inc. DMC-10 programmer module controls the bipolar chopper driver (also Sigma Industries, Inc.) that powers the stepping motor. The distance, maximum speed, ramp rate, and starting speed are preset in the DMC-10. The direction of motion is specified by a software program in the LSI-11. When the DMC-10 REMOTE/MANUAL switch is set to REMOTE, the LSI-11 controls the index and jog functions. The source position is monitored through an optical incremental shaft encoder coupled to an up/down counter that is input to the LSI-11 by reading address 167762 assigned to the encoder and I/O board. The least significant 12 bits of the 16-bit word read represent the source position. (See Sec. 4.2.2 for programming information.)

As shown in Fig. 4, two optical sensors (HEI Inc. OS-591S-200LW) mounted on the teleflex cable housing detect the storage and irradiation positions of the source. The circuit diagram for these sensors is given in Fig. 5. The sensor inputs to the LSI-11 are through the encoder and I/O board and are optically isolated. The source position is displayed on the LSI-11 front panel (see Sec. 4.1.4). The truth table for source positioning is given in Table II.

3.5.2. Manual Control. The manual controls for source transfer, located on the DMC-10, are activated by first setting the DMC-10 mode switch to MANUAL and then pressing the selected function switch. If no action occurs, perform the following operations at the keyboard of either terminal. (Operator-typed key commands are underlined; ODT responses are not.)

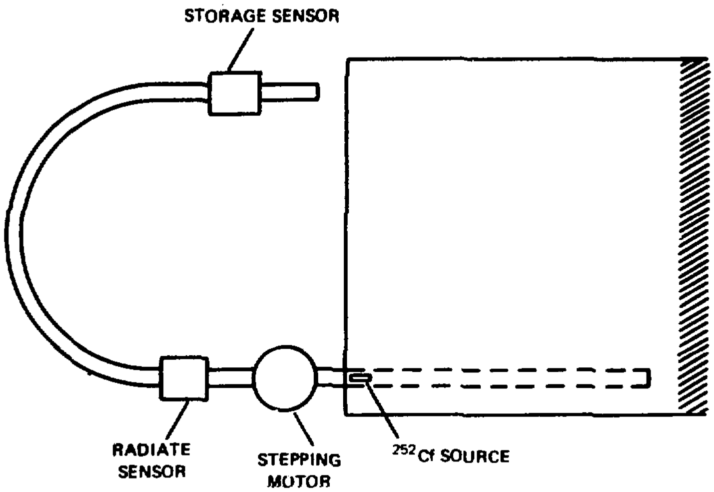

Fig. 4. Californium-252 source transfer system.

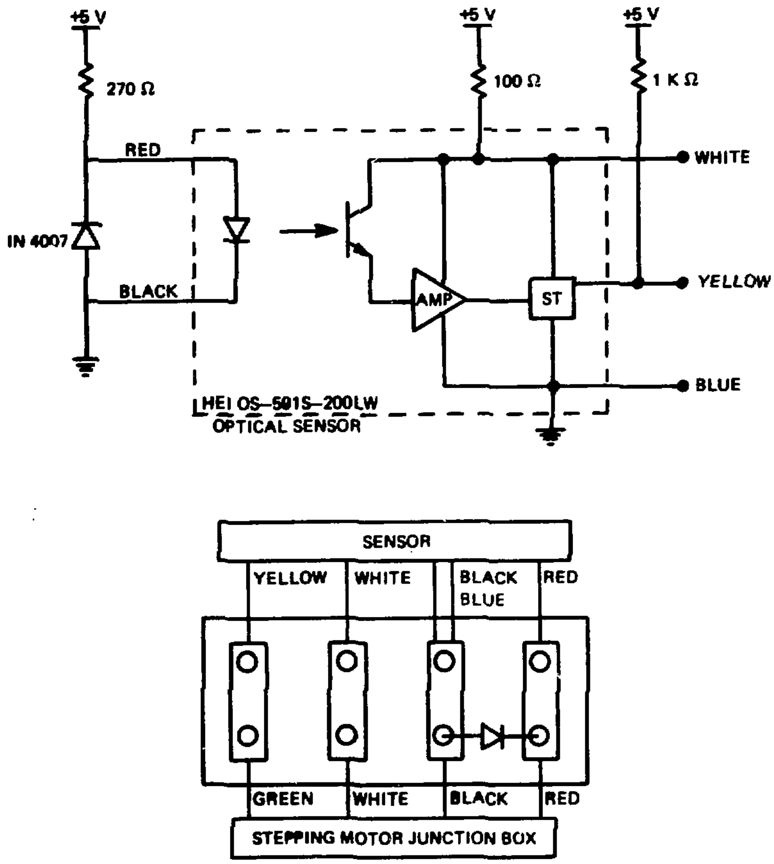

Fig. 5. Circuit diagram for the source position sensors.

TABLE II

SOURCE POSITION TRUTH TABLE

STORAGE Sensor	RADIATE Sensor	LSI-11 Front Panel Indicator	Comment
0	0	RADIATE	Neither sensor blocked
0	1	TRANSFER	Cable blocking RADIATE sensor
1	0	none	Error condition
1	1	STORAGE	Cable blocking both sensors

BREAK (Press the BREAK key; the LSI-11 is now in ODT mode.)

@ 167760/000000 7400 CR (CR is the carriage return key.)

@

The manual control functions should now be operable. Caution must be exercised when manually controlling the source because the safety interlocks are bypassed. To return to remote control, set the DMC-10 mode switch to REMOTE and type P followed by CR on the keyboard.

Before running any of the software programs, the teleflex cable should be in a position such that the LSI-11 front panel indicators show that the source is in the storage position. If the source is in the transfer position, the cable can be moved by hand by first turning off the power to the bipolar chopper driver, thus removing the holding torque, and then hand turning the shaft on the stepping motor until the source reaches the storage position.

3.6. Temperature Measurement Hardware

3.6.1. General. Three copper-constantan thermocouples monitor the temperature inside and outside the electronics rack and inside the LSI-11 chassis. The thermocouples are multiplexed by computer control into an Omega Engineering, Inc. 2160A digital thermometer where the temperature is digitized, displayed, and made available to the ADAC 1632 I/O board in the LSI-11 chassis. Figure 6 shows a block diagram of the temperature measurement system. A software program selects one of the three multiplexed probes, reads the register of the ADAC 1632 I/O board, and converts the two BCD digits to binary. Upon

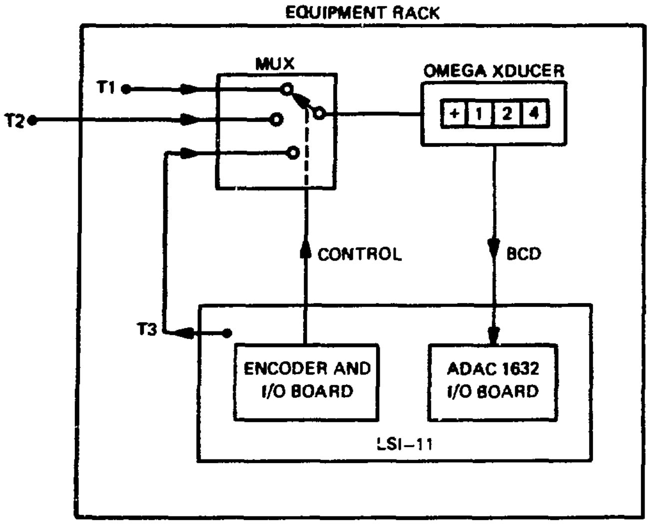

Fig. 6. Block diagram of the temperature measurement system.

completion of the assay, the temperatures are included with the data stored on the disk file.

3.6.2. Multiplexer. The multiplexer, located on a vector board next to the temperature transducer, contains two 5V relay chips and one 75454 driver chip. An AUTO/MANUAL switch and a probe selection switch located on the temperature panel allow manual selection of temperature readout. When the system programs are being run, the AUTO/MANUAL switch must be set to AUTO. The multiplexer circuit diagram is given in Fig. 7. Section 4.2.4 describes the bit selection, addressing, and control of the temperature signals through the ADAC 1632 I/O board.

3.7. Humidity Measurement Hardware

The humidity inside the electronics rack is measured by a General Eastern Corp. series 1200 condensation dew-point hygrometer. The output, three BCD digits, is cabled to the DEC DRV-11 parallel I/O board in the LSI-11 chassis. Two status bits from the hygrometer, HOLD and PRINT COMMAND bits, are also part of the input to the DRV-11. When the HOLD bit is a zero, the hygrometer is in a calibration cycle and its output is not valid. When the PRINT COMMAND bit is a zero, the hygrometer can be read. Valid data will be read only if the HOLD bit is a one and the PRINT COMMAND bit is a zero. The BCD data and

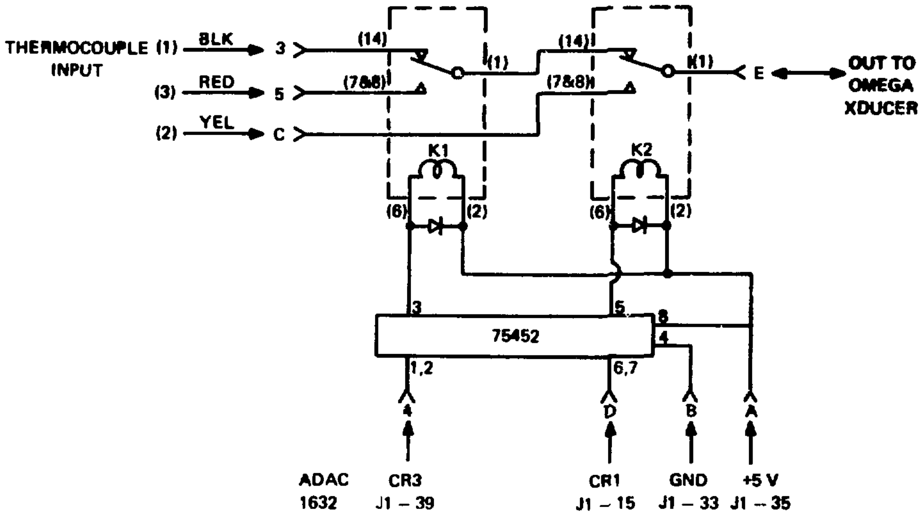

Fig. 7. Thermocouple multiplexer circuit diagram.

DEW-POINT HYGROMETER PIN NUMBER	AMPHENOL CONNECTOR PIN NUMBER	DATA TRANSMITTED	J2 Pin	DRV–11 DATA BIT AT ADDRESS 177544
10	4	SIGN BIT	P	13
20	14	BCD 100	U	12
16	9	BCD 80	V	11
18	11	BCD 40	W	10
19	12	BCD 20	Y	9
6	K	BCD 10	Z	8
13	7	BCD 8	CC	7
5	J	BCD 4	EE	6
14	8	BCD 2	HH	5
4	H	BCD 1	KK	4
11	5	BCD 0.8	BB	3
3	F	BCD 0.4	H,E	2
12	6	BCD 0.2	LL	1
2	E	BCD 0.1	TT	0
7	N	GND	J	
7	R	SHIELD	L	
1	D	$\overline{\text{HOLD}}$	N	14
8	3	$\overline{\text{PRINT COMMAND}}$	M	15

Fig. 8. Bit layout and cable pin assignments for the dew-point hygrometer inputs.

the two status bits are read into the DRV-11 at address 177544. The bit layout and cable pin assignments are shown in Fig. 8.

4. LSI-11 SYSTEM

4.1. Chassis

The LSI-11 chassis includes a rack-mountable enclosure, a DEC H9270 dual backplane, three power supplies, two zero-crossing solid state relays, a line filter, two standalone boards, two fans, and front and rear panels. There are two ac inputs, one for the power supplies and the other for the zero-crossing relays. The chassis is 48.3 cm (19 in.) wide, 55.9 cm (22 in.) deep, and 17.8 cm (7 in.) high.

4.1.1. Power Supplies. Power to the LSI-11 and the interfaces is provided by two Power-One, Inc. power supplies, one 5V-23A and the other 12V-6.8A. An Analog Devices, Inc. 5V-1A power supply is used for external logic and optical isolators. The power supply ac is filtered through the line filter.

4.1.2. Dual Backplane. The dual backplane has a capacity of eight quad-wide cards and has a tilt-up frame for easy access. Figure 9 shows the placement of the cards in the backplane.

4.1.3. Standalone Boards. One of the standalone boards, the power fail control board, is a power fail, power restart, and line clock board. This board has two switches, one for the CPU HALT/RUN and the other for the line clock ENABLE/DISABLE.

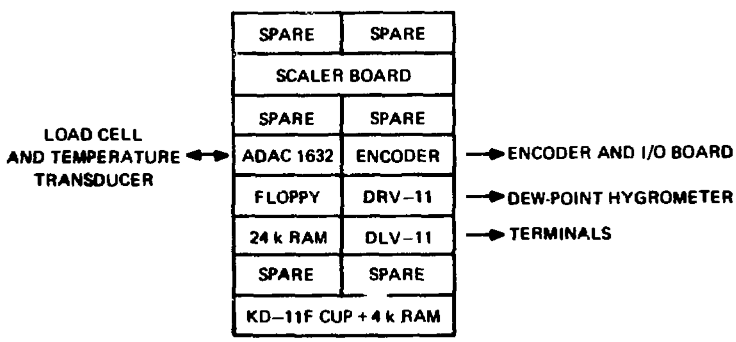

Fig. 9. Q-BUS backplane card assignments.

The other standalone board, the status logic board, contains the interlocking circuitry (see Sec. 3.4) and driver controls for the elevator and rotation motors. The circuitry for positive conformation of ac power to the motors is also on this board and is fed back to the encoder and I/O board for entry into the LSI-11. A circuit diagram for this board is located in the Appendix.

4.1.4. Front Panel. As shown in Fig. 10, the front panel is blocked off into four sections. The COMPUTER section contains the power on/off switch, two lights that show +5V and +12V power, and a light indicating that the LSI-11 CPU is in RUN status.

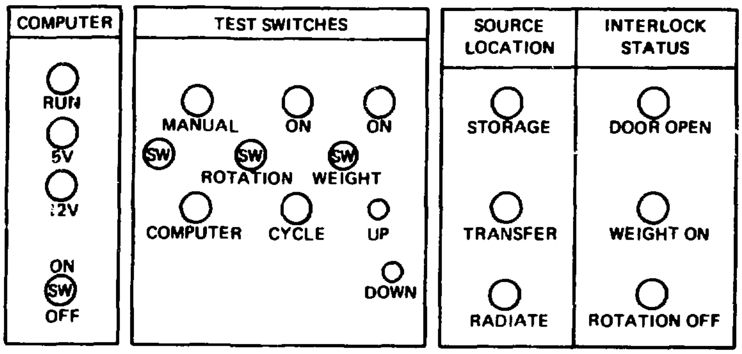

Fig. 10. LSI-11 chassis front panel.

The TEST SWITCHES section has a switch with MANUAL and COMPUTER lights. When this switch is set to MANUAL, the manual ROTATION and manual WEIGHT switches are enabled. The ON lights indicate power to the rotation and elevator motors. The LED lamp CYCLE flashes once per revolution of the turntable (6 s). The LED lamps UP and DOWN show the status of the turntable.

The lights in the SOURCE LOCATION section indicate that the ^{252}Cf neutron source is in one of three positions: the storage position (STORAGE), the irradiation position (RADIATE), or in between (TRANSFER).

The lights in the INTERLOCK STATUS section indicate that the assay chamber plug is out (DOOR OPEN), that the turntable is in the down position (WEIGHT ON), and that the rotation motor is off (ROTATION OFF). All INTERLOCK STATUS lights must be off for the system to be in operational mode.

4.2. Q-BUS and Interfaces

4.2.1. Q-BUS. The DEC Q-BUS transfers signals between the LSI-11 CPU and memory and the interfaces. The bus is bidirectional and has 16 data/address lines and 18 control/synchronization signal lines.

4.2.2. Encoder and I/O Board. The encoder and I/O board transfers source position information from the stepping motor to the LSI-11, provides all interface circuitry to the Q-BUS, and effects digital I/O between the LSI-11 and other peripherals. The circuits are built on an MDB Systems Inc. 1710 foundation wirewrap module with space for 20 user chips. The board provides a clear command, written at memory address 167766, to clear all I/O registers and counters. A 3M Company 40-pin connector provides a flat ribbon cable that is split into four sections. One section goes to the status logic board, another to the DEC KWV-11 clock, and the remaining two to the P2 and P3 connectors on the LSI-11 back panel. The pin assignments for this ribbon cable are given in Fig. 11.

Steering logic in the encoder circuit transforms the two-phase serial information from the optical incremental shaft encoder on the stepping motor to up/down information for the 12-bit 74193 up/down counter. The source position information can be read at memory address 167762. The two-phase inputs A and B from the shaft encoder are filtered and optically isolated to provide noise immunity.

The encoder input bits consist of two status bits from the optical incremental shaft encoder (A and B), two bits from the source irradiation and storage position optical sensors (STORAGE and RADIATE), a bit from the assay chamber plug interlock sensor (DOOR OPEN), a bit from the sample rotation optical sensor (CYCLE), two bits from the turntable position sensors (ELEVATOR 1 and ELEVATOR 2), a busy bit from the DMC-10, two bits from the elevator and rotation ac power sensors, and a bit from the LSI-11 front panel MANUAL/COMPUTER switch. The last three bits are not optically isolated. The bit layout for this encoder input word, read at memory address 167764, is given in Fig. 12.

The 12-bit encoder input is multiplexed to a 12-bit encoder outport port consisting of two 6-bit 74176 registers. The memory address for writing out to this port is 167760. The bit layout for this word is given in Fig. 13. The INDEX, FWD, REV, and JOG bits are set for use by the DMC-10. The ROTATION

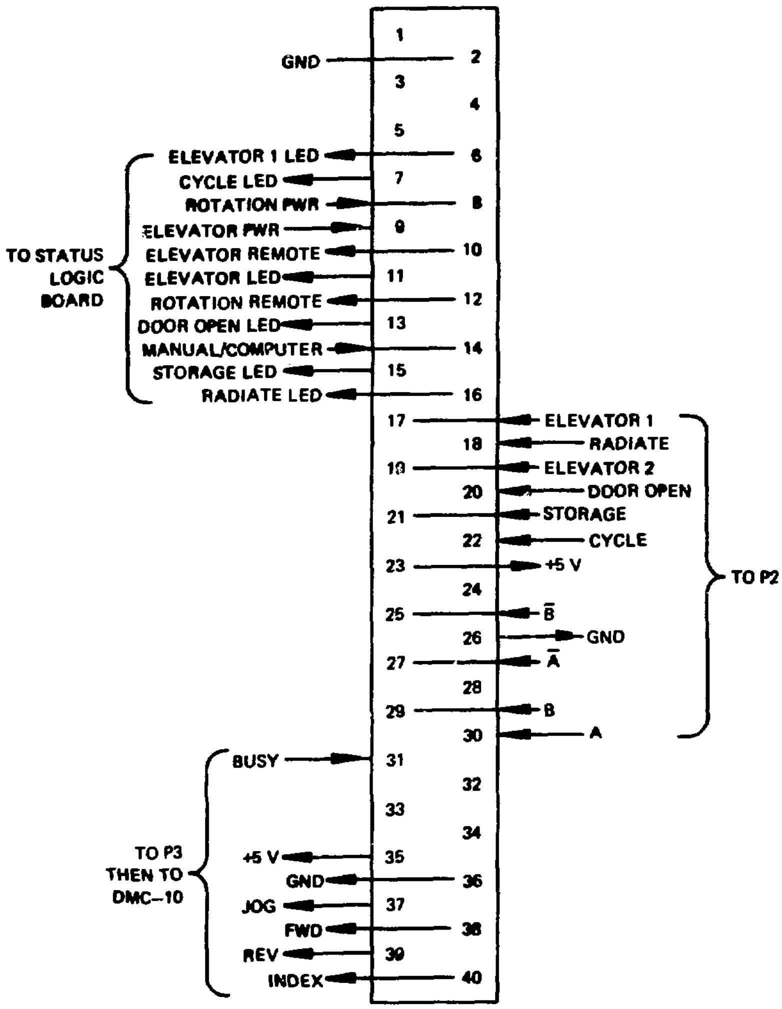

Fig. 11. Pin assignments of the encoder and I/O board ribbon cable.

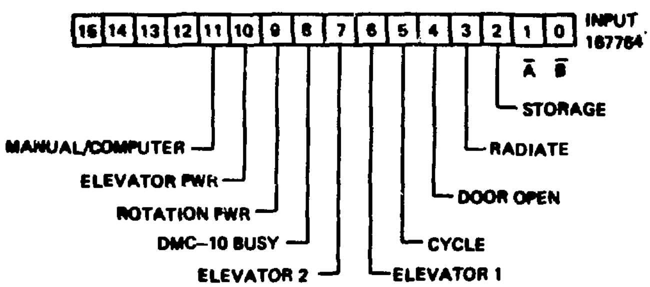

Fig. 12. Bit layout for the encoder and I/O board input port.

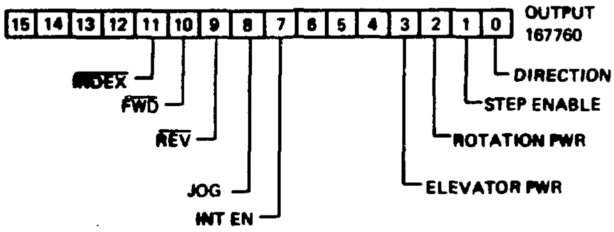

Fig. 13. Bit layout for the encoder and I/O board output port.

and ELEVATOR bits turn on the zero-crossing relays to the elevator and rotation motors. The DIRECTION and STEP ENABLE bits can be used to drive the stepping motor bipolar chopper driver directly using the KWV-11 clock as a source of pulses to the encoder and I/O board's 74123 one-shot pulse extender.

A summary of the commands for the encoder and I/O board is as follows.

- 167760 Output Write to 12-bit output port.
- 167762 Input Read 12-bit up/down counter.
- 167764 Input Read 12-bit input port.
- 167766 Output Write to clear all I/O registers and counters.

4.2.3. Scaler Board. The scaler board is a quad-wide board that plugs directly into the Q-BUS; it consists of six separate channels, each with a 24-bit (16 777 215) count capacity. The scaler inputs are TTL compatible and operate in a ripple mode. A count is registered upon transition of a pulse from a low to a high state. The minimum pulse width for counting is 50 ns; the pulse pair resolution of the scalers is 30 ns. A universal clear strobe zeroes all counters simultaneously. A control status register directs the individual scalers to enable/disable counting or to read contents. Counting and readout functions of the scalers can be tested with a feature that permits scaler incrementing.

The FORTRAN-callable scaler driver effects all communications required to control the scaler board. The following FORTRAN calls control the scalers.

- CALL CSCAL — Clear all scalers.
- CALL ESCAL (X) — Enable scalers designated by X.
- CALL RSCAL (N, DATA) — Read scaler N; assign name DATA to its contents.
- CALL TSCAL (INC) — Test all scalers by incrementing INC times; precede this command with ESCAL (0).

The clear command (CSCAL) requires no input parameters; all scalers are cleared. The enable command (ESCAL) requires an octal parameter (X) that specifies which scalers are to be enabled. For example, octal 35 (binary 11 101) enables scalers 4, 3, 2, and 0 (and disables scaler 1). The read command (RSCAL) assigns the name DATA to the count obtained from the scaler specified by N (N = 0,1,2,3,4,5); the count data are in double precision integer format (INTEGER*4). The test command (TSCAL) tests the scalers by incrementing them INC times. Before testing, all scalers must be disabled with the command CALL ESCAL (0).

Scaler 5 is unique because its input is a 1-MHz clock. Thus, the counts in scaler 5 are the number of microseconds the scaler was enabled. Scaler 5 is used during an assay to measure counting time intervals for the other five scalers.

4.2.4. ADAC 1632 I/O BOARD. The ADAC 1632 I/O board, a double-width board, can receive up to 32 inputs. The board receives the BCD information from the temperature and load cell transducers and controls the thermocouple multiplexer. The board has two 3M Company ribbon cable connectors J1 and J2 used, respectively, for the temperature I/O and the load cell inputs. Figure 14 shows the pin assignments of these cables.

Two modifications were made to the board. One supplies +5V and ground through the ribbon cables to the load cell transducer optical isolators; the other permits all load cell inputs to be on a single ribbon cable. The latter modification was effected with jumpers from J1 to J2.

There are three 16-bit registers on the ADAC 1632 I/O Board. One is a status and I/O control register; the other two are 16-bit input registers A and B. The status and I/O control register, selected at memory address 167700, provides output control signals CR1 and CR3 that are sent to the thermocouple multiplexer to select one of three thermocouples. The bit layout for the status and I/O control register is shown in Fig. 15; the bit pattern for thermocouple selection is given in Table III.

TABLE III

THERMOCOUPLE SELECTION BIT PATTERN

CR3 Signal	CR1 Signal	Thermocouple Selected
0	0	1
0	1	2
1	1	3

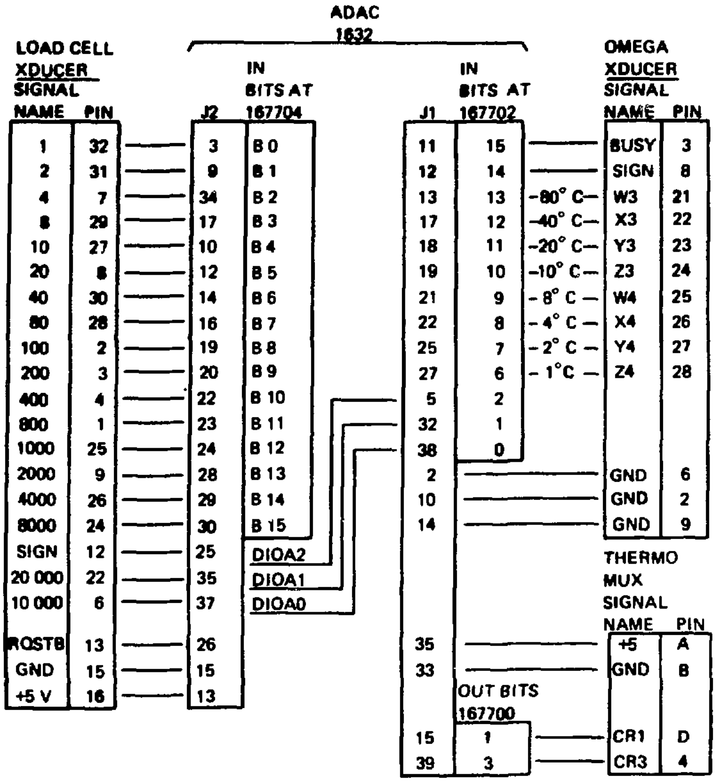

Fig. 14. Pin assignments of the two cables J1 and J2 between the ADAC 1632 and the load cell and temperature transducers.

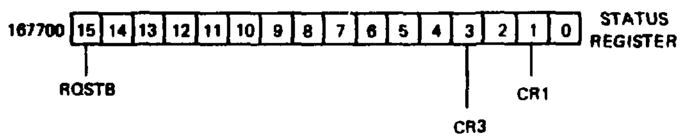

Fig. 15. Bit layout for the ADAC 1632 status and I/O control register.

Register A contains the temperature BCD input bits and three of the load cell BCD bits. Register B contains the remaining load cell bits. The bit layout and memory addresses for these registers are shown in Fig. 16 and 17.

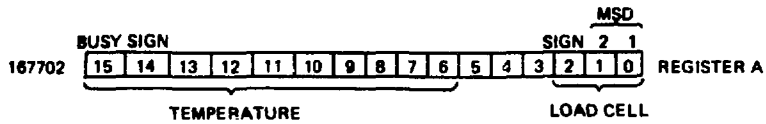

Fig. 16. Bit layout for the ADAC 1632 input register A.

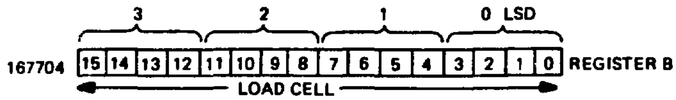

Fig. 17. Bit layout for the ADAC 1632 input register B.

5. DELAYED NEUTRON DETECTION SYSTEM

The neutron detection system consists of ^{3}He-filled proportional chamber neutron detectors, preamplifiers, combination amplifier-single channel analyzer (SCA) modules, high-voltage power supplies, and the scaler board in the LSI-11 chassis. A block diagram of the five detector electronics chains is shown in Fig. 18.

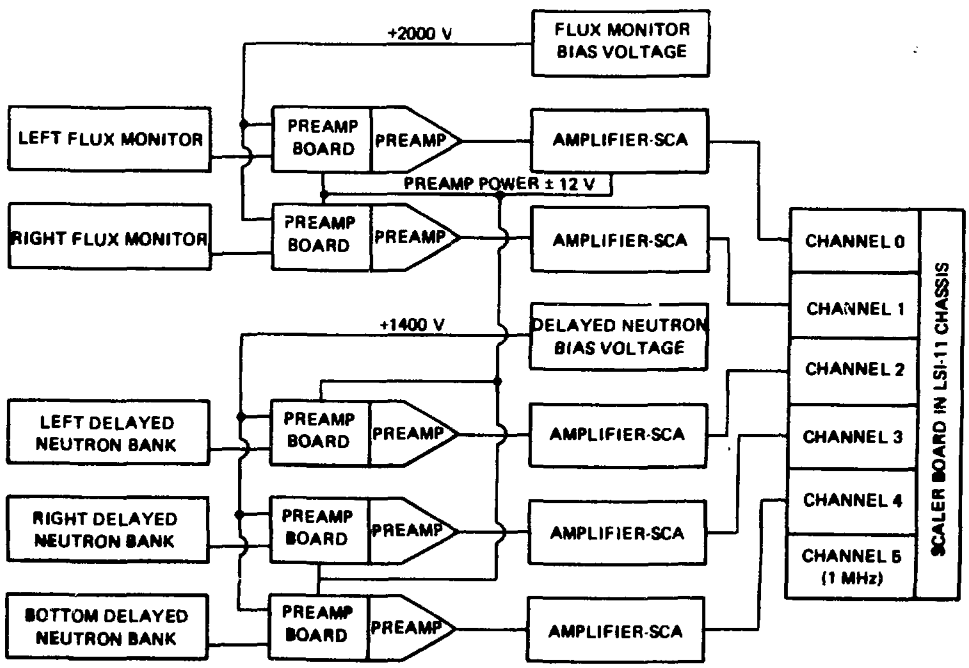

Fig. 18. Block diagram of the neutron detection and counting system.

The size, number, and type of ^{3}He tube differ for the flux monitors, the two side detector banks, and the bottom detector bank. The specifications of the ^{3}He tubes, manufactured by Reuter-Stokes, Inc., are given in Table IV.

TABLE IV

^{3}He NEUTRON DETECTOR SPECIFICATIONS

Electronics Chain Designation	Number of Neutron Detector Tubes	Diameter by Active Length (mm)	Gas Mixture and Pressure
Left flux	1	6.35 by 76.2	40 atm ^{3}He, Ar and CH_4[a]
Right flux monitor	1	6.35 by 76.2	As above
Left delayed neutron bank	8	25.4 by 533.4	4 atm ^{3}He, 5% CO_2[b]
Right delayed neutron bank	8	52.4 by 533.4	As above
Bottom delayed neutron bank	2	25.4 by 279.4	As above
	2	25.4 by 254.0	As above
	2	25.4 by 203.2	As above

[a]The mixture is selected for fast risetime and good resolution.

[b]The mixture is selected for gamma-ray and noise insensitivity.

Although the tubes differ, the same electronics units are used for all five detector electronics chains, one of which is shown schematically in Fig. 19. To aid in describing the function and operation of the electronic components, a neutron event is traced as follows from its origin in the gas-filled detector to its registration as a count in one of the scaler channels.

The ^{3}He nuclei and the delayed neutrons emitted by the ^{235}U fission products undergo the exothermic reaction $^3He + {}^1n \rightarrow {}^3H + {}^1H + 765$ keV.

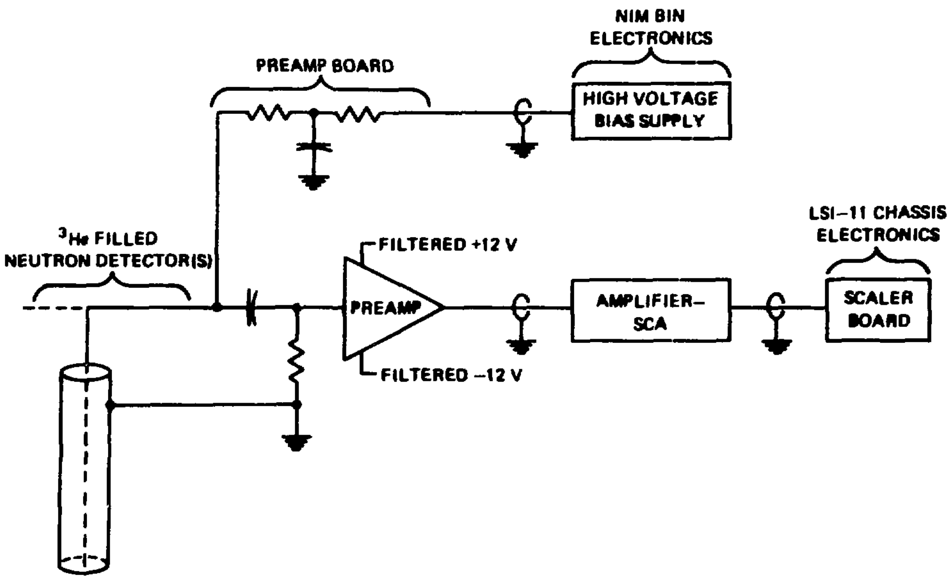

Fig. 19. Schematic diagram of a delayed neutron detector electronics chain.

The 765-keV energy, shared by the triton (^{3}H) and the proton (^{1}H), is rapidly absorbed by the detector gas. Part of the energy absorbed ionizes the atoms of the gas. As the electrons released by the ionization accelerate toward the thin wire in the center of the tube (maintained at a positive potential by the high-voltage power supply), they gain sufficient energy to cause further ionization. Thus, the number of electrons reaching the center wire is far greater than the number of electrons produced initially. These electrons constitute a negative pulse that reaches the preamplifier through the dc blocking capacitor.

5.1. Preamplifiers

The preamplifier, whose circuit diagram is given in Fig. 20, was chosen primarily because of its compactness. The unit, designed and fabricated at Los Alamos Scientific Laboratory, has proved reliable in several other applications. Because of its relatively low cost and compact component arrangement, it is more practical to replace the preamplifier than to attempt to repair it. The unit plugs into the high-voltage distribution board. An

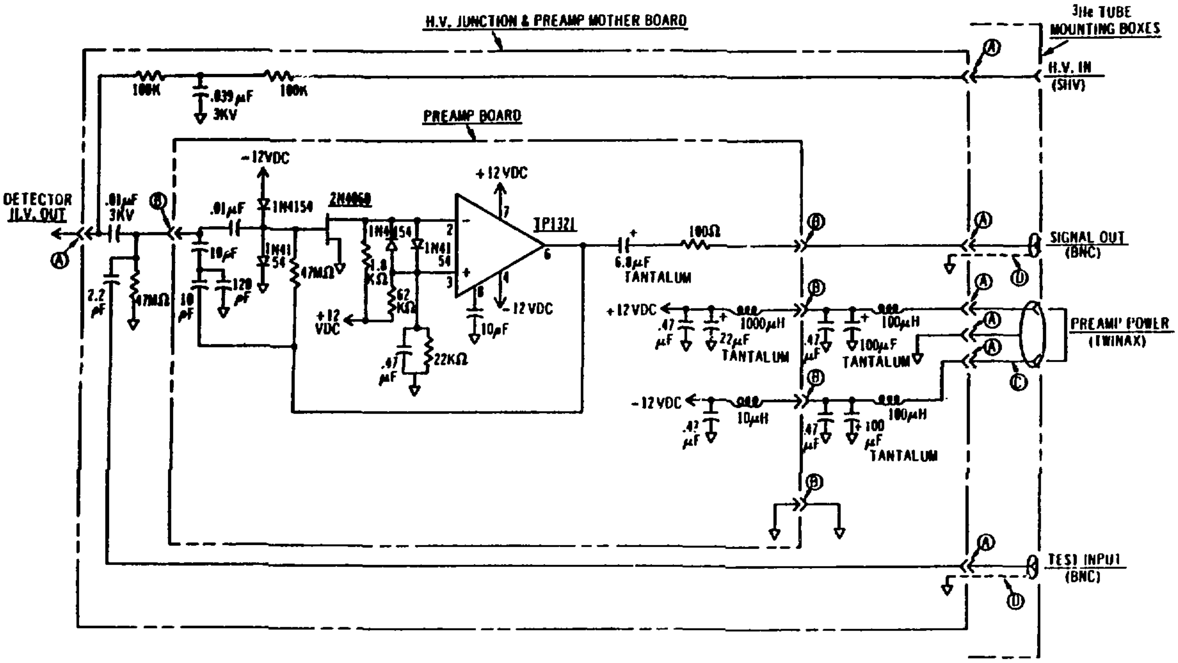

Fig. 20. Preamplifier circuit diagram.

inverting amplifier in the preamplifier matches the high impedance signal from the neutron detector tube to the low impedance input to the combination amplifier-SCA.

5.2. Amplifier-Single Channel Analyzers

The amplifier-SCA is an Ortec Inc. 490B NIM module with no modifications. The amplifier gain is adjusted with an oscilloscope to yield a 5-V pulse for the most intense neutron pulse band. The unit also contains an SCA that selects pulses from the amplifier with amplitudes corresponding to that of the neutron pulses. The lower amplitude limit for pulse acceptability is set to exclude extraneous noise pulses; the upper limit is set just below the dynamic range of the amplifier to avoid counting pulses that saturate either the amplifier or the preamplifier. The amplifier-SCA side panel switch settings for each of the electronics chains are given in Table V; the front panel gain and window settings are given in Table VI. The output of the SCA drives the input to the scaler board in the LSI-11 chassis (see Sec. 4.2.3).

TABLE V

AMPLIFIER-SCA SIDE PANEL SWITCH SETTINGS

Electronics Chain Designation	Window (INT or EXT)	Input Polarity (NEG or POS)	Lower Level (EXT or INT)	Amplifier (UNI or BI)
Left flux monitor	INT	POS	INT	BI
Right flux monitor	INT	POS	INT	BI
Left delayed neutron bank	INT	POS	INT	BI
Right delayed neutron bank	INT	POS	INT	BI
Bottom delayed neutron bank	INT	POS	INT	BI

TABLE VI

AMPLIFIER-SCA FRONT PANEL GAIN AND WINDOW SETTINGS

Electronics Chain Designation	Amplifier Coarse Gain	Amplifier Fine Gain	Lower Level Discriminator (Volts)	Window Width (Volts)
Left flux monitor	64	∿5.4	2.00	7.00
Right flux monitor	64	∿6.3	2.00	7.00
Left delayed neutron bank	32	∿3.9	0.80	8.20
Right delayed neutron bank	32	∿3.8	0.80	8.20
Bottom delayed neutron bank	32	∿3.0	0.80	8.20

5.3. High-Voltage Bias Supplies

The two high-voltage units are Ortec Inc. 459 NIM modules. One module, operated at +2000 V, supplies the bias voltage for the two small flux monitor detectors inside the counting well. The other module, operated at +1400 V, supplies the bias voltage for the 25.4-mm diameter ^{3}He tubes that detect the delayed neutrons.

6. ENVIRONMENTAL HARDWARE

6.1. Electronics Rack

The electronics rack is a NEMA type 12 industrial-use enclosure made by Hoffman Engineering Co. Neoprene gaskets on the front and rear doors provide seals from dirt, oil, dust, and water. The enclosure is 183.0 cm (72-1/16 in.) high, 76.4 cm (30-1/16 in.) wide, and 92.9 cm (36-9/16 in.) deep.

6.2. Air Conditioner

The air conditioner for the electronics rack, a 2931 W (10 000 Btu/h) unit manufactured by McLean Engineering Midwest, is attached to the side of the rack and is 134.0 cm (52-3/4 in.) high, 48.3 cm (19 in.) wide, and 24.1 cm (9-1/2 in.) deep. The power requirements are 115 V ac at 13.2 A single phase.

6.3. Power Conditioner

The ac power is divided into raw and clean power. Clean power is derived from raw power by a Topaz Electronics line 2 power conditioner designed for mini/micro-computers. The power conditioner has fast ½-cycle response, efficiency of 94%, output capacity of 2 kVA, and noise attenuation greater than 140 dB at 1 kHz.

APPENDIX

ADDITIONAL INFORMATION SOURCES

Further information about particular aspects of the Shuffler electronics may be obtained from the following prints, which are available from the Technical Informtion Center, Oak Ridge, Tennessee, by citing CAPE No. 2658.

LSI-11 Drawer Chassis

Schematic	LEA 76-9052-01-SC
Backplane Wire Wrap Assembly	LEA 76-9052-04-FO
Direct Chassis Wiring Diagram Point to Point, Plan View	LEA 76-9052-05-SB
Power Fail Control P.C. Schematic	LEA 76-9052-21-SB

SRP Shuffler

Front Panel Status Logic Board	68Y-155585 D-57
Interconnect Diagram, Control System	68Y-155585 D-58
	68Y-155585 D-59
Encoder and I/O Card	68Y-155585 D-60
Encoder and I/O Card, 1710 Modifications	68Y-155585 D-61
Hoist Run and Brake	68Y-155585 D-62

Model 568 LSI-11 Six Channel Scaler

Schematic	4Y-223041 R3
P.C. Board Component Assembly	4Y-223041 C1
Panel Detail	4Y-223041 C2

In addition, the following information may be obtained from the manufacturers of the commercial units.

- Model 1632TTL 32 Bit Parallel Input/Output Instruction Manual

  ADAC Corporation
  15 Cummings Park
  Woburn, MA 01801

- GoLo Power Winch Installation, Operation, and Maintenance Bulletin No. PBW-10

  Cordem Corporation
  7600 Highway 7
  Minneapolis, MN 55426

- Model 210 Floppy Disk Manual

  Data Systems Design, Inc.
  3130 Coronado Drive
  Santa Clara, CA 95051

- Microcomputer Handbook 1977-78
- La-36 DECwriter II User's Manual

Digital Equipment Corp.
146 Main St.
Maynard, MA 01754

- Digital Strain Gage Transducer Indicator Model DS-300-T2 Owner's Manual

Doric Scientific
3883 Ruffin Road
San Diego, CA 92123

- General Instruction Manual 1200 Series Condensation Dew-Point Hygrometers

General Eastern Corp.
36 Maple St.
Watertown, MA 02172

- Electronics Rack Instruction Manual

Hoffman Engineering Co.
9th & Tyler Sts.
Anoka, MN 55303

- Model MB-75-4 Load Cell Calibration Certificate and Installation Information
- Model 7500 Digital Indicator Manual

Interface Inc.
7401 E. Butherus Dr.
Scottsdale, AZ 85260

- Slimboy Air Conditioner Instruction Manual

McLean Engineering Midwest
9560 85th Ave. North
Maple Grove, MN 55369

- Model 2160A Digital Thermometer Instruction Manual
- Model 2160A-02 Digital Output Unit Instruction Manual

Omega Engineering, Inc.
1 Omega Drive
Largo Industrial Park
Stamford, CT 06907

- Teleray 3700 Cl Series CRT Data Terminal Instruction Manual

  Research Inc.
  P.O. Box 24064
  Minneapolis, MN 55424

- DMC-10 Instruction Manual 29D-02

- Stepping Motor Power Units Instruction Manual H1204

  Sigma Instruments Inc.
  170 Pearl St.
  Braintree, MA 02184