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MULTI-HIT TIME-TO-AMPLITUDE CAMAC MODULE (MTAC)

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MASTER

Abstract

A Multi-Hit Time-to-Amplitude Module (MTAC) for the SLAC Mark III drift chamber system has been designed to measure drift time by converting time-proportional chamber signals into analog levels, and converting the analog data by slow readout via a semi-autonomous controller in a CAMAC crate. The single width CAMAC module has 16 wire channels, each with a 4-hit capacity. An externally generated common start initiates an internal precision ramp voltage which is then sampled using a novel shift register gating scheme and CMOS sampling switches. The detailed design and performance specifications are described.

Introduction

The Mark III drift chamber system requires a high time resolution, a high channel density because of the great number of channels (or wires), a fast resetting ability to accommodate the SLAC SPEAR beam cycle (780 ns), good temperature stability, minimum crosstalk between channels, and low power consumption.

Several schemes which appeared feasible were compared in terms of the project requirements. Several digital approaches were studied and were rejected because of the rather low time resolution (2-8 ns), high power consumption, and complex supporting hardware. The existing analog schemes had good timing accuracy but could not handle the multiple hits per channel. Therefore, a new design was initiated.

The basic module is a single width CAMAC with 16 channels, each with a 4-hit capacity (see Fig. 1). Upon reception of an externally generated RESET signal (common START, 90 ns width), the voltage ramp is initiated 50 ns before the earliest data input. The capacitors (100 pF) start to follow the ramp until the input (hit) signals from the drift chamber enter the shift-registers (74LS96), and consecutively open the FET gates (CD4066), isolating the time proportional voltages in each memory capacitor (see Fig. 2). At the end of 550 ns (maximum) drift time, an externally generated STOP signal blocks the input chamber signal path and enables CAMAC readout operation.

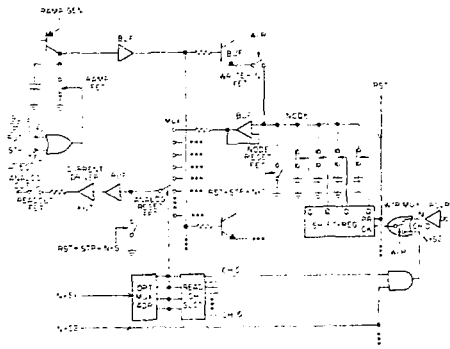


Fig. 1. MTAC Block Diagram.

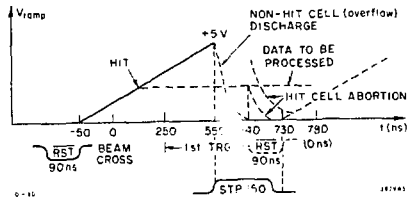


Fig. 2. Time Sequence of AMP Generation.

If the primary trigger decision is made to abort the data, then the external fast RESET signal is applied to discharge the hit cell capacitors and to enable the next data write cycle. If the decision is made to process the data, then the module is read out from further write cycles until readout by the semi-autonomous controller (BADC).

Readout is performed by utilizing BADC-generated CAMAC S1 and S2 pulses. Pulse S2 increments the channel shift register to consecutively read out and convert the charge from each cell, and the next S1 discharges that capacitor. Each cell readout requires 3 μs for the BADC address cycle, sample and hold, pedestal correction, and data conversion and storage.

Mark III System Organization

The basic Mark III system is shown in Fig. 3. Two crates share a dedicated autonomous controller (BADC) which contains a 16-bit ADC and 12K local memory. Crate A contains 960 data (4 hits/ch × 16 ch/module × 15 modules), while Crate B handles 1552 (18 modules) of multiplexed analog data. Crate A also contains a Crate Controller, Crate Verifier and a module (SPORT) for crate multiplexing and analog output buffering to the BADC. A simple slave module substitutes for the Crate Controller in Crate B. In the test setup, Crate A also contains an auxiliary controller for an LSI-11 micro-computer.

The scanning speed depends primarily upon the conversion speed of the BADC, as well as internal setup times. The average processing time per data point is 3 μs, leading to a total scanning time for all channels in two crates of about 6.4 ms (64 hits/module × 33 modules × 3 μs). The READOUT scan does not commence until certain fast trigger logic track-finding criteria have been

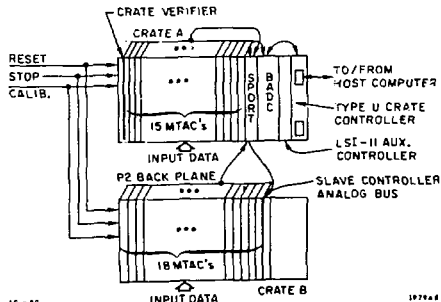


Fig. 3. System Organization.

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found. The droop (1.6 ns) during the maximum 6.4 ms hold time contributes negligible errors since each crate is scanned with a constant delay times for all events.

Detailed Circuit Description

The front end 16 channel (CH) input signal paths consist of translator-receivers, the WRITE/READ multiplexers (MUX) controlled by WRITE/READ-ENABLE circuit and the READ-CH SELECT circuit in READ, and 4-bit shift registers whose outputs are connected to the sampling FET switch gates. (See Fig. 1 MTAC Block Diagram.) A RAMP generator is followed by a buffer which fans out the RAMP to the 16-CH NODE(s) through each CH transistor emitter-follower and WRITE-IN FET switch. EACH NODE consists of 4 parallel memory capacitors (cells), each of which has a sampling FET switch in series, a NODE-RESET FET switch for resetting sampled charges or parasitic capacitor charges, and a CH-READOUT buffer. A READOUT control utilizes a 16-CH multiplexer which addresses each CH for four sequential CAMAC cycles, during which the four FET-capacitors of that channel are addressed.

The output is buffered through an adjustable gain stage and then through the READOUT FET to the BADC for digitization.

The front end input signal from the discriminator stage is a balanced differential ECL signal transmitted via a twisted-pair cable with 100 ohm nominal line impedance. The normal input signal width is about 100 ns followed by a minimum 20 ns dead time.

The receiver (MC10125) input terminals are biased so that the entire circuit operation will not be disturbed when a fault of the input line connection occurs. The RESET signal of 90 ns width is driven into another translator-receiver from the crate PC back plane. Since the signal is transmitted in a short printed circuit path, there is no need to terminate and bias the RESET signal receiver. The WRITE/READ multiplexer (25LS157) enables a clock path to the shift-register (74LS96). It selects either the detector (input) signal path for WRITE operation or readout path for READ operation, which is controlled by the READ-CH-SELECT circuit.

For READOUT the (N.S1) signals from consecutive CAMAC cycles are divided by four and scaled by a dual 4-bit counter (74LS393). The scaler output goes to the analog MUX address and also is decoded by the 25LS2538, which is enabled by N.S2, so that at N.S2 time the shift-register at the addressed channel is clocked, closing each of the four sampling FET switches in turn. (See Fig. 4 - Timing Diagram.)

The operation is initiated by the RESET signal of 90 ns width, which turns ON the RAMP FET (SD5000) and discharges the RAMP capacitor (330 pF). The trailing edge of the RESET signal which starts the RAMP (COMMON START) should be stable relative to the beam crossing (0 ns reference) which occurs every 780 nsec in SPEAR. The RAMP starts at -50 ns (+730 ns) from beam crossing to allow the RAMP to settle down. In normal operation, the RAMP reaches +3.4V amplitude at 550 ns maximum drift time. The RAMP generator is a voltage source. The diode D1 (1N3064) is to keep the RAMP base line at NODE roughly 0 volts.

For the calibration mode, which is performed by cosmic rays, the CALIBRATION signal (level) holds relay (K1) ON until the stop signal (150 ns \pm 5% width) turns it OFF. The resultant capacitance in the calibration mode becomes 720 pF, extending the RAMP time to 1.2 μ s at 3.5V RAMP height. The diodes D3 and D4 completely turn OFF the RAMP FET during WRITE operation. The overall system resolution in CALIBRATION mode was found to be \approx 1.5 ns.

The high speed buffer (LH0033) can provide 10 mA maximum output current over a wide power bandwidth (100 Mhz). The maximum current drawn during the maximum drift time by each CH-NODE of four parallel capacitor memories is about 2.5 mA. Due to the emitter-follower

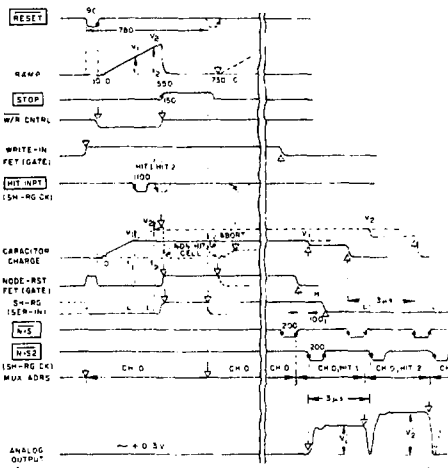


Fig. 4. MTAC Timing Diagram.

buffer ($R_{in} \approx 150K$) of voltage gain 1, located between the RAMP buffer and each CH-NODE, the total peak current drawn from the line driver is \approx 2.4 mA maximum. The series resistance of 100 Ω on each transistor base limits any possible oscillation and CH-to-CH interference, at the cost of slightly increasing the output resistance of the transistor buffer (by \approx 2 Ω).

The series WRITE-IN FET (SD5000) to the NODE becomes latched ON by the RESET signal, enabling the WRITE operation until the first N.S1 signal arrives. The first N.S1 isolates the WRITE-IN FET from the NODE for READOUT operation. Throughout the SD5000 FET circuits, the source is used as the input since feedback or reverse transfer capacitance of the SD5000 is lower when the drain is used as the output.

While all the sampling FETs (CD4066) and NODE-RESET FETs (SD5000) are ON, the NODE is reset during the 90 ns RESET signal prior to the common (RAMP) START. Since the time-constant in the sampling FET and the memory capacitor branch is 20 ns, the stored charges may be easily discharged in the allocated 90 ns (RESET) through the NODE-RESET FET (SD5000) in the event of an abort of the event. Actually, the NODE has an additional 50 ns for reset before the next beam crossing (0 ns), when the RAMP reaches about +0.36V. Empty (non-hit) cells are allowed to overflow up to the maximum RAMP voltage (+3.4V). The overflow charges in the cells are reset during a time of 180 ns maximum by the STOP signal and by the following RESET signal which is partially superimposed on the STOP. (See Fig. 2, Time Sequence of RAMP Generation.)

The shift register (74LS96) whose 4 parallel outputs are connected to the gates of the sampling FETs (CD4066) are held set (ON) in the beginning of the WRITE operation by the leading edge of the RESET signal until each HIT input-signal (4 nits maximum) on a channel resets each (output) bit in sequence, thus sampling the linear RAMP voltage.

In READOUT operation, N.S1 of the first CAMAC READOUT cycle resets all the shift-register bits and discharges stray capacitances of all the NODE(s). The first N.S2 pulse turns ON HIT 1 FET of CH0 and the fifth N.S2 HIT1 cell of CH1. Complete READOUT of a module requires 64 CAMAC cycles (192 μ s). An amplitude drop of about 38% occurs in the sampled capacitor voltage

when each cell is addressed. This is due to the capacitance of the CD4066's loading the NODE during readout, which is consistent throughout all NODE's.

The ΔR_{ON} of the sampling FET (CD4066) was measured over the maximum drift time range due to FET gate amplitude change from initial +3.8V at beam crossing to +4.6V; this was found not to contribute any significant nonlinearity to the charge measurement. The parameter ΔV_{DD} gave some contribution to the ΔR_{ON} change, resulting in some nonlinearity of the RAMP at the sampling capacitor over the drift time range. $V_{DD} = +6V$ was chosen for the best linearity (≈ 1 ns) up to the maximum drift time. (See Fig. 5, LINEARITY vs V_{DD} .) The gate signal driver for 1 SD5000 FET's is the TTL-to-MOS translator (75361).

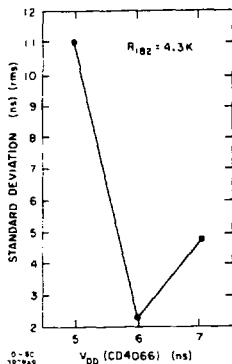


Fig. 5. Linearity vs V_{DD} .

The unity-gain voltage follower (CA3140T) on each NODE effectively isolates each sensitive NODE. The typical input leakage current of the CA3140 is ≈ 10 pA.

The 16-CH analog MUX (HI-506A) selects CH-outputs during the READOUT operation. It provides fast access time (500 ns typical) and low crosstalk. The CAMAC addressing cycle controlled by the BADC is 3 μ s, during which the BADC performs sampling/holding, pedestal correction and data conversion into digital form. At 2 μ s after addressing, the MUX output settles to within 0.1% of its full amplitude at 550 ns maximum drift time. The sampling of the analog output is done at about 2.6 μ s after address initiation. The MUX addressing is done by the OUTPUT-MUX-ADDRESS scaler which generates 4 READOUT (N.S2) pulses for each MUX address.

At the time every NODE is discharged through the NODE-RESET FET by RESET, STOP and 64 successive N.S1 pulses, the output of the analog MUX is reset through the ANALOG-RESET FET (SD5000).

The last buffer (CA3140T) with a voltage gain of about 1, located between the MUX and the final output terminal, provides, in addition to the buffering function, an output base line adjustment capability between 0 to +0.4V by a potentiometer (10K). This is necessary due to the fact that the BADC is biased to be unipolar (0 to +5V input).

The gain difference error among MTAC cards that may occur by the different pedestal level adjustments, is typically less than 0.02% of its normal voltage gain of 1, which is negligible.

The current driver (LH0024) stage, with closed loop gain of 1.74 boosts the maximum analog amplitude both at 550 ns maximum drift time and at 1.2 μ s calibration time to $\approx 3.5V$. The 1K resistor at the non-inverting input is to minimize the driver stage error due to the input bias current. The three capacitors (30p, 5p, 2p) associated

with the driver provide frequency compensation. The output rise time is slightly affected by the 100 Ω resistor at the driver output stage, which is added to isolate the LH0024 from the capacitive load of the analog cable connecting all modules in a crate to the BADC.

The READOUT FET (SD5000) driven by the TTL-to-MOS driver (75361) isolates ($R_{OFF} = 10^{10}\Omega$) the analog output circuit from the BADC input bus during WRITE-IN operation and until that module is selected for READOUT.

Since the input capacitance of the SD5000 is very low ($\approx 10p$), three switches are connected in parallel to improve the turn ON speed ($t_{ON} < 1$ ns). A maximum of 18 MTAC modules normally would be connected to the BADC at one time. The resultant time constant of the connected modules would be about 60 ns. The turn OFF time is given by the decay time-constant of the BADC input buffer resistance and the capacitance of the analog cable.

MTAC Tester

The MTAC Tester (135-641) is used to test MTAC modules in a laboratory setup. The module is capable of writing (WRITE operation) into a MTAC module with simulated detector HIT input signals. It also enables the BADC (135-421) to read the amplitude-converted analog data out of the MTAC module through the CAMAC system.

The front panel of the double width CAMAC module has a LOCAL/REMOTE operation mode control switch, four signal LEMO connectors, and a 36-pin connector for 16-CH HIT inputs to the MTAC. The four signals are: the initial START signal from an external pulse generator (BNC8010 source generator), BEAM-TRIGGER signal, INITIAL, and DELAYED pulses from a delay generator (BNC8010 programmable delay generator). (See Fig. 6, MTAC Test-setup Diagram.)

Upon the reception of INITIAL (INTL) signal initiated by the BEAM-TRIGGER pulse, the tester generates a differential ECL RESET (RST) signal that is a simulated Trigger System signal. The RST signal resets latches in MTAC, starting by its trailing edge of the pulse a positive RAMP of 600 ns width. During 550 ns drift time period, ECL HIT inputs from the tester to MTAC are generated by DELAYED (DLYD) signal to simulate the discriminator output. The selection of the number of up to 4-HITS on a channel, the HIT-CH address and WRITE mode (EA, SA, ALL, NONE) can be selected through a CAMAC WRITE command. The tester has another feature of repetitive

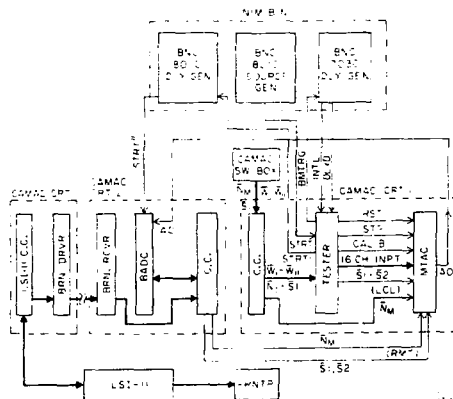


Fig. 6. MTAC Test-Setup.

(RPT) or nonrepetitive (NRPT) selection according to the WRITE line status.

HIT input delay during the RAMP can also be controlled by an external programmable BNC7030.

A switch on the front panel enables the selection of either local (LCL) or remote (RMT) mode operation. In LCL mode for a preliminary MTAC checkup, the MTAC module should be inserted in the crate #1. Following the WRITE operation, S1' and S2' signals are generated by the tester for a READ operation. The analog outputs are checked on an oscilloscope.

In remote (RMT) mode operation, the MTAC module is placed in crate #2. This is because the BADC and CAMAC Test Box cannot simultaneously access the same Crate Controller (135-315).

The RMT mode operation enables the BADC, controlled from an LSI-11 computer, to make precision measurements of MTAC outputs in various modes selected by the CAMAC Test Box. The START' signal originated by the external START pulse generates (through another delay generator) a START'' signal for the BADC to produce S1' and S2' signals under program control. This feature conveniently adjusts the READOUT pulse timing for a droop test following the WRITE operation.

The MTAC Tester requires 700 mA at +6V and 630 mA at -6V from the CAMAC crate power supply.

Performance and Specification Summary

A MTAC prototype was made and tested in a laboratory test setup (Fig. 6). The absolute linearity (deviation) vs drift time (550 ns maximum) is plotted in Fig. 7. The worst case deviation (2.3 ns) from a quadratic fit to the RAMP occurred at around 390 ns drift time.

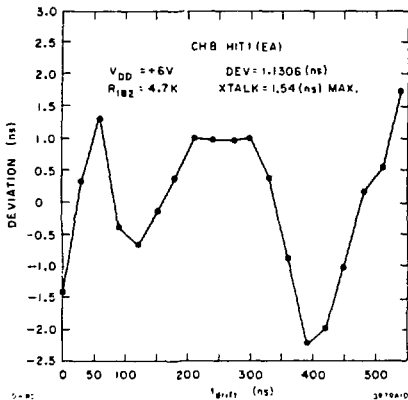


Fig. 7. Linearity (Deviation).

The extension of the normal operating range (RAMP = 550 ns) to allow cosmic ray calibration (RAMP = 1.2 μ s) resulted in a very poor linearity due to the fact that R_{ON} of the CD4066 sampling FET at V_{DD} = +6V suddenly changes when the RAMP amplitude exceeds +3.5V. Therefore, provision was made to increase the RAMP circuit capacitor for the calibration mode to generate a new RAMP with the same amplitude (+3.5V) at 1.2 μ s.

The performance specifications are as follows:

Crosstalk error (rms deviation in t_{DRIFT} measurement due to simultaneous 4-hits in all other channels in module) (see Fig. 8):

Operation mode (overall)	0.9 ns
(worst value)	1.5 ns max.
Calibration mode (overall)	0.9 ns
(worst value)	1.7 ns max.

RAMP error (rms deviations from quadratic fit to RAMP) (see Fig. 9):

Operation mode (0-550 ns)	1.1 ns
Calibration mode (0-1.2 μ s)	1.8 ns

Total resolution (combined rms error, due to effect of RAMP and crosstalk) is shown in Fig. 10:

Operation mode (0-550 ns)	1 ns rms
Calibration mode (0-1.2 μ s)	1.5 ns

Time shift due to temperature drift: 0.3 ns/10°C

Leakage droop (for 6.4 ms hold): 0.3% or 1.6 ns equivalent

Supply voltages: \pm 6V, \pm 24V

Power consumption: 10 W/module

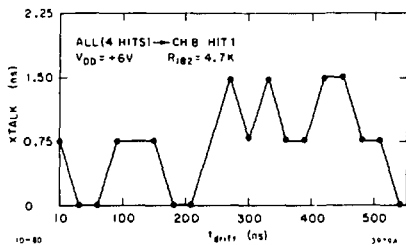


Fig. 8. Crosstalk.

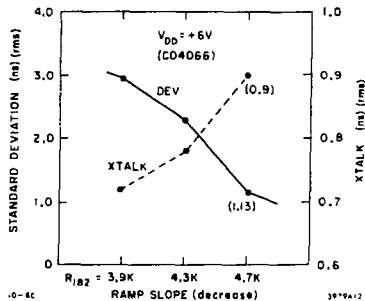


Fig. 9. Standard Deviation and Crosstalk on RAMP Slope.

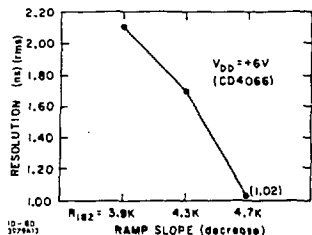


Fig. 10. Resolution vs RAMP Slope.

Conclusion

The MTAC system utilizes an accurate charge storage scheme where charge is proportional to the particle drift time, and an analog multiplexing scheme to provide readout for the drift chamber. The total analog data scanning speed depends on the number of modules associated with one BADC. The speed of scanning is 6.4 msec for 33 modules being scanned by one BADC; this is quite acceptable for the present MARK III system.

The MTAC technique offers the advantages of low cost per channel, high resolution, good linearity, and a low channel-to-channel crosstalk. It provides a fast resetting ability to accommodate the SLAC SPEAR beam. A relatively small power consumption with the moderate channel density and low leakage droop during readout are additional advantages. (See Fig. 11.)

Acknowledgements

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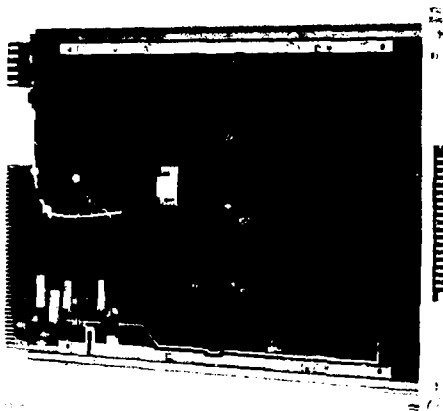


Fig. 11. MTAC

Reference

1. M. Breidenbach, E. Frank, J. Hail and D. Nelson, Semi-Autonomous Controller for Data Acquisition the Brilliant ADC, SLAC-PUB-2032, October 1977.