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(56) Documents cited
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(71) Applicants
Sony Corporation, 7—35 Kitashinagawa-6, Shinagawa-ku, Tokyo, Japan
(72) Inventors
Takeshi Matsushita, Takayoshi Mamine, Hisao Hayashi, Kazuo Nishiyama
(74) Agents
D. Young & Co.

(54) **Ion implantation methods for semiconductor substrates**

(57) A method of ion implantation for controlling the life time of minority carriers in a semiconductor substrate and hence to reduce the temperature dependency of the life time, comprises implanting iron ions into an N type semiconductor substrate with a dosage of 10^{10} to 10^{15} ions cm^{-2}, and then heat-treating the implanted substrate at 850° to 1250°C. The method is applicable to the production of diodes, transistors, Si controlled rectifiers and gate controlled switching devices.

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

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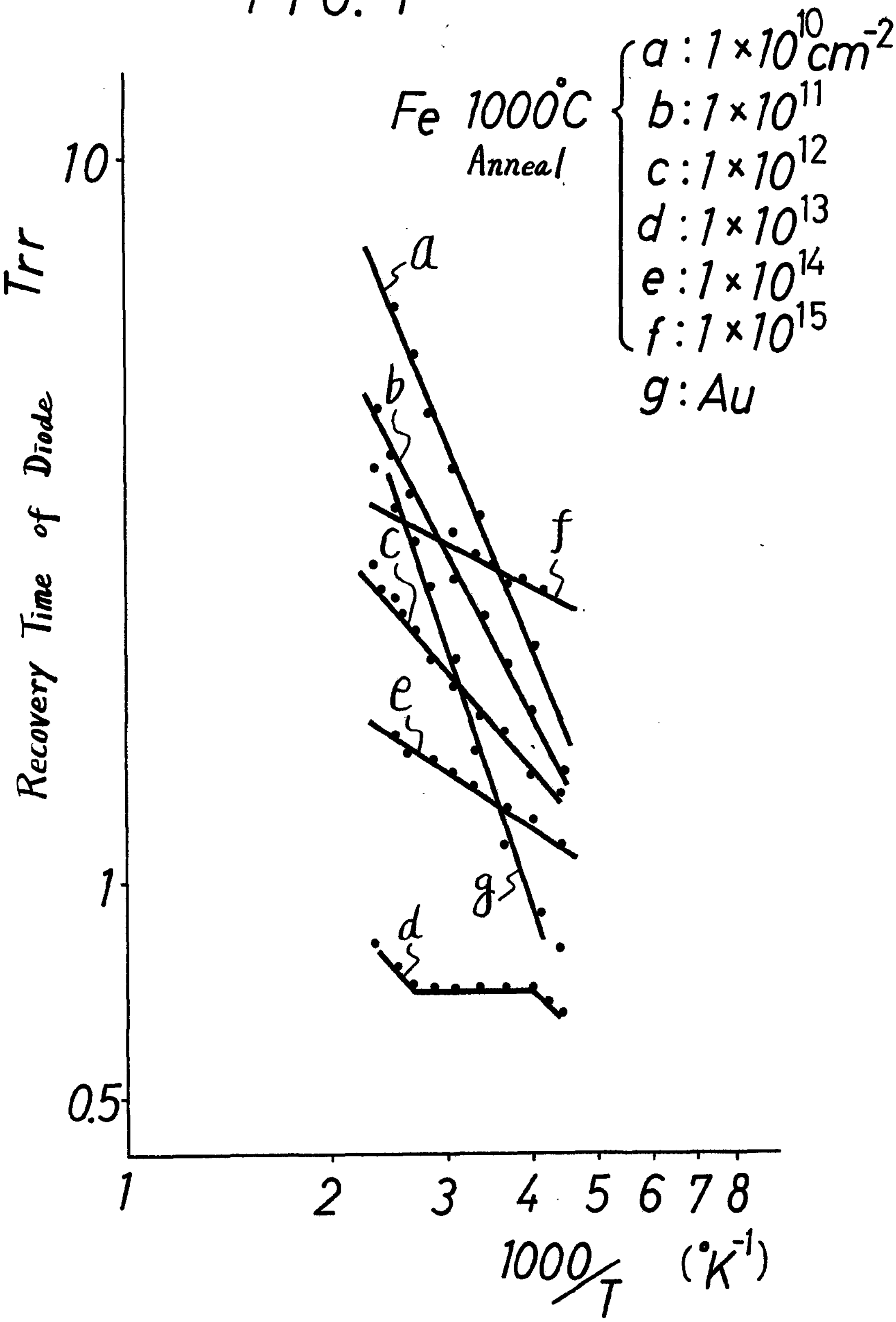
FIG. 1



Fe 1000°C Anneal
a : 1×10^10 cm^-2
b : 1×10^11
c : 1×10^12
d : 1×10^13
e : 1×10^14
f : 1×10^15
g : Au
Recovery Time of Diode Trr
10
1
0.5
1
2
3
4
5
6
7
8
1000/T (°K^-1)
a
b
c
d
e
f
g

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FIG. 2

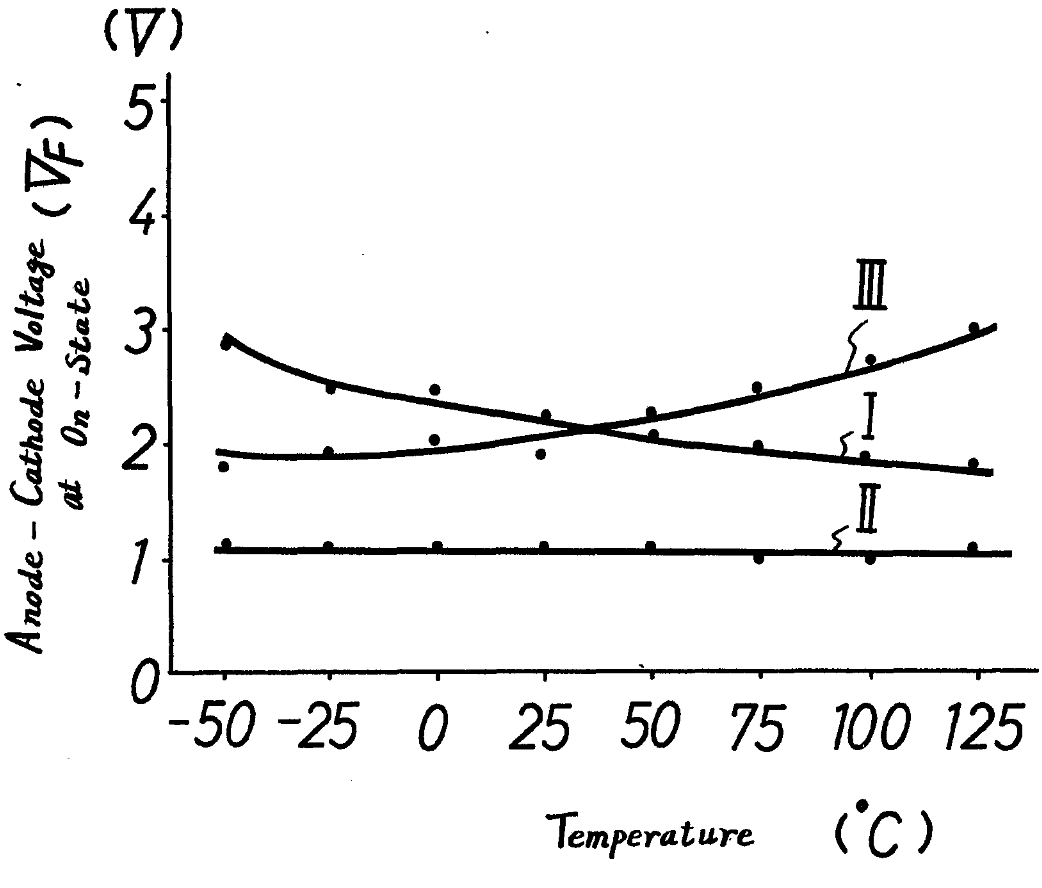

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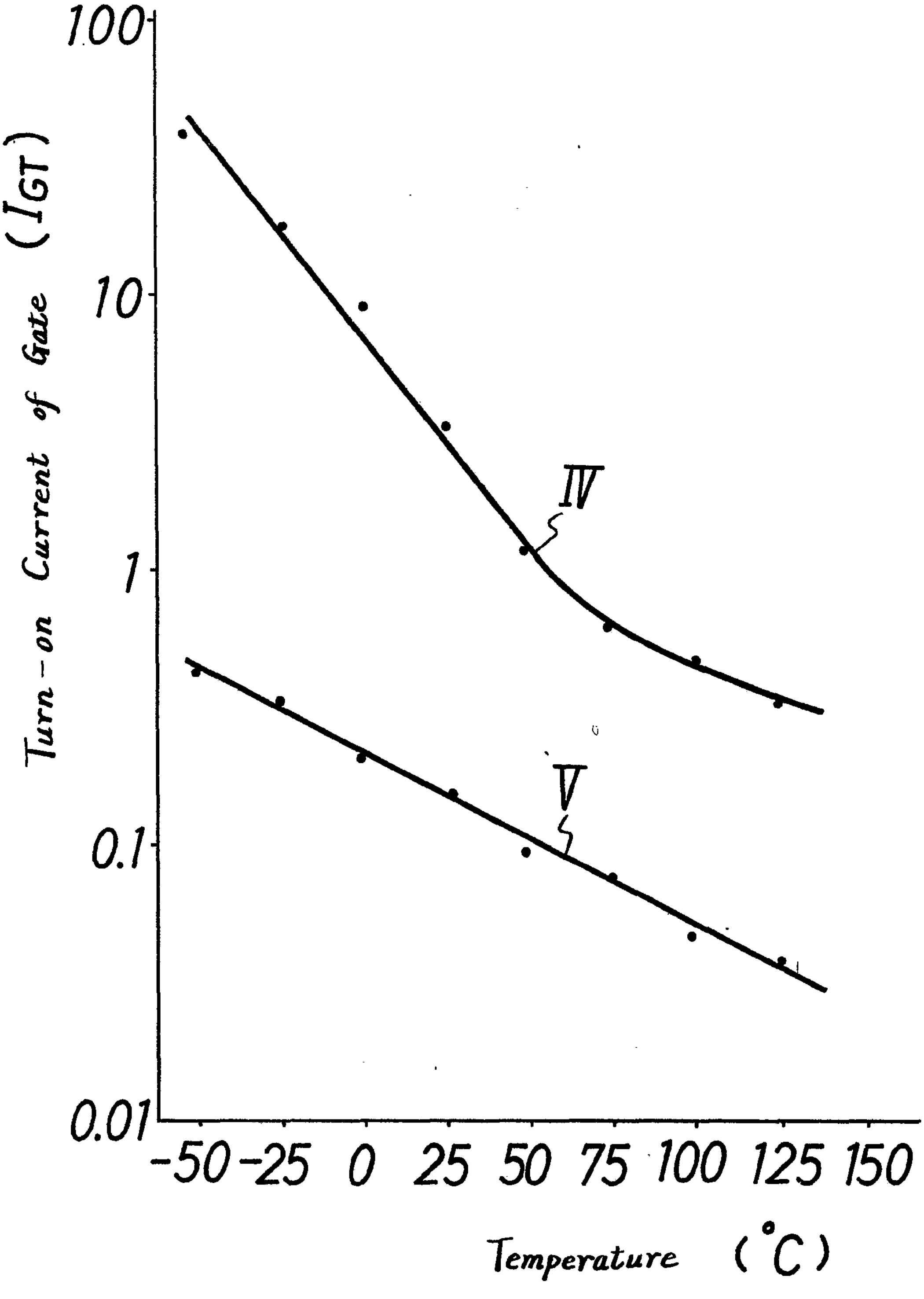
FIG. 3



SPECIFICATION

Ion implantation methods for semiconductor substrates

This invention relates to ion implantation methods for semiconductor substrates, and to semiconductor devices including material so implanted.

In relatively large-power semiconductor devices such as transistors, diodes and thyristors, it is advantageous if the temperature dependency of the life time of minority carriers in the semiconductor material, which is normally crystalline silicon, can be reduced.

US Patent No. 3 953 243 shows the control of the life time by utilising gold. Recently, platinum has been proposed for the same purpose. However, the effectiveness of both gold and platinum is very temperature dependent, and moreover when they are doped into a semiconductor substrate of N or P type conductivity they become an acceptor or donor, with the result that the resistivity of the semiconductor substrate is increased and hence the current capacity of the semiconductor substrate is reduced.

According to the present invention there is provided a method of Fe ion implantation into a semiconductor substrate of N type conductivity, the method comprising the steps of: implanting Fe ions into a semiconductor substrate of N type conductivity through a surface thereof with a dosage of 10^{10} to 10^{15} ions cm^{-2}; and heat-treating said implanted substrate at 850° to 1250°C.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a graph showing a temperature to recovery time characteristic of a diode;

Figure 2 is a graph showing characteristics of a voltage V_F between the anode and cathode of a gate controlled switching element to temperatures; and

Figure 3 is a graph showing a gate turn-on current to temperature characteristic of a similar gate controlled switching element.

In methods according to the invention of iron (Fe) ion implantation into a semiconductor substrate of N type conductivity and to be described, Fe is used as a life time killer to control the life time of minority carriers in a semiconductor crystalline substrate such as a silicon substrate. It is known from for example, Phys. Stat. Sol. (a) 10, K53 and K133 (1972) to use Fe as the life time killer. However, since Fe is easily oxidised, when Fe is vaporised and then diffused as in the prior art, the oxidation of the Fe on vaporisation becomes a problem. In the present case, in order to control the concentration of Fe, which serves as centres of recombination, with high reproducibility, Fe ions are implanted into a semiconductor crystalline substrate by an ion implantation method, and the dosage of implanted ions and the heat-treatment or annealing temperature, that is the diffusing temperature of the implanted ions are controlled to reduce the temperature dependency of the life time of the minority carriers. Since Fe ions are lighter than gold ions, Fe ion implantation can more easily be carried out.

The methods are especially suitable to control the life time of the minority carrier in an N type semiconductor crystalline substrate such as a silicon substrate. Since Fe atoms serve as only a donor in, for example, silicon semiconductor material, the effect of Fe is very different from that of gold and platinum. By way of example, when Fe is doped into an N type silicon semiconductor substrate, since Fe is a donor and hence neutral, this means that the temperature dependency of the life time is very small.

In general, it can be considered that the life time τ is given by the following equation:

$$\tau = \frac{1}{t\sigma v}$$

where Nt represents the density of trap centres, σ is the trap cross-sectional area, and v is the heat velocity.

In general, the temperature dependencies of the factors σ and v are as follows:

$\sigma(T)$ is proportional to $T^{-n}(n=0, 1, 2, ...)$

$v(T)$ is proportional to $T^{\frac{1}{2}}$

where T represents temperature.

Accordingly, the temperature dependency of the life time τ can be expressed as follows:

τ is proportional to

$$T^{n}\frac{1}{2}$$

Fe atoms diffused into, for example, an N type silicon semiconductor form a deep donor level which includes electrons, and so are electrically neutral. The trap cross-sectional area σ of a neutral level is less dependent on temperature. In other words, the temperature dependency of the trap cross-sectional area σ_{Fe} which includes Fe atoms doped thereinto is expressed as follows:

σ_{Fe} is proportional to T^0 to T^{-1}

Therefore, the life time σ_{Fe} of this case is expressed as follows:

σ_{Fe} is proportional to

$$T^{-}\frac{1}{2} \text{ to } \frac{1}{2}$$

The above expression means that the temperature dependency of the life time σ_{Fe} is small.

Now, gold atoms are considered. Gold atoms diffused into an N type silicon semiconductor form a deep acceptor level, and this deep acceptor level traps electrons to become negatively charged, and therefore to trap holes. As the temperature increases, the trap cross-sectional area σ_{Au} decreases. In general, the temperature dependency of the trap cross-sectional area σ_{Au} is expressed as follows:

σ_{Au} is proportional to T^{-2} to T^{-4}

Hence, the temperature dependency of the life time σ_{Au} becomes:

σ_{Au} is proportional to $T^{1.5}$ to $T^{3.5}$

This means that the temperature dependency of the life time σ_{Au} is rather large.

In the present methods, therefore, Fe ions, that is ^{56}Fe ions (or isotope ^{57}Fe ions) are implanted by an ion implantation method into and through the surface of a semiconductor crystalline substrate such as an N type silicon semiconductor substrate, the life time of the minority carriers in which must be controlled. In this case, the dosage of ^{56}Fe ions (or ^{57}Fe ions) is desired to be selected within the range of 1×10^{10} to 1×10^{15} ions cm^{-2}, and more preferably 1×10^{12} to 10^{14} ions cm^{-2}. If the dosage is greater than 1×10^{15} ions cm^{-2}, the trapping of the minority carriers becomes less and hence Fe is deposited. If the dosage is selected less than 1×10^{10} ions cm^{-2}, the effect thereby is reduced. An acceleration energy for the ion implantation of 100 KeV can be used by way of example. The ^{56}Fe ions are produced by reacting metallic iron with CCl_4 or $SnCl_4$ to produce $FeCl_3$, and then the $FeCl_3$ is heated to 400°C to 500°C to be vaporised.

After the ^{56}Fe ions or (^{57}Fe ions) are implanted into the silicon substrate through the surface thereof, the substrate is subjected to an annealing. The annealing temperature is within the range of 850°C to 1250°C, and more preferably 950°C to 1100°C. When the annealing treatment is carried out at high temperature, the trap concentration tends to be reduced.

The deep level formed by Fe ion implantation is different from that formed by the prior art ion diffusion. With the prior art method, a donor type level is formed 0.55 eV under the conduction band and 0.4 eV above the valence band. With the present method, the donor type level is formed 0.58 eV under the conduction band and 0.30 eV above the valence bond. Also, a level is formed 0.27 eV under the conduction band, but the type is not clear.

It is also possible that after the Fe ion implantation, gold or platinum is diffused into the same substrate.

Figure 1 is a graph showing temperature characteristics of the life time of the minority carrier in diodes, made by methods according to the invention, evaluated by the recovery times T_{rr} of the diodes. In the graph of Figure 1, cureves *a, b, c, d, e* and *f* represent the characteristics of diodes made by methods according to the present invention, where the annealing temperature is constant at 1000°C but the dosage of Fe ions is selected as 1×10^{10} ions cm^{-2}, 1×10^{11} ions cm^{-2}, 1×10^{13} ions cm^{-2}, 1×10^{14} ions cm^{-2} and 1×10^{15} ions cm^{-2}, respectively, and a curve *g* represents the characteristic of a prior art diode into which gold is doped. From the graph of Figure 1, it is noted that the temperature characteristic of the recovery time T_{rr} of the diodes made by methods according to the invention is improved as compared with the prior art diode into which gold has been doped.

In experiments, the dosage of Fe ions and the annealing temperature of a diode and a gate controlled switching element (GCS), which have Fe ions doped thereinto by a method according to the present invention, were controlled suitably under the above range. A diode, the recovery time T_{rr} of which is lowered at high temperature or the recovery time T_{rr} of which is not varied within the temperature range of −50°C to 150°C is obtained. In case of the GCS, the voltage V_F between the anode and cathode thereof increases at high temperature, but decreases at low temperature (which tendency is opposite to that of the prior art GCS having gold doped thereinto) or the voltage V_F of which is not changed within the temperature range of −50°C to 150°C.

Figure 2 is a graph showing temperature characteristics of the voltages V_F of a GCS made by a method according to the invention which has Fe doped thereinto, and a prior art GCS having gold doped thereinto. In the graph of Figure 2, a curve I represents the case of a prior art GCS into which gold is diffused at 890°C, and curves II and III represent the cases of GCSs, which have Fe doped thereinto and annealed at temperatures of 950°C and 1000°C, respectively.

Figure 3 is a graph showing the temperature characteristics of the turn-on current I_{GT} of a GCS having Fe doped thereinto by a method according to the invention and that of a prior art GCS having gold doped therein, in which a curve IV represents the case of the prior art GCS into which gold is diffused at 890°C and a curve V represents the case of the GCS made by a method according to the present invention which is annealed at 950°C.

In methods according to the invention as described above, the dosage of the doped Fe can be accurately controlled and hence good reproducibility is obtained.

A bipolar semiconductor device having Fe doped thereinto by an ion implantation method according to the invention has good temperature characteristics compared with a prior art semiconductor device having gold doped thereinto.

Methods according to the invention can advantageously be used for making high-power semiconductor devices. For example, improved temperature characteristics for the collector of an NPN transistor and for the base of an PNP transistor, improve the storage time in the NPN transistor.and the temperature characteristic of the current amplification factor h_{FE} in the PNP transistor. Moreover, the current gain of a power transistor, GCS and silicon controlled rectifier can be controlled, and the switching characteristics of a diode improved.

CLAIMS

1. A method of Fe ion implantation into a semiconductor substrate of N type conductivity, the method comprising the steps of: implanting Fe ions into a semiconductor substrate of N type conductivity through a surface thereof with a dosage of 10^{10} to 10^{15} ions cm^{-2}; and heat-treating said implanted substrate at 850° to 1250°C.

2. A method according to claim 1 wherein said substrate is a silicon substrate.

3. A method according to claim 1 or claim 2 wherein said dosage is within the range 10^{12} to 10^{14} ions cm^{-2}.

4. A method according to claim 1, claim 2 or claim 3 wherein said heat-treating temperature is within the range 950 to 1100°C.

5. A method according to claim 1 and substantially as hereinbefore described.

6. A semiconductor device including semiconductor material implanted by a method according to any one of the preceding claims.

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