# DISTRIBUTED INTELLIGENCE AT CELLO

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Abstract

This paper describes the use of distributed intelligence at CELLO, a large $4\pi$ detector at PETRA. Besides special purpose hardware processors for online calibration and reformatting of data, several microcomputers are used for monitoring and testing the various detector components.

## I. INTRODUCTION

During the planning stage of a large experiment an obvious question is : which microprocessors/microcomputers/minicomputers are the most useful for our experiment taking into account speed, maximum memory size, available manpower and expertise for hard- and software development, cost, timescale, etc. ?
In this paper we discuss this question as it was posed about five years ago for CELLO, a large 4 detector at the $e^+e^-$ storage ring PETRA. We then discuss the resulting data acquisition system and the experience obtained with it during one year of operation at PETRA.

The possible application of processors can be divided in three classes :

1. very fast processors needed for trigger purposes
2. fast processors needed for online data calibration and reformatting
3. slow processors needed for testing and monitoring purposes.

In this paper we will restrict ourselves to applications in the last 2 categories, since the CELLO trigger will be discussed by Dr. Schröder in a separate contribution to this conference.

In section 2 we formulate the requirements made for CELLO. In section 3 we describe the resulting data acquisition system with its distributed intelligence up to the point where the data is delivered to the online minicomputers, which transfer them to the IBM of the DESY computer center for storage on magnetic tape.

## II. REQUIREMENTS

From the computer scientist's point of view CELLO is a conglomerate of many different detectors[1] (tracking detector, liquid argon detector,

muon identifier, forward detector, and others) with about 2o ooo channels to be read. The testing, monitoring and calibration of such a large detector is a formidable task, which can be solved most easily with what is called distributed intelligence, since a central computer or, even worse, the people who know how to program it, would be overloaded. We will now discuss the requirements and possible choices of processors for two different applications.

A) Very fast processors needed for online transformation and reformatting of data.

The processors for such operations have to perform very simple operations like multiplying, adding or subtracting 2 numbers. Simple steering logic together with muliplier and adder circuits are much more attractive than fast microprocessors, both for reasons of speed and ease of interfacing. For example a single multiplier chip multiplies two 12 bit numbers in about 1oo ns. A typical example of such a processor has been shown schematically in Fig. 1. More details and applications of these kind of special purpose hardware processors will be discussed herafter.

B) Processors needed for testing, calibration and monitoring purposes.

The main requirements for these processors can be summarized as follows :

a) Capability to operate as a stand alone processor, thus allowing testing independently from the central computer.
b) Integration in the data acquisition such that monitoring is also possible during datataking.
c) Powerful enough to monitor and calibrate a large number of ADC's or TDC's.
d) Programmable in a higher level language so the programming load can be distributed over a large number of people.

The microcomputers chosen at CELLO for these purposes were a Z8o, 2 Mitra's and 6 LSI-11's. All are equipped with 2 floppy discs and a terminal. One LSI-11 has been equipped additionally with a normal disc. These microcomputers have been programmed mainly in FORTRAN. The popularity of the LSI-11 stems from the following facts :

a) a relatively low price : ~ $ 1o,ooo for a 16 bit LSI-11/2 CPU, 32 K x 16 bit memory, 2 double density floppy discs, CAMAC interface, and a teletype interface;
b) availability of commercial CAMAC interfaces for A2-Type crate controllers which allow more than one processor to have access to the same dataway[2];

c) software compatability with the PDP11 which means one does not have to develop a histogram package, graphic package, and an interactive CAMAC compiler (CATY);
d) two compatible LSI-11 versions exist : LSI-11/2 and LSI-11/23. The latter has an 18 bit address bus and thus can address up to 128 K x 16 bit memory. Furthermore, the latter is about twice as fast as the former;
e) all the PDP11 peripherals can be used..

## III. DATA ACQUISITION SYSTEM

A sketch of the CELLO data acquisition with it's distributed intelligence has been given in Fig. 2. The ROMULUS system is used for data compaction. Each detector has it's own ROMULUS branch driver (ROBD) located in a so-called master crate, equipped with an A2- type crate controller which allows ROBD readout either by the central computer or the microcomputer.

The data acquisition proceeds as follows : as soon as the trigger has interrupted the central computer a start signal is sent to every ROBD. Time delays needed for ADC- or TDC-conversion are generated by hardware via the inhibit input of the ROBD. Then each ROBD starts to collect the data of the corresponding detector component in their own FIFO memory and the central computer starts to read the 8 FIFO's of 8 ROBD's using the FIFO-READY signal for DMA synchronization.

In front of the ROBD's are located the various special purpose hardware processors:

a) the BAG[3] (Block Address Generator). This processor transforms CAMAC crate-, station- and subaddresses into continuously increasing addresses up to maximum blocksize, where the blocksize is given by the available address bits in the 16 bit dataword (e.g. 64 for a 1o bit ADC, 256 for an 8 bit ADC). Then the address and data can be transferred in a single 16 bit word. The conversion time is less than the cycle time of the ROBD (2 $\mu$s) thus allowing the conversion of the incoming word during the output of the previous word.
b) Ax + b processors[4]. These processors can transform the data from up to 8o96 ADC's or TDC's (8 to 12 bit) with a conversion time of less than 2 $\mu$s per word. Here again the read cycles overlap in time with the data conversion. This processor has been shown schematically in Fig. 1. The calibration constants for these processors can be determined and loaded either by the central computer or the microcomputer attached to that detector component.

c) The ACE[5] (Anode Cluster Encoder). This processor combines up to 8 clusters of proportional chamber hits on neighbouring wires into a single address with an additional 3 bits indicating the length of the cluster.

The microcomputers can calibrate and test the equipment as stand alone units or monitor the data during datataking. For the latter purpose spy modules[6] are used. These are CAMAC memories which spy on the dataway during ROBD readout thus enabling a second reading of the data by another controller via the A2 crate controller. This allows the microcomputer to produce histograms, wiremaps, and event displays during datataking.

SUMMARY

The concept of stand alone microcomputers which are able to access the data also during datataking has been found to be very useful, firstly because the detector builders can test, calibrate, and monitor their detector components independently of the other detector components and the central computer, and secondly because the datataking does not depend on the status of the microcomputers. Furthermore, the A2 crate controller allows easy communication between the various processors via standard CAMAC memories.

Although it may look rather expensive to equip each detector component with a complete microcomputer system, the total price of the distributed intelligence is less than 1% of the total cost of the detector. This together with the fact that microcomputers are much easier to use than microprocessors justifies the use of the first ones instead of the second ones.

The role of microprocessors has been further reduced in $e^+e^-$-physics experiments by the advent of cheap, compact memories which make the use of look-up table techniques for trigger purposes much more attractive than microprocessors, since many possible combinations can be searched for in parallel in large memories. Also data transformations can be done much faster with special purpose hardware processors than with microprocessors, as discussed in section II.

To conclude let us ask the question : what would you do different if you would start again ? The answer : nothing except to replace the ROMULUS system by the REMUS system, and the LSI-11/2 by the LSI-11/23 and a few things I have no time to talk about.

REFERENCES

1) CELLO - A new detector at Petra, DESY 80/128.
2) Eg. Standard Engineering, Fremont, CA. 94538, USA.
3) Designed and build by R.Chase, Orsay, and J.P. Denance, Univ. of Paris VI.
4) Designed by P. Bernaudin, Orsay.
5) Designed by R. Chase, Orsay.
6) Designed by K. Truong, Orsay.

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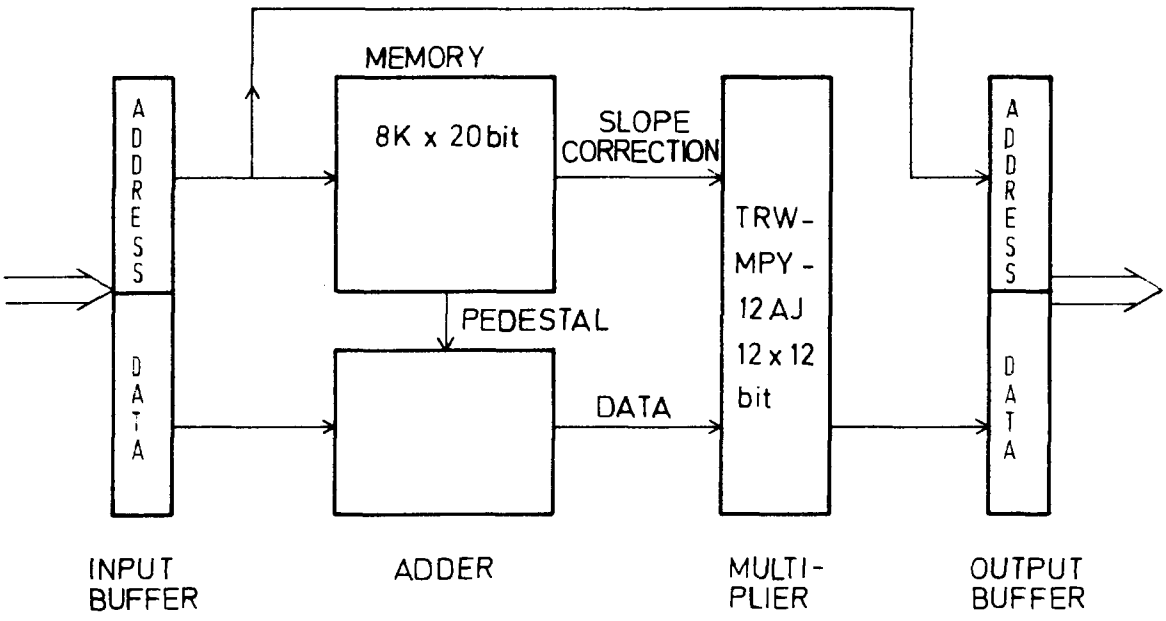


AX + B PROCESSOR

Fig. 1 Example of special purpose hardware processor which can transform the data from up to 8096 ADC's linearly thus correcting slope and pedestal simultaneously

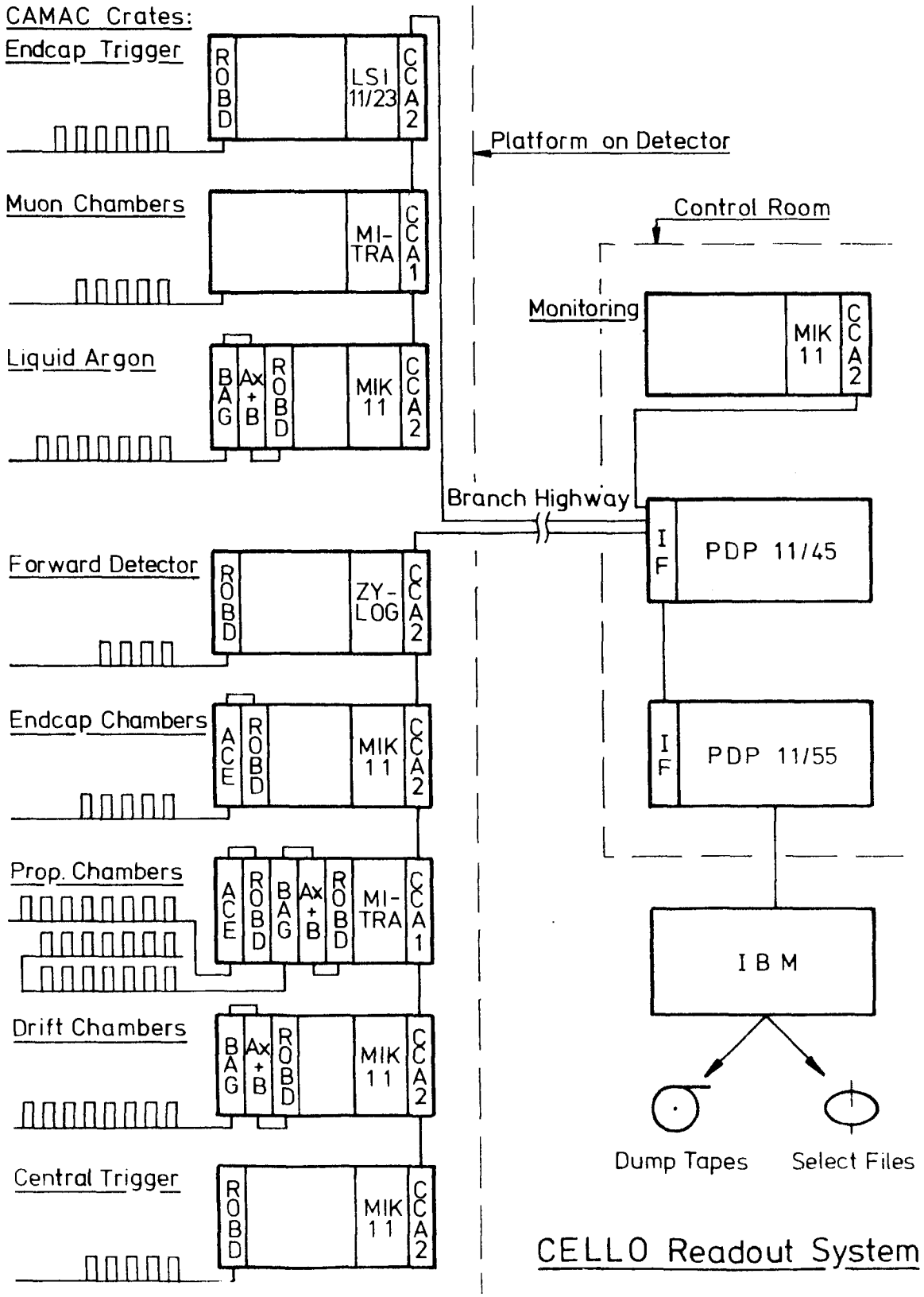


Fig. 2 Schematic layout of the CELLO data acquisition system