MICROPROCESSOR BASED TECHNIQUES AT C E S R

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Microprocessor based systems succesfully used in connection with the High Energy Physics experimental program at the Cornell Electron Storage Ring are described. The multiprocessor calibration system for the CUSB calorimeter is analyzed in view of present and future applications.

INTRODUCTION

High energy physics is a field where, partly due to increasingly complex accelerators and detectors, the need for efficient control and data acquisition has become an ever more pressing requirement. One approach to this problem lies in the use of microprocessor systems which are specialized to particular tasks. Thanks to advances in large scale integration, microprocessors have become competitive computing devices in many situations. The distribution of tasks among several small processors, as opposed to handling them on a time sharing basis within a large computer, can offer increased reliability, efficiency and flexibility with the added advantage of low cost.

The Cornell Electron Storage Ring (C E S R) has been operating since the fall of 1979, providing electron-positron annihilations at center of mass energies in the region of 10 GeV. There are two interaction regions at CESR. The south one is surrounded by the CLEO detector which is operated by a collaboration of physicists from Cornell,Harvard,Rochester,Rutgers, Syracuse,Vanderbilt Universities. Experiments in the north area are being conducted by the CUSB collaboration of Columbia,StonyBrook,Louisiana universities and Munich MPI. The Physics program at CESR centers on the study of the Upsilon particles containing the b ('bottom' or 'beauty') quark both below and above threshold for 'bare' flavor production.

MICROPROCESSORS AT C E S R

The storage ring is completely under computer control and it is in connection with its operation that we have started making use of microprocessors. Here one has the situation of a multiplicity of tasks which may be handled by dedicated computers running in parallel that quickly produce results for further utilization. The system has been built on a bus structure which can accomodate a large number of microprocessors. The main bus (X-bus, fig.1)is driven by a PDP-11 and links together up to 16 independently addressable crates. Furthermore, each crate has an internal bus (the C-bus) to which microprocessors are interfaced. An example[1] of a particular task handled on this system is using a Z-80 8-bit μP as a knob scanner. It allows the operators to change the values of control program variables by simply turning a knob. Another example is the Z-80 μP based motor driven devices controller for the RF phase shifters. Microprogrammed processors of the AM2900 family are extensively employed for the south area experiment (CLEO) data taking.

MICROPROCESSORS IN FUTURE EXPERIMENTS

As the center of mass energy available to high energy physics experiments inreases and for Z^0 physics the detectors have to face higher multiplicity and in general more complex final states. Calorimetry is a possible answer that is becoming more and more attractive. The resolution of energy measuring detectors improves as a function of the energy while momentum measurements become more difficult and stronger magnetic fields are required. Combinatorial background makes practically impossible the reconstruction of intermediate state masses in hadronic events with charged multiplicity larger than twenty.

Another clear trend is towards higher trigger rates together with a larger amount of data words to be read for each event. I believe that to design a new experiment the maximum attention and study have to be devoted to the problem of how to handle the information produced, how much computing power is needed and which configurations of computers have to be chosen. Microprocessors and especially multiprocessing systems with a large number of microcomputers can represent a solution. To understand more about performance and reliability of such systems, they have to be carefully tested in the environment of running experiments.

MICROPROCESSORS AND CALORIMETRY

The north area experiment CUSB is an electromagnetic calorimeter based on higly segmented arrays of sodium iodide (NaI) crystals and lead glass. A total of 756 energy measuring elements, 332(in the central detector) plus 168(in the end caps) NaI and 256 Pb-glass Cerenkov counters give information about energy deposition of electromagnetic showers and charged particles. The precise calibration of every component of the detector is a fundamental requirement to attain good resolution in particular when showers spread over many adjacent crystals. Furthermore this uniformity has to be kept over running periods of several months. The calibration is made possible by having a small radioactive source (gamma's from Cs^{137} or Co^{60}) attached to each NaI crystal and pulsed light emitting diodes in optical contact with the lead glass. In both cases one has a reference source of known intensity.

The microprocessor based system I am going to describe provides a way of calibrating continuously and automatically the whole detector.

MULTIPROCESSOR DEVELOPMENT SYSTEM

The 8086 family of 16-bit microprocessors produced by Intel offers several features that are particularly interesting in view of applications involving multiprocessing besides a rather wide variety of development tools both in hardware: single board computers, interfaces, I/O devices and in software: operating systems, program libraries,language translators[2]. The Intellec Series III development system has been chosen; on its internal Multibus (multi stands for multimaster configuration) two microprocessors run in parallel (fig.2): an 8080 is essentially an I/O manager servicing the requests of an 8086 which runs the disk operating system. For storage of programs and data files two flexible disk and one fixed hard disk are interfaced to the Multibus allowing access to 7 Mbytes of information on the hard disk and 1/2 Mbytes on each removable flexible disk . In this configuration program developing and debugging turns out to be very easy. PLM/86 is a powerful high level language

which also allows a good control of the hardware; the compiler produces linkable and relocatable object code that can be run on the MDS or loaded in shared memory or downloaded to all the external microprocessors. The Intel 8086 CPU presents a rather efficient structure: 16-bit data path, 20-bit addressability (1 Mbyte of memory and 64 Kbyte of I/O ports), 6-byte instruction prefetching, maskable and non maskable interrupts.

The System Design Kit SDK86 is the single board microcomputer of very reasonable cost (about 1 K$ per unit) based on the 8086 CPU that has been adopted for the multiprocessors calibration system; it is simple to assemble and offers a programmable 8-levels priority resolver, bus arbitrator and programmable serial and parallel interfaces : all on board.

MULTIPROCESSOR CALIBRATION SYSTEM FOR C U S B

The signals from the photomultipliers, besides going to the data taking section of the CUSB experiment (fig.3), are 'picked off' by non loading differential input/output amplifiers and through a computer controllable multiplexer are sent to a 16 channel gated ADC for analog to digital conversion. Digitized numbers proportional to the signal pulse hight reach the microprocessor which controls data flow, performs pedestal subtraction and updates histograms residing in the 256 Kbyte shared memory. In parallel another 8086 is performing statistical analysis of the same spectra determining which channels require more accumulation and which are ready to be fully utilized. When the histogram is 'ready' it is copied into private memory. A typical spectrum is shown in fig.4. Then a peak finding subroutine estimates the background to be subtracted and fits the remaining curve with a gaussian.

The center of the fitting gaussian becomes the calibration point for the corresponding phototube and it is stored in memory for further use. If anomalies are detected, warning messages are sent to the console and spoken by the DT1050 Digitalker[3], a speech synthesis kit, that has been connected to a programmable interface unit of the microprocessor[4].

In order to guarantee a good precision of the calculations, floating-point arithmetic is used. The system will accomodate the 8087 Numeric Data Processor which is expected to be released by Intel in few weeks. It is actually a coprocessor that extends the instruction set of the 8086 CPU and performs 'hardware' arithmetic on up to 64 bit formatted real numbers in 30÷50 μsec , in parallel to the CPU. Waiting for the chip to come the software emulator E8087 is used.

As soon as the calibration points for the 756 elements of the detector are available, a comparison with the previous set of values is made. If the difference is significant a change of gain is calculated in terms of increase or decrease of high voltage. An interface between the Multibus and the programmable high voltage power supplies,that drive the photomultipliers,is being built to allow the microprocessor itself to automatically set the new high voltage and compensate for gain fluctuations as revealed by the shift of the peak.

The whole procedure, that takes about two hours to complete, is a closed loop and the detector keeps calibrating itself as long as it is running.

EXPANSION OF THE SYSTEM

The calibration system has shown that the advertised flexibility and reliability of multimicroprocessing is real. To put under more stringent test the configuration, the system

may be extended so that data taking itself can be accomplished by microprocessors. A new arrangement is being designed in which high parallelism allows efficient data taking and monitoring with fail safe characteristics: if one microprocessor is not avalilable, another takes over. The Multibus is going to be linked to the'transport system',the core of data flow in CUSB, so as to connect the microprocessors to the on-line computers PDP-11 and VAX.

ACKNOWLEDGEMENTS

I would like to thank Robert Dean Shamberger for the invaluable contributions and Paolo Franzini, Juliet Lee-Franzini, George Blanar, Garry Levman, Mike Sivertz, Mike Tuts, Turhan Rahman, Serge Lusin and Lee Spencer for useful discussions and help in the preparation of this talk.

*This work is supported in part by National Science Foundation.

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2) The 8086 user's manual. Intel Corporation, 1979.
(Intel Intellec Multibus are trade marks of Intel Co.)

3) Digitalker is a trade mark of National Semiconductor Co.

4) Peripheral design handbook. Intel Co., 1980.

5) Numerics Supplement (NDP8087) to 8086 family, Intel Co.,1980

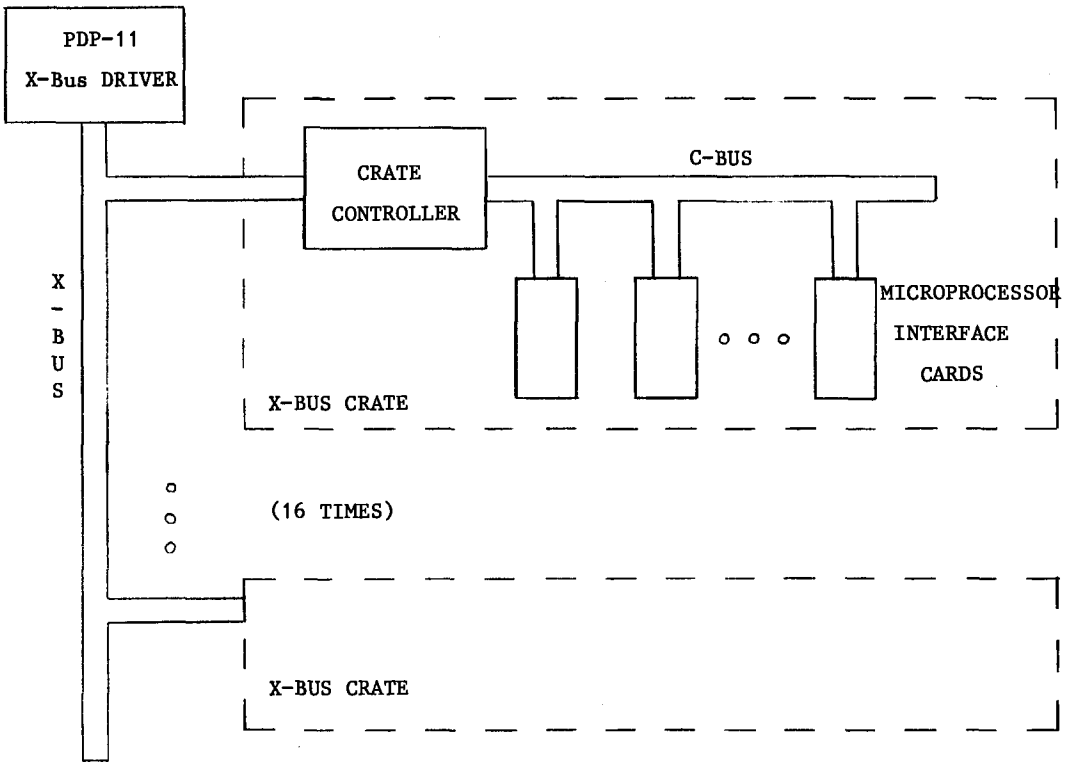

Fig. 1 C E S R X-BUS SYSTEM

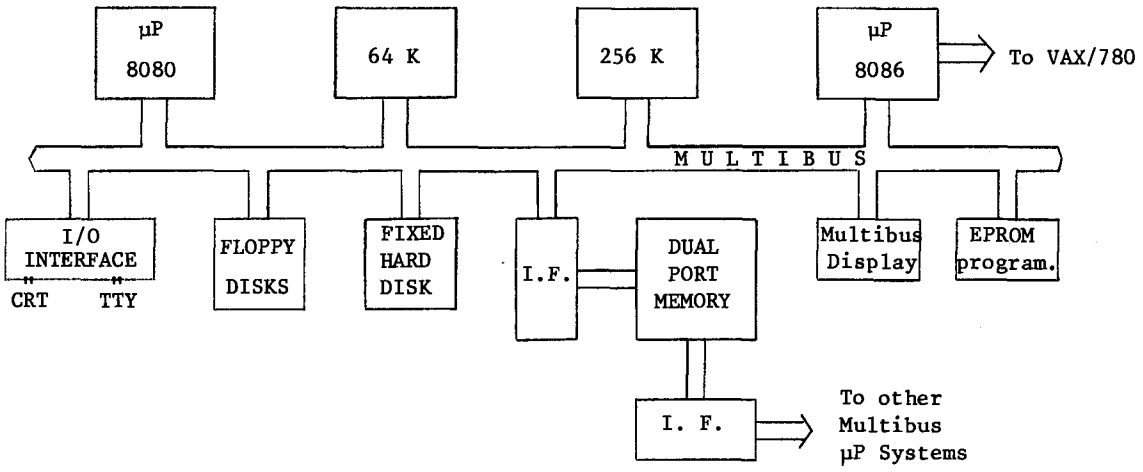

Fig. 2 Microprocessor Development System

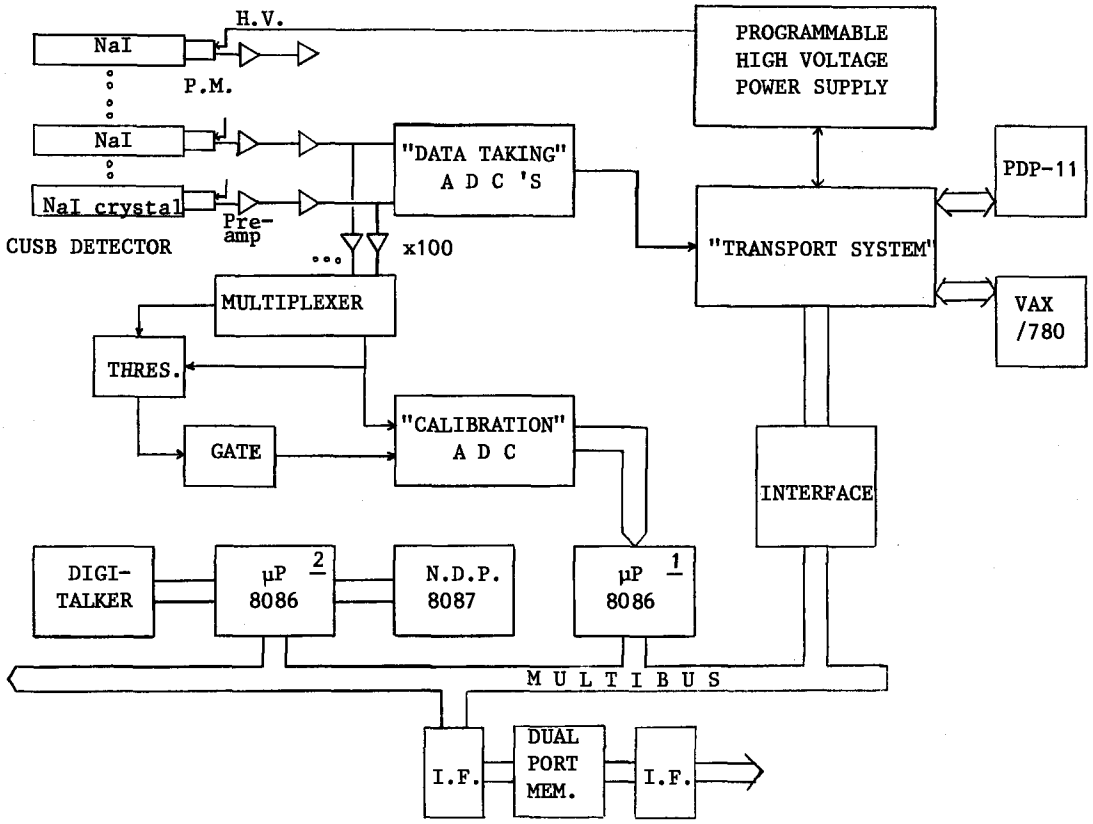

Fig. 3 Multiprocessor Calibration System for CUSB

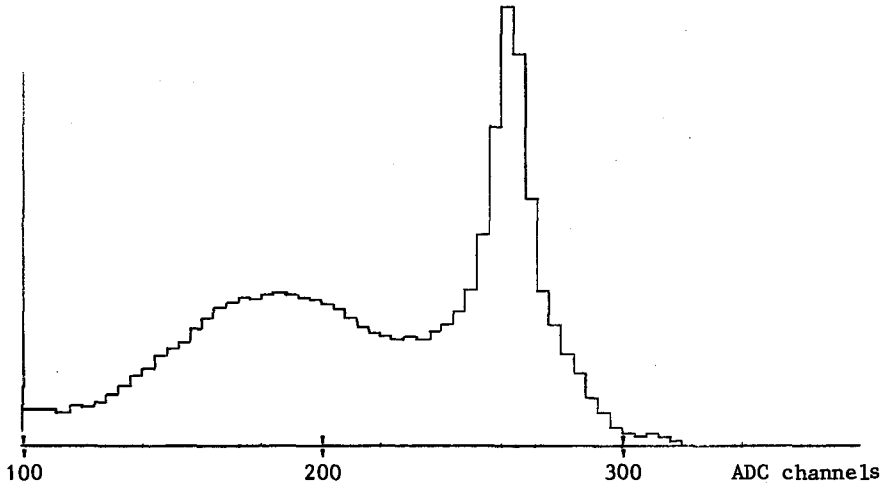

Fig. 4 Typical calibration spectrum from ^{137}Cs