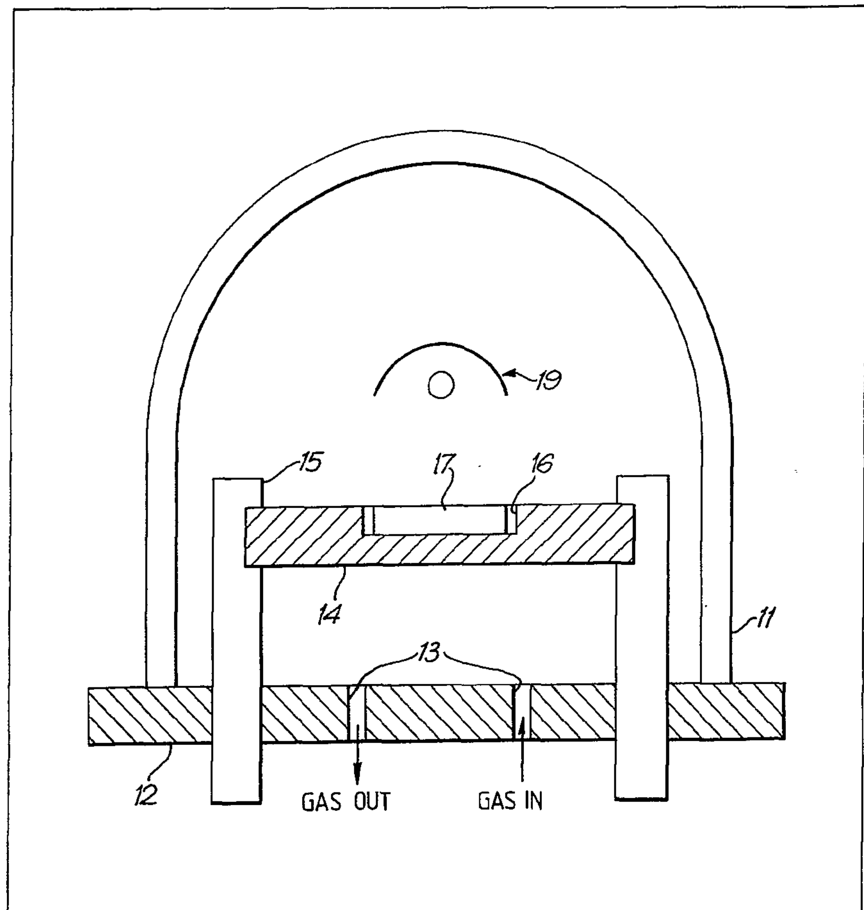
(12) UK Patent Application (19) GB (11) 2 060 998 A

(21) Application No **7936041**
(22) Date of filing **17 Oct 1979**
(43) Application published **7 May 1981**
(51) **INT CL^3 H01L 21/265 21/324**
(52) Domestic classification H1K 2S20 2S2D 3E5A 3F 8VE 9D1 9N2 LCA
(56) Documents cited
GB 1384935
GB 1239043
GB 1205288
US 4151008A
(58) Field of search **H1K**
(71) Applicants
ITT Industries Limited, 190 Strand, London, WC2R 1DU, England.
(72) Inventors
John Michael Young, Peter Denis Scovell.
(74) Agents
S.R. Capsey, ITT-UK Patent Department, Maidstone Road, Foots Cray, Sidcup, DA14 5HT, England.

(54) Semiconductor annealing

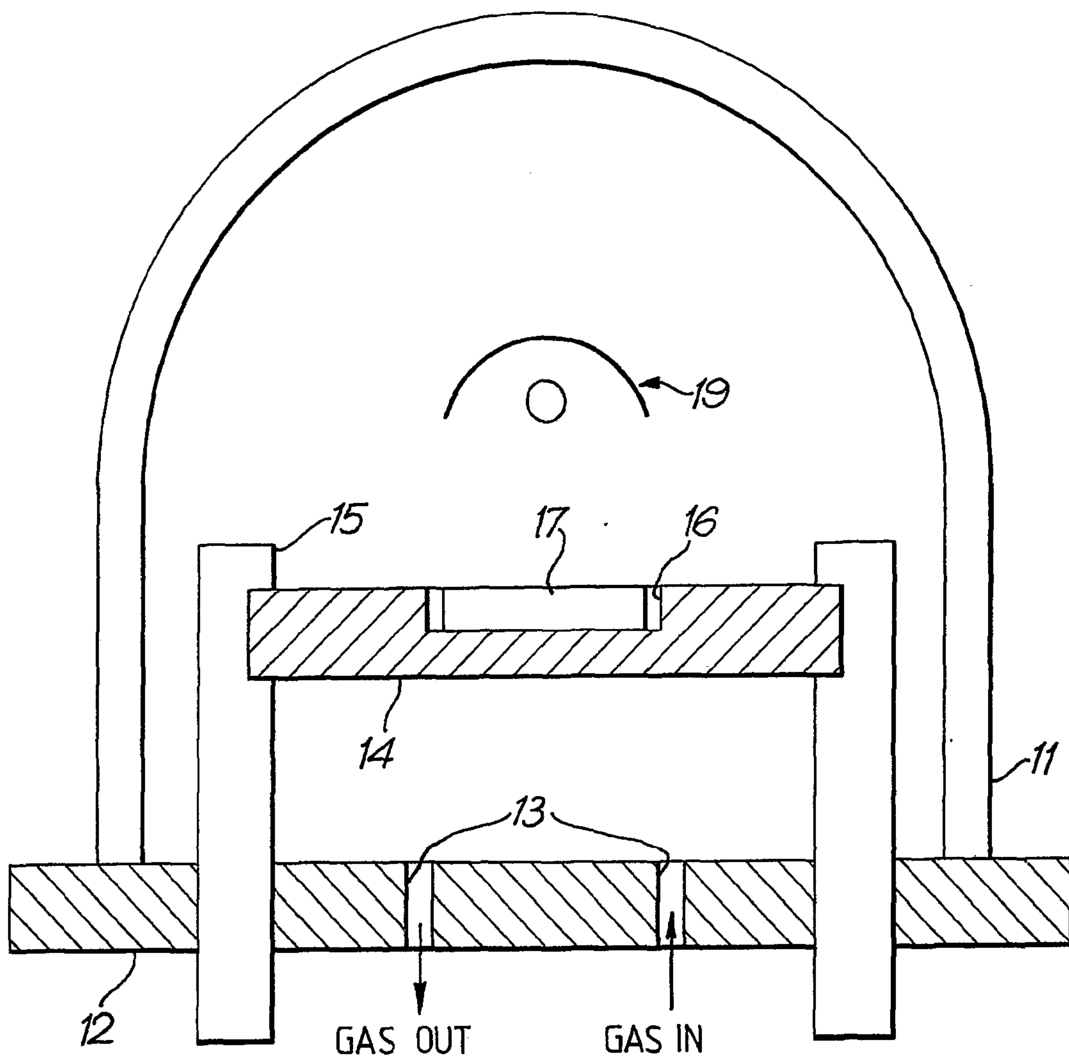
(57) A process for annealing crystal damage in ion implanted semiconductor devices in which the device is rapidly heated to a temperature between 450 and 600°C and allowed to cool. It has been found that such heating of the device to these relatively low temperatures results in rapid annealing. In one application the device (17) may be heated on a graphite element (14) mounted between electrodes (15) in an inert atmosphere in a chamber (11). The process may be enhanced by the application of optical radiation from a Xenon lamp (19).



The drawing(s) originally filed was/were informal and the print here reproduced is taken from a later filed formal copy.

GB 2 060 998 A

2060998



SPECIFICATION

Semiconductor annealing

This invention relates to processing for annealing ion implantation damage in semiconductor devices and to apparatus for effecting such annealing.

Ion implantation has become a widely used technique in the fabrication of semiconductor devices. In this technique a semiconductor body is bombarded in vacuum with ions of an element with which the semiconductor body is to be doped. These ions penetrate the semiconductor crystal lattice and form a buried layer the depth of which is determinded by the original ion energy.

During the ion implantation process the semiconductor crystal lattice is damaged and it is therefore necessary to anneal out this damage before further semiconductor processing can be effected. Conventionally this is done by maintaining the semiconductor body at an elevated temperature, e.g. 600 to 900°C for an extended time during which recrystallisation occurs. Such a process is of course time consuming and limits the rate of device throughput. Further, the high temperatures and extended times involved can lead to undesirable diffusion of the dopant.

The object of the invention is to minimise or to overcome this disadvantage.

According to the invention there is provided a process for annealing an ion damaged semiconductor body, including pulse heating the body to a temperature within the range in which the sheet resistivity of the semiconductor falls to a minimum value.

We have found that the relatively low temperature annealing process is very rapid as compared to the conventional high temperature process. We have also found that the sheet resistivity of an ion implanted silicon body is not a linear function of the annealing temperature, but has a definite minimum value at a temperature between 450 and 600°C, typically 540°C. The sheet resistivity shows a slow rise with increasing temperature up to about 750°C and then falls again at 800 to 900°C, this latter temperature being that employed in the conventional annealing process. Furthermore, we have established that, at the relatively low temperatures we employ, a rapid excursion to the annealing temperature is sufficient to effect the desired annealing process.

Embodiments of the invention will now be described with reference to the accompanying drawings in which the single figure is a schematic diagram of a semiconductor pulse annealing apparatus.

Referring to the drawing the apparatus includes a chamber, e.g. a glass bell jar 11, supported on a base plate 12 provided with openings 13 whereby the bell jar may be purged with an inert gas, e.g. nitrogen. Within the bell jar 11 a conductive, typically graphite, heater element 14 is mounted between a pair of electrodes 15. The heater element 14 is provided with a circular recess 16 of suitable dimensions for receiving a semiconductor wafer 17 to be annealed. The apparatus may also include a high power Xenon lamp 19 mounted above the heater element 14.

A silicon process wafer 17 to be annealed is placed in the recess 16 in the heater element 14, and the chamber 11 is purged with inert gas via openings 13. A heavy current, typically 100 - 200 amp, is passed through the element 14 so as to raise its temperature and the temperature of the wafer from ambient to between 500 and 600°C. This temperature rise should be achieved rapidly and the heater element 14 should therefore have a low thermal mass. We have found that a temperature rise to 500°C can be achieved within 20 to 30 seconds. When the element 14 has reached the desired temperature the current is switched off and the element and wafer are allowed to cool. We have found that ion implanted silicon wafers treated to such a temperature profile anneal rapidly. The optimum annealing temperature may depend on the nature of the implanted ion and the extend of the crystal damage. In practice this temperature may be determined empirically. In a typical process employing 30 ohm cm single crystal polished silicon implanted with 150 keV arsenic ions to a level of 6×10^{15} cm^{-2} it was found that annealing was effected by such a pulse heating to 540°C, the maximum temperature being maintained for 3 seconds.

Exposure of a silicon wafer to ion implantation produces a damaged surface layer which can be observed from the optical interference colour it produces. The visual appearance of such a silicon surface is similar to that of a metal with a very thin surface oxide layer. When the silicon is annealed the surface damage is repaired and the interference colour therefore disappears. Using the low temperature thermal pulse technique described herein the annealing process can be followed by observing the wafer surface through a suitably placed long focus misroscope.

In some applications the thermal pulse technique may be supplemented by exposing the wafer 14 to radiation from a high power Xenon lamp 19. In such an arrangement the heater element 14 is raised to a somewhat lower temperature than before, the final annealing then being achieved by optical pulses from the Xenon lamp.

The annealing process is not of course limited to the apparatus described in the accompanying drawing. It is merely necessary to provide some means whereby the semiconductor body is heated rapidly to the desired annealing temperature. Thus, in a continuous process, a plurality of process wafers may be traversed rapidly through a furnace, the furnace temperature and the wafer throughput being such that the desired temperature pulse excursion is obtained. In other applications the wafer may be placed for a predetermined time on a hot plate of a material which does not contaminate the semiconductor.

The following example illustrates the invention:

Example:

A series of 3-inch Czochralski grown p-type (100) 30 ohm cm single crystal silicon wafer was bombarded with arsenic ions at an average energy of 150 keV using an electrostatically scanned beam to produce a sub-surface doping level of 6×10^{15} cm^{-2}. One set of the wafers was treated to a conventional furnace process at a temperature of 650°C for 30 minutes.

The remaining wafers were treated to the pulse annealing process described herein. Each wafer was heated to a temperature of 540°C within 30 seconds, the temperature being maintained at 540°C for 3 seconds. The sheet resistivity, indicative of the efficiency of the annealing process, was determined for both sets of wafers, the results being summarised in the following table:

Anneal Process	Sheet Resistivity ohms/square
Furnace 650°C 30 min.	39.3 ± 0.2
Pulse 540°C 3 min.	30.8 ± 0.2.

These results show that the pulse annealing technique described herein provides effective annealing in a far shorter period of time than the conventional high temperature furnace technique. Also, by operating within the low temperature end of the annealing/temperature curve as against the conventional techniques which operate at the high temperature end of the curve, undesirable diffusion of the implanted and other dopants, if any, is avoided.

CLAIMS

1. A process for annealing an ion damaged semiconductor body, including pulse heating the body to a temperature within the region in which the semiconductor sheet resistivity falls to a minimum value.
2. A process for annealing an ion damaged semiconductor body, including contacting the body with a heater element of low thermal mass, pulse heating the body by raising the temperature of the heater element and the body to 450 to 600°C so as to effect annealing, and allowing the element and the body to cool.
3. A process as claimed in claim 1 or 2, and in which the semiconductor is silicon.
4. A process as claimed in claim 3, and in which the semiconductor body is ion implanted with arsenic.
5. A process as claimed in claim 1, 2, 3 or 4, and in which the temperature is raised to 450 to 600°C within 20 to 30 seconds.
6. A process as claimed in claim 5, and wherein the temperature of the body is maintained at 540°C for 3 seconds.
7. A process as claimed in any one of claims 1 to 6, and in which the thermal treatment of the body is supplemented by optical radiation.
8. A semiconductor annealing process substantially as described herein with reference to the accompanying drawing.
9. A semiconductor body annealed by a process as claimed in any one of claims 1 to 8.
10. A semiconductor annealing apparatus substantially as described herein with reference to the accompanying drawing.

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1981.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.