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THE EFFECT OF THE GATE ELECTRODE ON THE C-V CHARACTERISTICS OF THE STRUCTURE M-TmF₃-SiO₂-Si *

R.R. Basily ** International Centre for Theoretical Physics, Trieste, Italy.

ABSTRACT

The C-V characteristics of the structure M-TmF₃-SiO₂-Si , thermally treated at a temperature of 300° C for 15 minutes, were investigated. At higher temperatures of about 150° C, the hysteresis of the C-V characteristics is completely absent, whereas at room temperature hysteresis depends on the applied voltage and on the material of the gate electrode. The dependence of the flat band voltage shift on the applied voltage, the thickness of SiO₂ layer and the material of the gate electrode.

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** Permanent address: Department of Basic Science, Faculty of Engineering, Ain Shams University, Cairo, Egypt. The C-V characteristics of the structure M-TmF₃-SiO₂-Si with a gate electrode from different materials: AL, Ni and Au, were investigated. The method of preparation of the structure was explained in Ref.1. All structures under investigation were thermally treated at 300° C for 15 minutes. The thermal treatment leads to rearrangement of the structure of the dielectric films and to complete absence of hysteresis of the C-V characteristics at higher temperature of about 150°C. However, at room temperature, it was observed that the C-V hysteresis behaviour depends on the applied voltage, on the thickness of SiO₂ layer and on the material of the gate electrode. These dependences are illustrated in Figs. 1 and 2, where the flat band voltage shift ΔV_{FB} is plotted against the bias applied voltage to the metallic electrode V_{ap} .

Our results agree with the point of view given by Tsujide [2], that not only the material of the electrode, but also the metal preparation process affect the dependence of $\Delta V_{\rm FB}^{}$ on V $_{\rm ap}^{}$. In agreement with the proposal of Tsujide [3], the increase of the absolute value of $\Delta V_{\rm FB}$ with increasing V_{aD} is due to the tunneling of the electrons through the SiO₂ layer and their capture on the interface surface of the dielectrics or by electron migration from the traps. The decrease of absolute value of $\Delta V_{\rm FB}$ by increasing the absolute value of V at high absolute values of V is due to the aptunneling of electrons through the TmF, layer. As can be seen from Fig.3, where we have shown the dependence of the charge density of the fast surface state Q_{ss} on the band bending V_{s} where the SiO₂ layer has a thickness of 100 A, the value and sign of Q_{ac} depend on the material of the electrode. This effect may be due to the dependence of the state of the surface interface of the dielectrics and form of tunnel barrier near that surface on the material of the gate electrode. This dependence does not appear at high negative values of V when the thickness of the SiO_{p} layer is large (Fig.2).

The study of the dependence of surface charge density on the time of bias-temperature treatment shows that the surface charge density is stabilized in the first 30 minutes of the treatment and practically does not change when the treatment is applied for one hour.

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<u>Fig.2</u> Flat band voltage shift as a function of applied bias of the structure with SiO₂ layer thickness = 500 A . 1 - Au electrode, 2 - Ni electrode, 3 - Al electrode.



<u>Fig.1</u> Flat band voltage shift as a function of applied bias of the structure with SiO₂ layer thickness \pm 50 A . 1 - Au electrode, 2 - Ni electrode, 3 - Al electrode.



<u>Fig.3</u> Fast surface state Q_{ss} as a function of band bending V_s . Thickness of SiO₂ layer = 100 A. 1 - Au electrode, 2 - Ni electrode, 3 - AL electrode.

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