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(54) INTEGRATED CIRCUIT STRUCTURE

(71) We, STANDARD MICROSYSTEMS CORPORATION, a corporation organized and existing under the laws of the State of Delaware, United States of America, of 35 Marcus Boulevard, Hauppauge, L.I., New York 11787, United States of America do hereby declare the invention, for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:

The present invention relates to integrated circuit structures.

Recent developments in MOS (metal-oxide-silicon) technology have made possible the fabrication of a multiplicity of devices, such as FET's, in a small area, for use in such products as pocket calculators and microprocessors. One of the major components of these products is the read-only memory (ROM) in which a plurality (for example, 4,096 or 8,192) bits of data is stored or programmed in a preset matrix pattern. The stored data in the ROM may be employed, for example, to control the operation of other stages of the microprocessor, calculator, or the like in a known manner.

In the conventional MOS ROM each data bit is established by a single field-effect transistor (FET) arranged with the other data-storing FETS in an array or matrix consisting of intersecting rows and columns. The intersection of a row and a column defines a data location. The data stored at each location, to wit, a logic "1" or a logic "0", is determined by the electrical characteristics of the FET at each of the data locations. Thus, an FET which is conductive upon the application of a gate signal may define a logic "1", and an FET that cannot be made conductive upon the application of a gate signal may define a logic "0" signal.

The selective modification of the electrical characteristics of the FETS to establish the desired data-storage pattern in a ROM is conventionally achieved during one of the early (first or second photolithographic) stages of fabrication, by performing a photolithographic process using a mask conforming to the desired program or data pattern. Typically, in a conventional metal-gate read-only-memory, the second photolithographic mask is used to selectively form windows through a thick silicon dioxide film and a thin insulating layer such as silicon dioxide is grown in the etched out regions, thereby establishing a relatively low threshold voltage for the FET to be subsequently formed at the locations defined by these regions, while the threshold voltages at the FETs which are to be subsequently formed where the thick silicon dioxide remains will be relatively high. Thus, the desired data pattern at the memory locations can be established. The fabrication of the ROM then continues by the performance of several additional masking steps steps to form, for example, the contact holes, and metalization and passivation layers, as is conventional.

Since the known ROM fabrication techniques require that the data program process masking procedure to establish the desired data pattern by performed at an early stage of fabrication, such as the second photolithographic operation, read-only memories which have different programs must be segregated and separately processed during the subsequent stages of their fabrication. Thus, to fabricate ROMs with different programs, the ROM manufacturer must, after the first or second photolithographic step, segregate wafers of each different data pattern into a separate lot or wafer run and maintain lot traceability for each lot or run. Thus, the read-only memory manufacturer is not able to inventory wafers at a late stage of fabrication for subsequent mask-programming, and the requirement for

separate fabrication runs of ROMs having different stored programs significantly increases the cost and complexity of ROM fabrication.

ROMs which are programmable after fabrication, known as field-programmable ROMs (pROMS), have been developed which permit the end user to program the memory in accordance with a desired data pattern by applying a preset sequence of electrical signals to the unprogrammed memory. Although the pROM offers the advantage of standardized fabrication for all memories, followed by subsequent data-pattern formation, the density of these memories is relatively low, typically between one-quarter to one-eighth that of the previously described mask-programmable ROMs. No electrically alterable or field-programmable ROMs, however, are presently available that have the high density and ease of fabrication that are associated with the conventional mask-programmable ROMs. Moreover, the low density of the known pROMs substantially reduces their effectiveness for use in a microprocessor, particularly one formed on a single chip. It is also desirable, for similar reasons, to modify other characteristics of MOS devices, such as the formation of enhancement-and depletion-mode MOS devices, at a late stage of device fabrication, rather than, as is presently required, at an early fabrication stage and, preferably, to do so without introducing any additional photolithographic operations.

The present invention provides an integrated circuit structure comprising a semiconductor substrate; diffused regions selectively formed in one surface of said substrate; thin insulating regions, thick insulating regions, polycrystalline silicon regions, and metallic interconnections, each selectively formed overlying selected areas of said surface of said substrate; said diffused regions, said thin and thick insulating regions, said polycrystalline silicon regions, and said metallic interconnections forming an integrated circuit; an insulating layer overlying said integrated circuit; said insulating layer serving the function of providing a passivation layer over, and providing mechanical protection for, said integrated circuit; said insulating layer including openings selectively formed therein at locations overlying selected portions of selected ones of said metallic interconnections at which it is desired to define the position of bonding pads, said insulating layer including at last one additional opening selectively formed therein and overlying a portion of said integrated circuit at a position other than that of a bonding pad, said one additional opening being positioned above one of said polycrystalline silicon regions positioned above one of said thin insulating regions.

In the fabrication of MOS devices, it is conventional, at the last stage of fabrication, to form an overlying passivation layer to protect the chip. This layer is typically made of pyrolitically (i.e. by chemical vapor depositing) deposited silicon dioxide, but can also be formed by chemically depositing silicon nitride, phosphorus-doped silicon dioxide, or other materials. After the passivating layer is deposited, a photolithographic operation is performed to define windows at bonding pad locations and the passivating dielectric material is subsequently etched away at these locations in order to enable one to probe each die and then attach bonding wires to the device during the assembly operation.

In the structure of the present invention, the additional opening(s) in the passivation layer may be employed in the selective modification of certain electrical characteristics of the structure. In a particular embodiment of the invention, the structure forms a high-density ROM, and the passivation layer is employed as an implantation barrier and ion implantation is performed to form implantation layers at selective channel locations, thereby to program the high-density ROM at virtually the last stage of its fabrication. The time between programming or coding and completion of the device is thus reduced, thereby enabling the ROM manufacturer to fabricate and store uncoded chips for later programming with the protective passivating layer already deposited thereon.

The structures of the invention, such as ROMs, may be fabricated and then maintained in inventory, and later selectively modified in accordance with a desired pattern. MOS depletion-mode devices in accordance with the invention can be fabricated at lower cost and at higher yields.

Preferred embodiments of the present invention will now be described with reference to the accompanying drawings, in which:

Figures 1(a) - 1(g) are partial cross-sectional views illustrating some of the steps employed for manufacturing a structure according to one embodiment of the invention;

Figure 2 is a cross-sectional view illustrating a stage in a process for manufacturing a structure in accordance with another embodiment of the invention;

Figure 3 is a plan view of an MOS device illustrating a stage in a process for manufacturing a structure according to a further embodiment of the invention; and

Figure 4 is a cross-sectional view of the MOS device of Figure 3.

The process illustrated in Figures 1(a) - 1(g) is employed to fabricate a ROM, with

the coding of the ROM being performed in a late stage of the process. The process begins with the forming of the structure shown in Figure 1(a), which includes a p-type (100) substrate 10 on which is thermally grown a relatively thin (1,000Å to 1,5000Å) layer 12 of silicon dioxide, SiO_2. Layer 12 is immediately covered with a thicker (in the order of 2,000Å to 4,000Å) layer 14 of arsenic-doped polysilicon upon which a layer 16 of silicon nitride Si_3N_4 is deposited, such as by a chemical deposition process, to a thickness of between 1,000Å to 2,500Å. Alternately, other slow diffusants such as antimony may be used to dope the polycrystalline layer 14.

Thereafter, a first photolithographic operation is performed on the structure of Figure 1(a) to define the windows 18 at the locations of the source and drain regions of the FETs that are to define the data locations in the ROM. In this operation, portions of the silicon nitride layer 16 are selectively removed at the window locations. Then, using the remaining silicon nitride layer as a mask, the exposed portions of the polysilicon layer 14 and the underlying silicon dioxide layer 12 are removed as by etching to define the windows. Thereafter, n+−type impurities, such as phosphorus, are introduced, such as by diffusion or ion implantation, into the surface of the substrate to form the n+ source and drain regions 20 and 22 (Figure 1(b)).

A second photolithographic operation is then performed to remove portions of the silicon nitride layer 16 over the field or parasitic regions, allowing the nitride layer to remain at the gate regions of the locations of the proposed FETs. Portions of the polysilicon layer 14 from which the overlying nitride film has been removed are then either completely thermally oxidized and thus converted to silicon dioxide (not shown) using the remaining nitride layer as a mask against the oxidation of the remaining polysilicon layer, or alternately, are etched away using the nitride layer as a mask, after a thermal oxidation of the n+ regions 20 and 22 to protect them from the effects of the subsequent polysilicon etch.

The exposed portions of the silicon dioxide layer are then etched away and, as shown in Figure 1(c), a thin (in the order of 1,000Å) layer of silicon dioxide (not shown) is thermally grown over the unprotected source, drain, and field regions, after which a low-level implant of boron ions is carried out into and through this oxide layer and into the source, drain, and field regions, with the remaining nitride layer and underlying polysilicon layer at the gate regions acting as an implantation barrier. This implantation operation forms a p-type layer 24 at the field regions for the purposes described in U.S. Patent No. 3,751,722.

The structure at this stage of the process is then placed into an oxidizing environment, whereby the portions of the wafer that are not covered by the remaining nitride layer 16 are oxidized to form a thick silicon oxide region 26 at the field regions, which overlies the p-type layer 24.

The remaining nitride layer 16 is then removed, such as by the use of a hot phosphoric acid, and desired contacts through the thick silicon dioxide region 26 to any of the various n+ diffused regions are defined and etched using a conventional photolithographic technique, and a second (n+ doped) layer of polycrystalline silicon 23 is then deposited over the structure to a thickness of between 1000Å and 3000Å (Figure 1(d). A metal layer 30 is deposited directly on top of the doped polysilicon layers over the entire surface of the wafer. The metalization pattern is then defined and etched, and the underlying second layer 28 of polysilicon is etched away from all areas that are not covered by metal, using the remaining metal layer as a mask. The etch employed to etch the polycrystalline silicon will not materially attack either the metal or the silicon dioxide.

As shown in Figure 1(e), at this stage of the process the metalization pattern remains over all rows of the ROM matrix defined by the FETs that have been formed (two of which are shown in Figure 1(e)) and thus remains over all portions of the gate regions of these transistors. A passivation layer 32, which may be chemical-vapor deposited silicon dioxide, is then deposited over the surface of the wafer to a thickness of between 3,000Å and 10,000Å, and the passivation layer is covered by a photoresist 34.

The ROM, at this late stage of the fabrication process, is now coded to define the desired stored data pattern. To this end, the photoresists 34 is patterned and etched to define windows, such as 36 (Figure 1(f)), over every gate or bit location in the ROM at which it is desired to store a logic "O" or "off" state. The silicon dioxide passivation layer is then etched away and the remaining photoresist and underlying silicon oxide of the passivation layer are used as a mask to etch away the exposed metal layer 30, such as by using a plasma etching technique or a chemical etch.

Once the metal has been removed from the desired gate locations, the wafer is subjected to a high-energy (e.g. 150 KeV or higher) implant of singly-ionized boron (B+) ions, as indicated at. Alternately, doubly-ionized boron ions of lower energy may be employed. The ions are of sufficient energy to penetrate through the polycrystalline layers 14 and 28 and silicon dioxide

layer 12 to the underlying substrate to form an implanted layer 40 (with a higher concentration of boron atoms than in the substrate) in the channel region of the left-hand transistor which extends between the source and drain regions 20 and 22 (Figure 1(g)). The water is then subjected to a low-temperature anneal in hydrogen at a temperature of between 440°C and 500°C to eliminate radiation damage and fast states, and in a subsequent photolithograhic operation, the passivation layer is again selectively etched away to define the areas for pad locations.

For a sufficient dosage of boron ions (typically between 10^{11} and 10^{14} ions/cm^3), the implant layer 40, wherever it has been formed, has the effect of shifting the threshold voltage associated with the gate region of the n-channel FET in a positive direction. The threshold voltages associated with the exposed FETs thus become more positive as a result of this ion implantation, such that when a positive voltage is applied to the conducting line over the bit at which the implant region is thus formed, the transistor will not turn on, no current flow will be detected between the drain and source, and the bit will be recognized as a logic "0", as indicated for the left-hand transistor of Figure 1(g). However, at any bit location over which no window was etched away in the passivation layer, the metal and passivation material remaining over those transistor gate regions will provide an effective implantation barrier, and accordingly, no ion implantation will occur at these locations. Electrical continuity along each conducting row of the ROM matrix is effected by the electrical conductivity of the metal layer and underlying doped polycrystalline silicon layer, and where the former has been removed at "O" bit locations, the remaining polysilicon layer provides the conduction path. A transistor at a location such as that at the right of Figure 1(g), will turn on at a low voltage when a potential is applied to the metal line, current flow will be caused and detected between the drain and source, and the bit will be recongnized to be a logic "1", as indicated.

The process of Figure 82, which illustrates a stage in a process for programming a ROM by forming "1" and "0" data storing transistors at selected locations in the data matrix, may be used to code a metal-gate, thick-oxide, MOS structure after the passivation layer has been applied. A p-channel structure is shown in the Figure but, as in all the embodiments of the invention herein described, the process can easily be used to fabricate the opposite polarity (n-channel in this case) structure. More specifically, the process as shown in Figure 82 is performed on a MOS structure including an n-type silicon substrate 126 in which p+ source and drain regions 128 and 130 are formed, e.g., by diffusion. Gate insulator films 132 of silicon dioxide and thick silicon oxide regions 134 are formed by conventional processes and are then covered by a thin layer 136 of n+ doped polysilicon.

Metal is then deposited and etched away to form a metalization layer 138 over the doped polysilicon layer 136. The metal, after it is etched, is in turn used as a mask to etch away the exposed doped polysilicon layer. Thereafter, a passivation layer 140 is deposited over the surface of the wafer.

The process for manufacturing a structure according to the embodiment of Figure 28, departs from the conventional techniques by etching windows through selected locations of the passivating layer, such as at 142, over each location at which it is desired to form a "0" storage location. Using the remaining passivation layer as a mask, the exposed metal at the selected locations is etched away to leave the polysilicon layer exposed. An ion implantation procedure is then carried out utilizing singly-ionized or doubly-ionized phosphorus ions 144, which are of sufficient energy to pass through the exposed polysilicon-silicon dioxide gate structure to create an n-type implanted layer 146 which extends between the source and drain regions 128, 130. For the reasons described previously, the implanted layer shifts the threshold voltage associated with the left-hand transistor in Figure 2 to create a logic "0" bit, as desired.

The metal (aluminum)-doped polysilicon interconnections achieved in the structure of Figure 2 will also have a beneficial effect on the elimination of leakage currents caused by aluminum spiking through dislocations through shallow junctions and into the substrate. At contact hole locations, the doped layer of polysilicon will act as a spiking barrier to the penetration of aliminum through the underlying junction during the alloying step. The effectiveness of the doped polysilicon layer will be heavily dependent on its thickness and the degree of order/disorder of the "lattice" associated with the polysilicon material itself.

The n-channel RDM forming the embodiment illustrated in Figures 3 and 4, can be coded at the same time as the formation of the pad mask. As shown in Figure 4, n+ regions 74, 76 78 and 80 are formed in the upper surface of a p-type silicon substrate 82. P-type regions 84 with acceptor concentrations greater than in the substrate are formed in the surface of the substrate and extend between nonrelated n^+ regions, as described above with respect to the embodiment of Figure 1. The gate regions are covered with a thin oxide insulating region

86 and a doped polysilicon layer 88, and the field regions are covered with a thick silicon dioxide region 90. It should be noted that the fabrication precedure employed to fabricate this structure results in coplanar drain, source, and channel regions.

A phosphosilicate glass layer 148 is formed over the thick oxide regions 90, the polysiliconoxide gate structures, and the exposed drain and source regions. Next, contact hole openings are formed in the phosphosilicate glass layer 148, and a selectively etched metalization layer 150 is formed which makes contact with the gate, source, and drain regions through these openings. Subsequently, a low-temperature deposited silicon nitride passivating layer 152 is deposited over the surface of the wafer.

To code a ROM during the final photolithographic operation, during which, conventionally, openings are formed in the passivation layer at the desired pad locations, additional openings are formed in the passivation layer at specific locations within the ROM matrix. Thereafter, using the remaining passivation layer and overlying photoresist as a mask, the exposed phosphosilicate glass layer is etched away, typically through the use of either chemical or plasma etching, to form a window 154 which leaves exposed either a portion of, or all of, the polysilicon layer 88a overlying the oxide gate insulator 86a.

Thereafter, an implantation operation utilizing high-energy singly-ionized or doubly-ionized boron ions 156 is performed with any, some, or all of the remaining passivation layer, metalization layer, phosphosilicate layer, or remaining resist acting as an implantation barrier. As a result of the ion implantation, a p-type implanted channel 158 is formed in part of, or throughout, the channel region of the right-hand transistor in Figure 4, thereby the change the threshold voltage associated with this transistor to place it in the always "off" condition corresponding to a logic "0" condition. A metal contact 160 (Figure 3) is made to the polysilicon gate structure of this transistor. The left-hand transistor, which was protected by the combined passivation and phosphosilicate layers during the ion implantation, remains unaffected by the ions and is thus in a logic "1" condition.

In summary, MOS devices in accordance with the invention can be selectively modified, such as to code or program the bit locations of a ROM, or to form depletion-mode devices near the final stages of wafer fabrication, and often without the need for additional photolithographic and masking operations. The modification of the MOS device may be achieved during the contact, metalization, or pad mask photolithographic operations followed by ion implantation through openings formed during these operations to form an implanted layer at desired gate channel locations, which has the effect of modifying the characteristics of the associated MOS devices.

It will thus be appreciated that almost-finished MOS devices can be fabricated and then stored in wafer form, ready, as in the case of a ROM, to be mask-programmed and then passed quickly into final assembly. The invention finds particular utility and importance in the field of ROMs and associated input-output circuits for peripheral support circuits on a single chip as is the present trend in the industry. A high-speed microprocessor with on-chip read-only-memories and random-access memories, complete with input-outputs, may be formed on a single chip after which the ROMs and input-output circuits can then be programmed after the passivating layer has been deposited on the wafer. A product which is standard up to virtually the last stages of wafer fabrication may be later customized, or programmed, to meet specification in a small fraction of the time presently required to design and fabricate an MOS custom circuit. The unprogrammed wafers can be kept in inventory until programmed in the final stages of the process.

Many different types of passivating layer materials presently used in MOS fabrication, such as silicon dioxide, silicon nitride, doped silicon dioxide, and aluminum oxide maybe employed in structures of the invention. Moreover, the implantation procedures employed for modifying the characteristics of the structures may utilize singly-, doubly-, or triply-ionized boron or phosphorus ions at suitable energy and dosage levels so long as the ions in sufficient amounts penetrate through the exposed layers and into the substrate. While the structures described herein have either an n-channel of p-channel configuration, each can alternatively have the opposite polarity configuration.

The processes described herein for manufacturing integrated circuit structures are also described, and certain aspects thereof claimed, in our co-pending parent application No. 46245/77. (Serial No. 1594957).

WHAT WE CLAIM IS:-

1. An integrated circuit structure comprising a semiconductor substrate; diffused regions selectively formed in one surface of said substrate; thin insulating regions, thick insulating regions, polycrystalline silicon regions, and metallic interconnections, each selectively formed overlying selected areas of said surface of said substrate; said diffused regions, said thin and thick insulating regions, said polycrystalline silicon regions, and said metallic interconnections forming an integrated circuit; an insulating layer

overlying said integrated circuit; said insulating layer serving the function of providing a passivation layer over, and providing mechanical protection for, said integrated circuit; said insulating layer including openings selectively formed therein at locations overlying selected portions of selected ones of said metallic interconnections at which it is desired to define the position of bonding pads, said insulating layer including at least one additional opening selectively formed therein and overlying a portion of said integrated circuit at a position other than that of a bonding pad, said one additional opening being positioned above one of said polycrystalline silicon regions positioned above one of said thin insulating regions.

2. A structure as claimed in claim 1, in which said integrated circuit is a metal-insulator-semiconductor integrated circuit.

3. A structure as claimed in claim 1 or 2, in which said diffused regions are of a conductivity type opposite to that of said semiconductor substrate.

4. A structure as claimed in any preceding claim, in which said insulating layer comprises silicon dioxide.

5. A structure as claimed in any one of claims 1 to 3, in which said insulating layer comprises silicon nitride.

6. A structure as claimed in claim 5, including a layer of phosphosilicate glass covered by said layer of silicon nitride.

7. A structure as claimed in any preceding claim, in which the concentration of impurity atoms at the surface of said semiconductor substrate has been selectively altered at locations underlying at least one of said additional openings.

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Sheet 1

FIG.1a

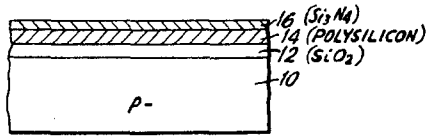


FIG.1b

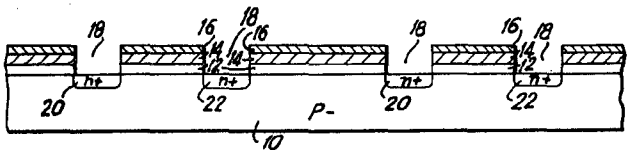


FIG.1c

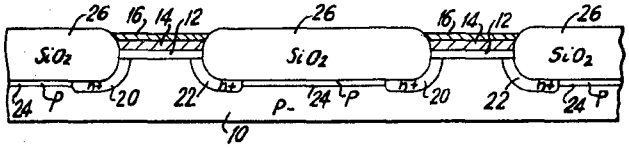


FIG.1d

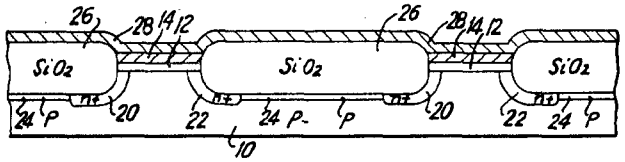


FIG.1e

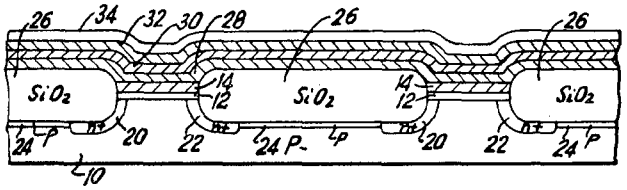


FIG.1f

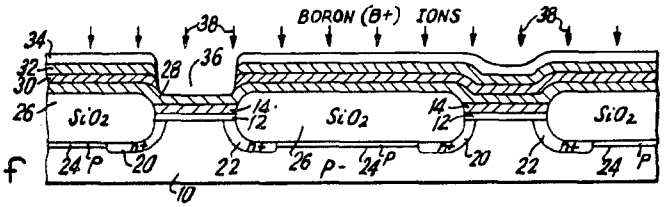
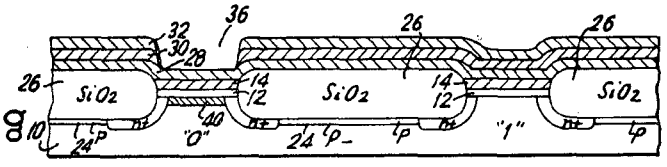


FIG.1g



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Sheet 2

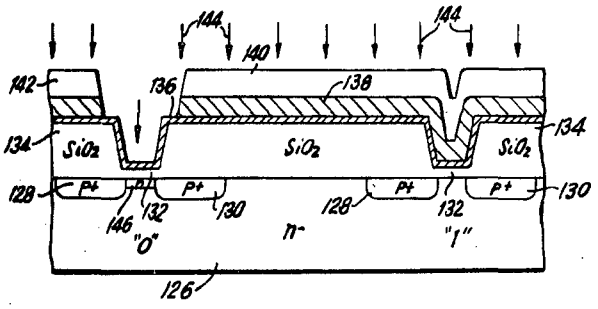

FIG. 2

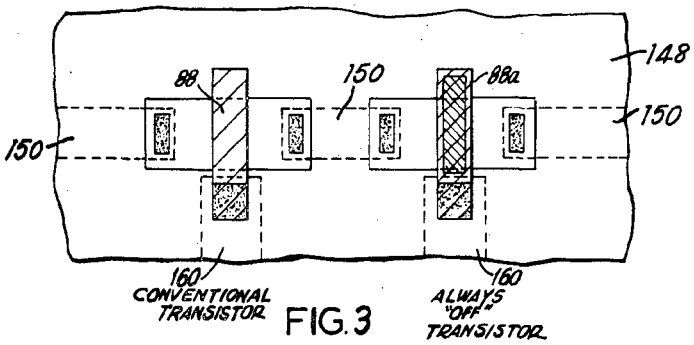

FIG. 3

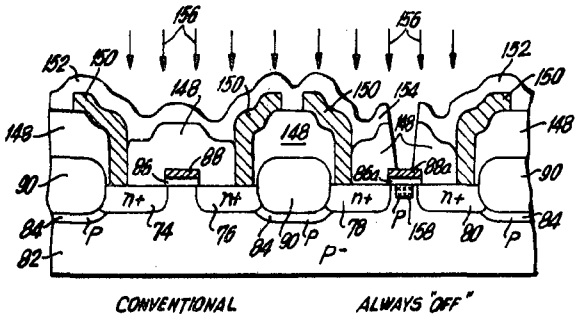

FIG. 4