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SUMMARY OF TRANSIENT HIGH-VOLTAGE CALCULATIONS FOR THE FRX-C EXPERIMENT

by

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ABSTRACT

Calculations of the electrical circuit equations are performed over a wide range of parameters corresponding to the FRX-C field-reversed Θ-pinch experiment at Los Alamos. Without any plasma or external damping, serious voltage doubling and quadrupling of the main capacitor bank charge voltage are observed. These oscillating high voltages are found to be adequately suppressed by the strategic placement of external "snubber" circuitry. On the other hand, no doubling of the Θ-pinch preionization bank charge voltage is found. Calculations of the equations for the z-pinch preionization circuit are also performed.

I. Introduction

In an effort to determine and suppress any transient high voltages, calculations of the electrical circuit equations were performed corresponding to the parameters of the FRX-C device.[1] The code Mini-Sceptre,[2] available on the Lawrence Livermore National Laboratory MFE - CDC-7600 computer, was used for these numerical evaluations.

The equivalent circuit used in these computations is shown in Fig. 1. In view of the near-symmetry of the FRX-C dual-feed system, this circuit represents only one-half of the respective main and Θ-pinch preionization capacitor banks, cables, collector plates, bias field circuit, and load. Average values of the respective circuit parameters are listed in Fig. 1. The low-voltage bias magnetic field capacitor bank circuit could be neglected because it is normally crowbarred during the high-voltage bank operation. Each transmission line (consisting of parallel coaxial cables) was represented as five discrete capacitors and six inductors. (Doubling these numbers of discrete elements made no noticeable changes in the computed voltages and

currents.) Any coupling to the discharge plasma was neglected, and the only damping considered was that caused by external "snubber" circuitry; therefore, these results represent "vacuum" or worst cases where transient voltages are not suppressed by the plasma.

Adjustable parameters in these calculations included (see Fig. 1) : (1) bias inductor snubber parameters R_{Bs}, L_{Bs}, C_{Bs}; (2) collector plate resistive damper elements R_D, L_D; (3) main-bank snubber parameters R_x, L_x, C_x. The results are arranged into three sections consisting of studies of the main capacitor bank, Θ-pinch preionization (PI), and Z-pinch PI, respectively.

II. Main-Bank Studies

Figure 2 shows results corresponding to the case where the main bank is discharged at 42 kV and where the Θ-PI bank is fully discharged with spark gaps closed. (No qualitative differences appeared when PI gaps were considered open.) For this case, no snubbers or damping resistors were considered, so these results represent FRX-C operational conditions before January 1982. As seen from this figure, the load coil voltage "rings" at approximately 3.1 MHz (resulting from cable pulse charging), often doubling the original charge voltage. Further doubling (~150 kV) occurs across the bias isolation inductor; this effect probably caused the observed high-voltage breakdown failures at the cable feeds to this inductor.

During January 1982, four snubbers, each consisting of a 0.05-μf, high-voltage, low-inductance capacitor in series with a 1.8-Ω resistor and with a total self-inductance (after installation) of approximately 80 nH, were installed across the bias inductor. Results from calculations for this situation are shown in Fig. 3. As seen from these graphs, the bias snubber successfully damps out the recurrent oscillations shown in Fig. 2, both on the bias inductor as well as on the load coil. A peak current per snubber of approximately 20 kA flows for about 100 nsec with a total energy less than 200 J deposited. The first voltage peak may be reduced with additional parallel snubbers (e.g., see Fig. 4) at the expense of persistent oscillations across the load coil.

Further reductions (although less dramatic) of the initial voltage oscillations could be achieved by adding snubbers across the main-bank capacitors. For example, Figs. 5a-d show the load coil and bias inductor

voltages when 10%, 25%, 50%, and 100% of these capacitors each have a 0.05-μf, 3.6-Ω, 80-nH snubber across them. These snubber values were considered because they were "tuned" to damp out the calculated oscillations; furthermore, a sizable quantity of these components (~300) has already been procured by CTR division and might be made available for use on FRX-C, if necessary. The total snubber currents and deposited energies for these cases are shown in Figs. 6a-d.

The effect of a damping resistor R_D, perhaps consisting of a conducting rubber linking the edges of the collector plates, was also considered. Including the existing bias inductor snubber, Fig. 7 shows results for R_D = 0.7 Ω . Unfortunately, this represents a lower limit on R_D, since lower values will conduct more than 10% of the Θ-pinch PI current.

The effect of main-bank jitter is shown in Figs. 8a-d where the discharging of 10% of the main bank was delayed 50, 100, 200, and 500 nsec, respectively. For these calculations, only the actually installed bias snubbers were included. Figs. 9a-d show the same type of plots if 25% of the main bank fired late. The persistent oscillations observed in Figs. 8 and 9 were significantly decreased by adding the 0.7-Ω damping resistor R_D (e.g., see Fig. 10a); however, the addition of the above-mentioned snubber circuits to the entire main bank was much less effective (Fig. 10b).

To justify the use of the "half" circuit model (Fig. 1), a limited number of calculations were performed using the full FRX-C electrical circuit shown in Fig. 11. The near-symmetry of this circuit is reflected in Fig. 12, corresponding to the case where the complete main bank is discharged. In Fig. 12a, voltages across the load coils LLT and LLW (see Fig. 11) and both bias inductors are plotted for the case with no external damping. The effect of the normal bias inductor snubbers (R = 0.45 Ω, L = 20 nH, C = 0.2 μF across each inductor) on these parameters is shown in Fig. 12b. The jitter problem associated with one side of this bank discharging late was also investigated and no further voltage enhancements were found.

III. Θ-Pinch PI Studies

Calculations were also performed for the discharging of the Θ-pinch PI bank. Figure 13 shows results when no snubbers or dampers were considered. (Again, this case corresponded to FRX-C operation conditions before January 1982.) For this case, the PI bank was discharged at 55 kV and the main bank

was charged to 42 kV with spark gaps continuously open. Both the absence of voltage doubling and the relatively low frequency oscillations (1.0 MHz) are indicative of the large capacitance arising from the 420 main-bank cables also connected across the collector plate. The effect of the bias inductor snubber (i.e., current operational conditions) is shown in Fig. 14. Further calculations for a variety of snubber and damper resistor values showed no high-voltage transients.

IV. Z-Pinch PI Studies

Some brief results are presented from analyzing the FRX-C Z-pinch PI circuit (see Fig. 15). Mini-Sceptre was especially suited for these analyses, since it allowed the proper dependence of resistance on current for the varistor stack as well as a delayed breakdown time of the plasma. Sample results are presented in Fig. 16 for the case with 45-kV bank voltage and a very low resistance plasma (compared with the inductive reactance). The effect of delayed plasma breakdown is shown in Fig. 17. Each curve corresponds to a separate calculation where the plasma resistance was decreased from essentially infinity to zero in 1 nsec at times up to 12 μsec after triggering the z-pinch capacitor bank. The observed decreasing plasma current with later breakdown time is a consequence of the increasing fraction of the capacitor bank discharged through the 3.1-Ω shunt resistance.

V. Conclusions

Calculations were performed of the FRX-C circuit equations for the main capacitor bank, Θ-pinch PI, and Z-pinch PI systems. Serious voltage doubling and even quadrupling of the main-bank charge voltage were observed for vacuum shots when no external snubber or damping circuitry was considered (corresponding to the experimental situation before January 1982). The addition of bias inductor snubbers, installed on the experiment in January 1982, resulted in the successful damping of the calculated enhanced oscillating voltages both at the bias inductor and the load coil. Although further suppression of the initial oscillations could be achieved using individual snubbers across a fraction of the main-bank capacitors, it is not recommended at this time in view of the sizable cost and machine downtime required. However, if bank jitter appears to be a serious problem, a

collector-plate-damping resistor could prove very useful in suppressing calculated persistent oscillations.

Calculations of the Θ-PI circuit equations resulted in no observed voltage doubling, even without any snubbing or damping circuits. This was a result of the relatively low-impedance main-bank cables located across the collector plate.

Mini-Sceptre also proved useful in analyzing the Z-pinch PI circuit. For example, it could handle plasma breakdown time variation as well as the varistor R (I) dependence.

Acknowledgments

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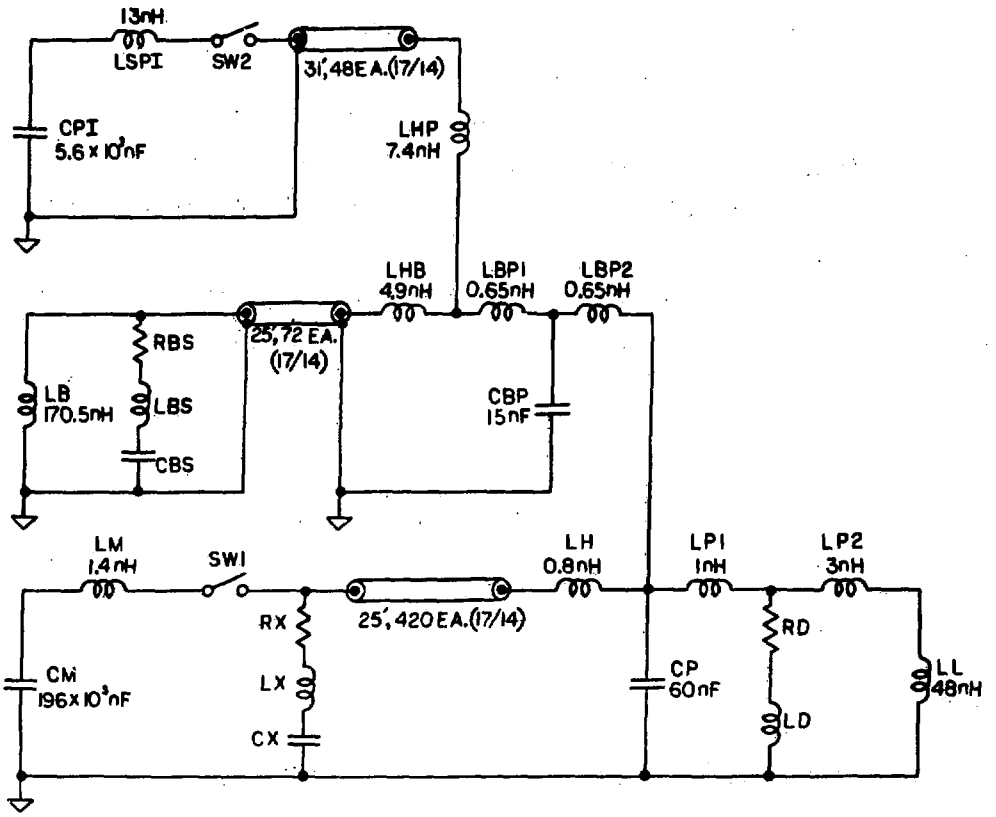
References

1. W. T. Armstrong, R. R. Bartsch, J. C. Cochrane, R. W. Kewish, M. Haworth, R. K. Linford, J. Lipson, K. F. McKenna, D. J. Rej, E. G. Sherwood, R. E. Siemon, and M. Tuszewski, Proc. Fourth Symp. on the Physics and Technology of Compact Toroids, Lawrence Livermore National Laboratory, 1981.

2. H. W. Carter, "Mini-Sceptre A Computer Program for Electronic Circuit Analysis," Lawrence Livermore Laboratory report UCID-30069 (1973).



LEGEND FOR FIGURE 1

CM	-	Main-bank capacitance
LM	-	Main-bank spark gap inductance
RX, LX, CX	-	Main-bank snubber circuit elements
LH	-	Average collector plate cartridge inductance
CP	-	Average collector plate capacitance
LP1, LP2	-	Average collector plate inductance
RD, LD	-	Average collector plate damping resistor circuit elements
LL	-	Pinch coil inductance
LB	-	Bias isolation inductance
RBS	-	Bias snubber circuit elements
LHB	-	Average collector plate bias cartridge inductance
CBP	-	Average collector plate capacitance at bias and PI cartridges
LBP1, LBP2	-	Average collector plate inductance at bias and PI cartridges
CPI	-	θ-pinch preionization bank capacitance
LSPI	-	θ-pinch preionization spark gap inductance
LHP	-	θ-pinch preionization cartridge inductance

Fig. 1. Schematic diagram of circuit used in these calculations.

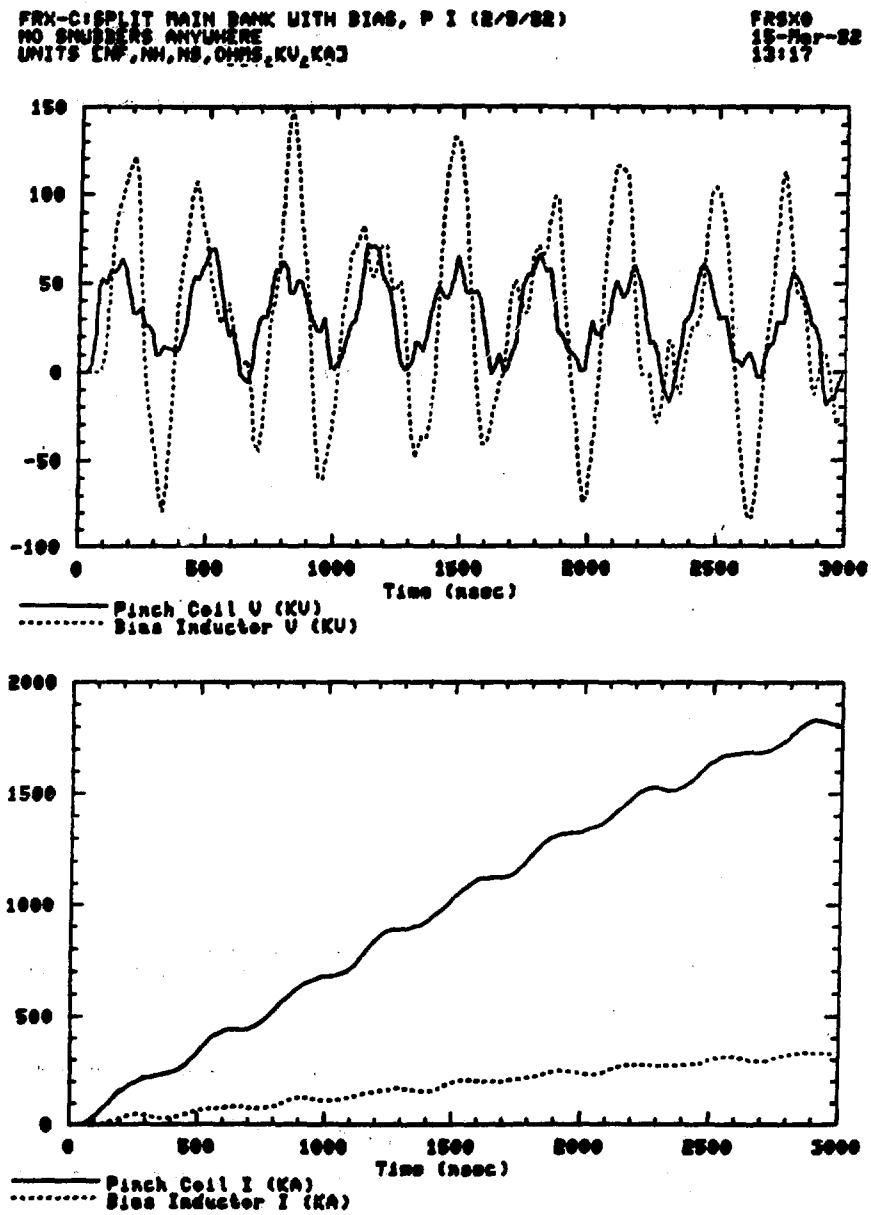


Fig. 2. Load coil and bias inductor voltages and currents calculated for a 42-kV main-bank discharge with no snubbers or damping resistors.

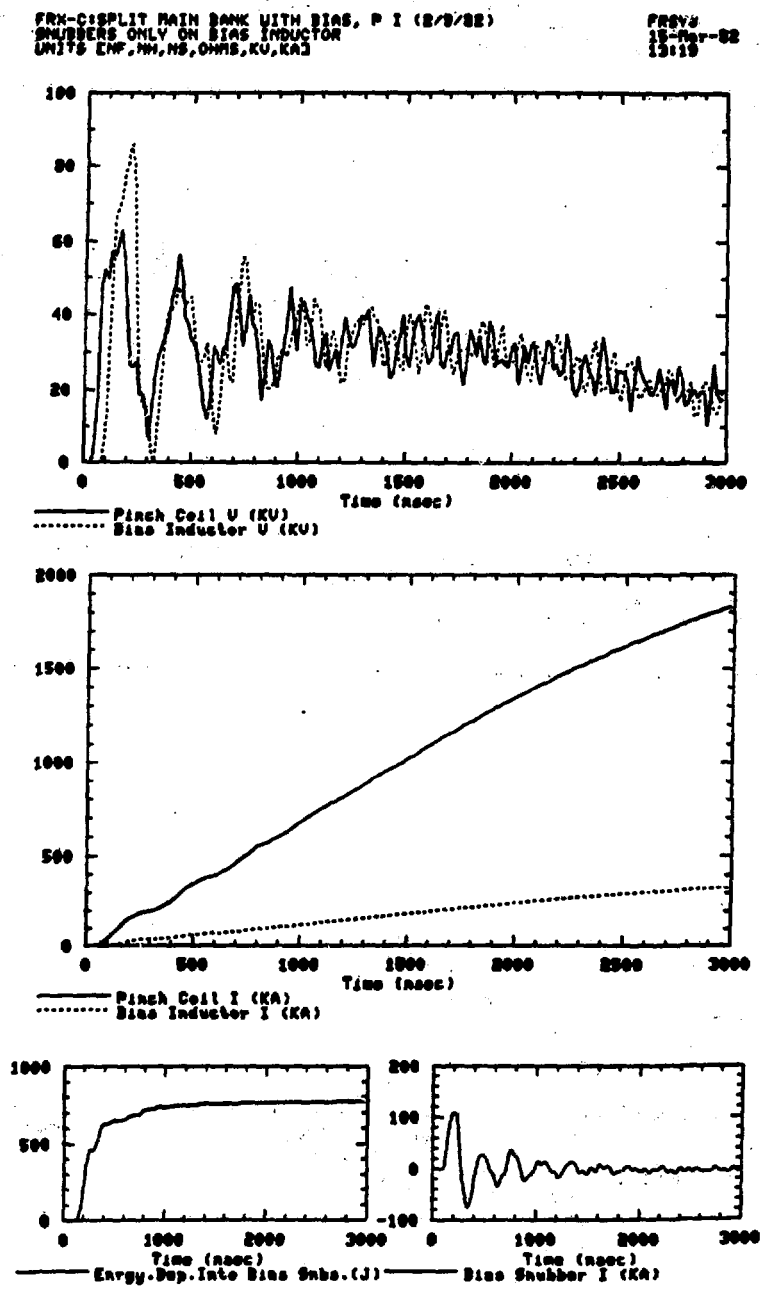


Fig. 3. Voltages, currents, and total deposited energy calculated for a 42-kV main-bank discharge with a 0.45-Ω, 0.2-μF, 20-nH snubber placed across the bias isolation inductor.

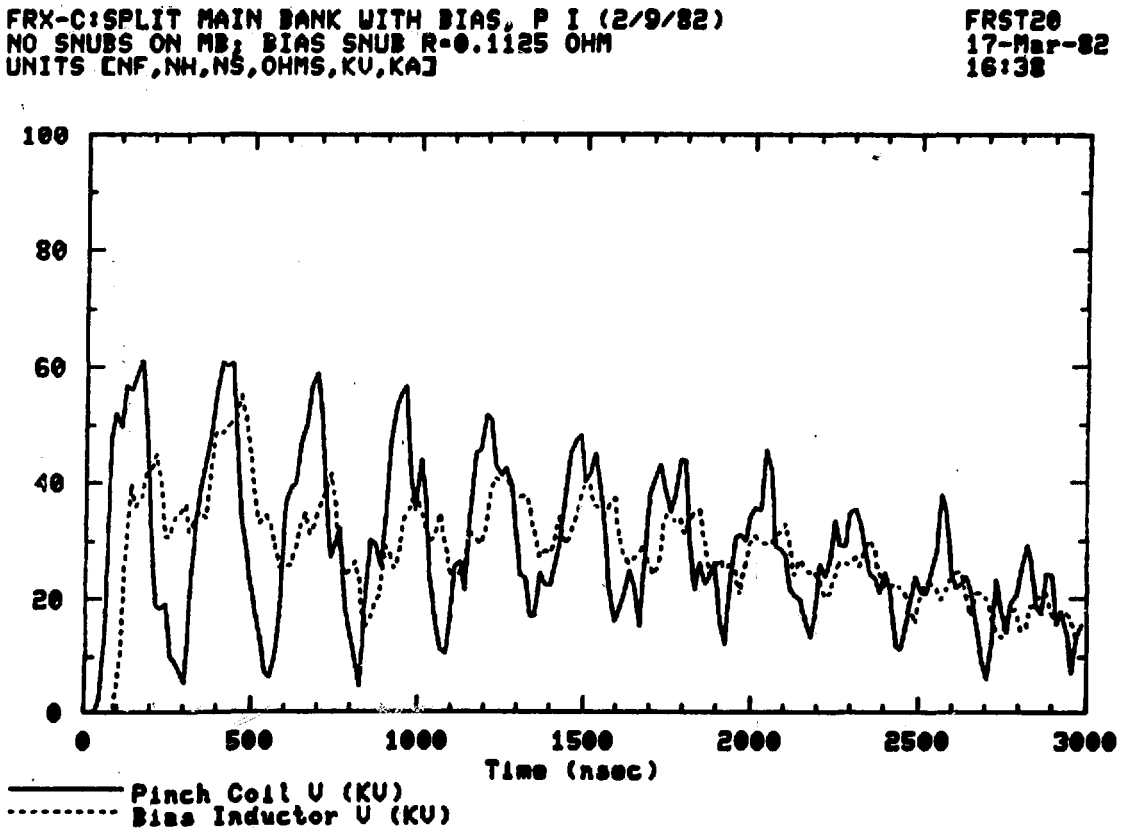


Fig. 4. Voltages calculated for a 42-kV main-bank discharge with a 0.113-Ω, 0.8-μF, 5-nH bias inductor snubber.

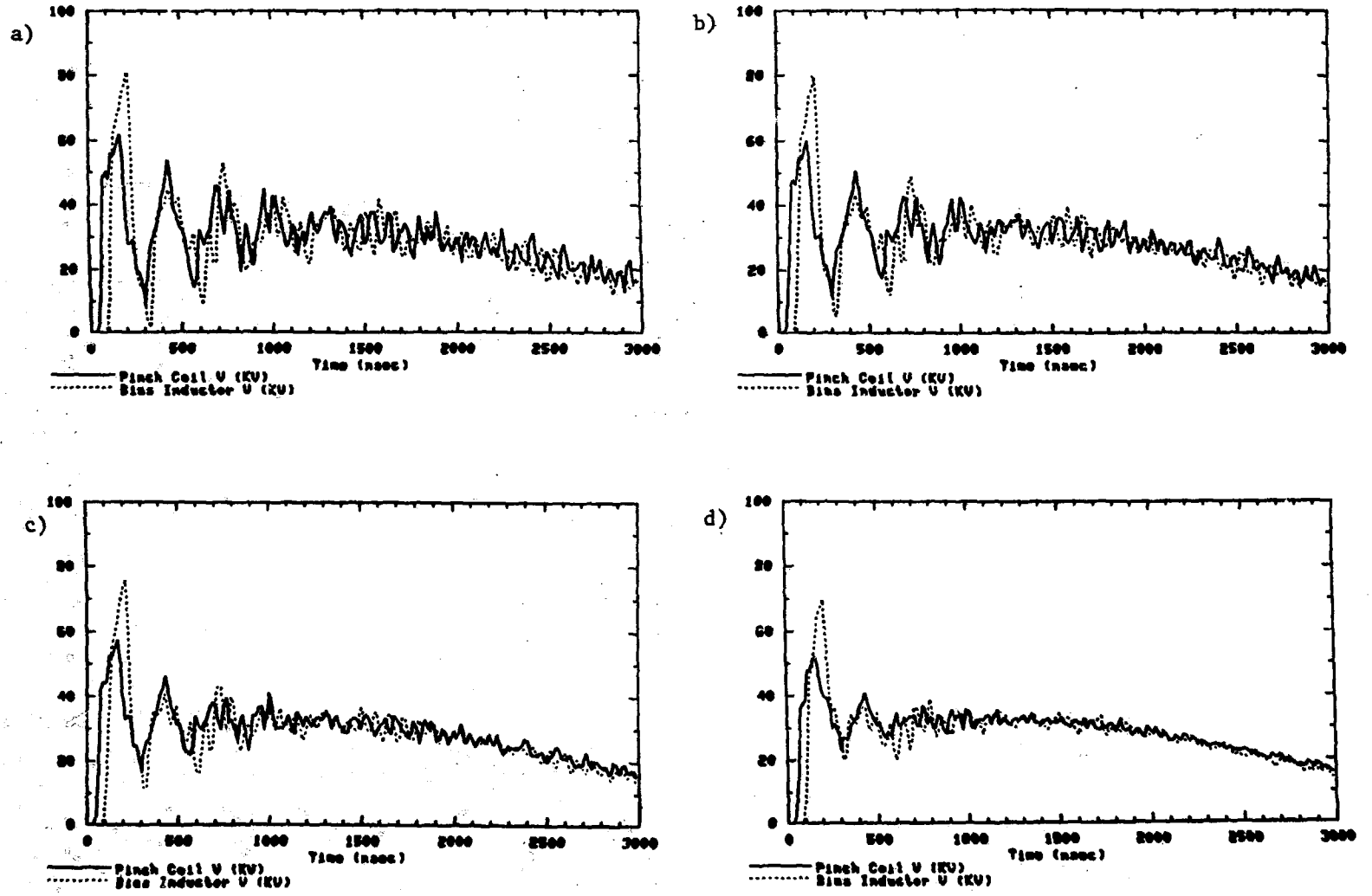


Fig. 5. Effect of main-bank snubbers: voltages calculated when a) 10%, b) 25%, c) 50%, and d) 100% of the main-bank capacitors are each equipped with a 3.6-Ω, 0.05-μf, 80-nH snubber; a 0.45-Ω, 0.2-μF, 20-nH snubber is also across the bias inductor.

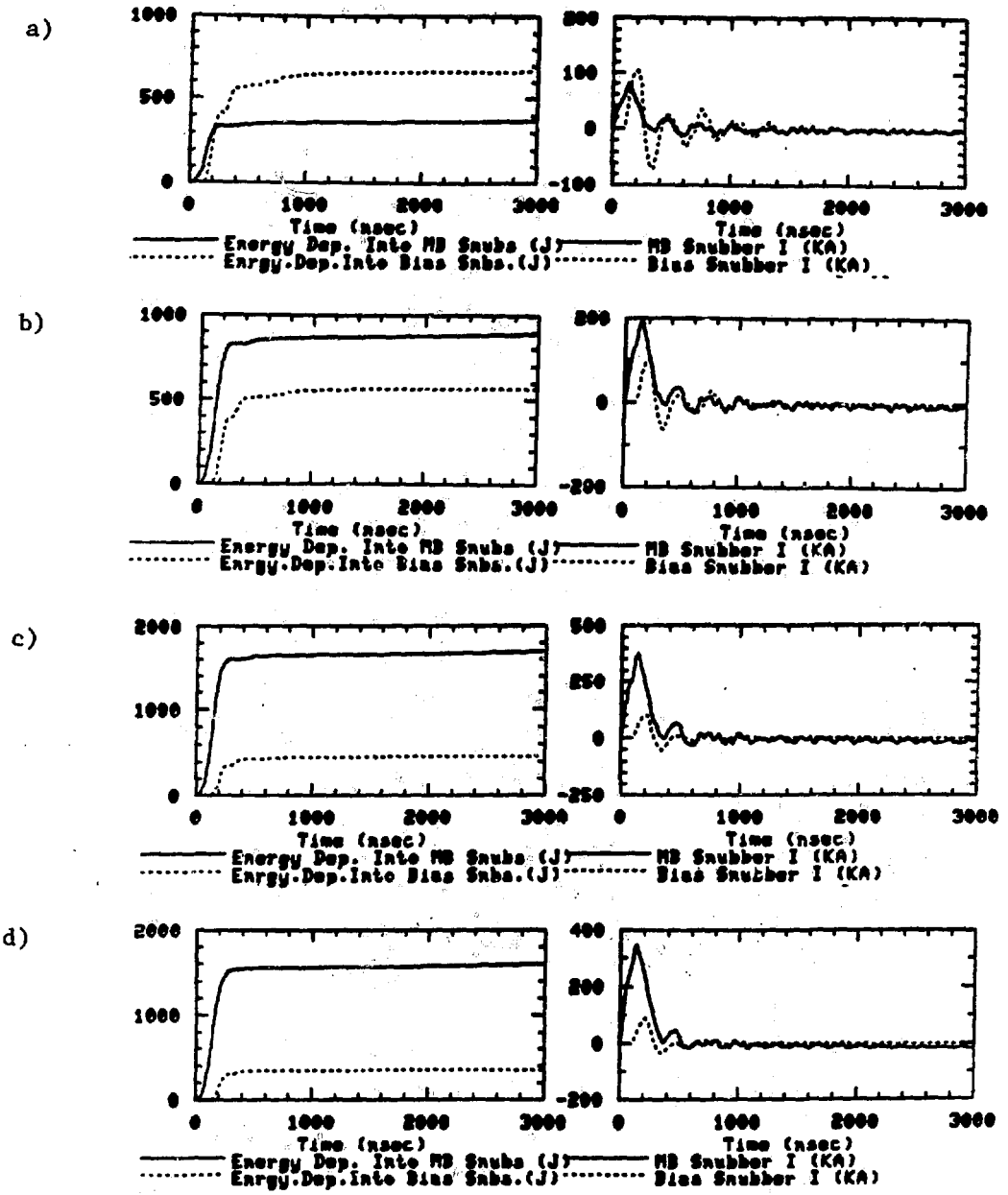


Fig. 6. Bias and main-bank snubber energies and currents for the cases where a) 10%, b) 25%, c) 50%, and d) 100% of the main bank is equipped with snubbers.

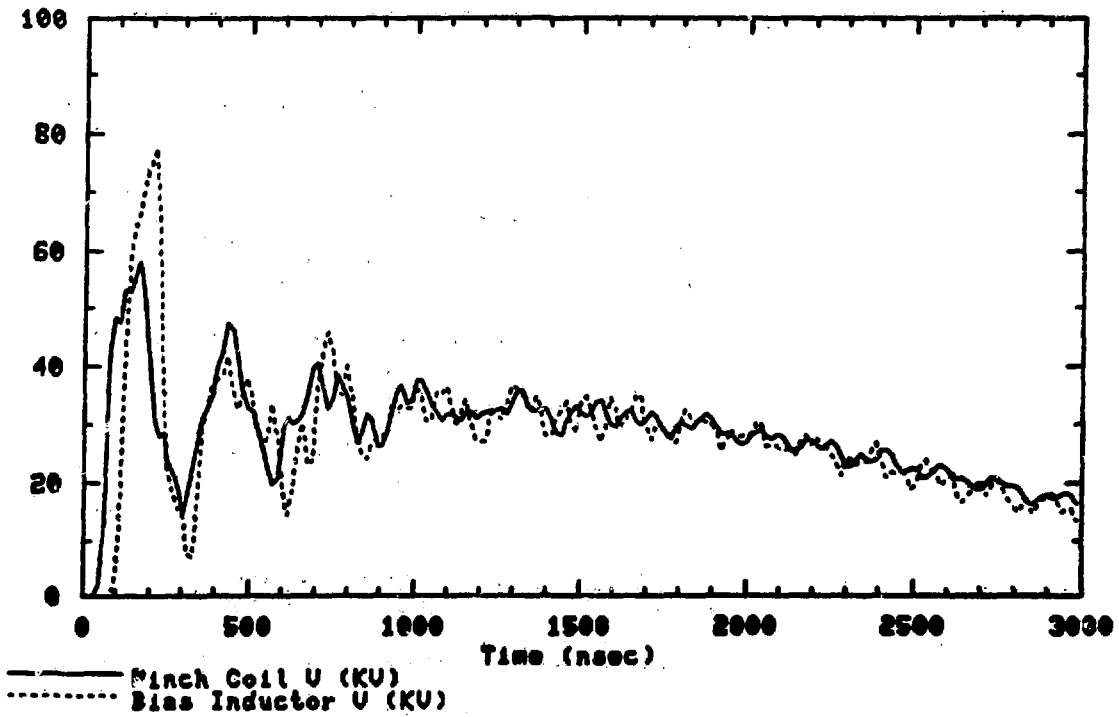


Fig. 7. Effect of a 0.7-Ω "damping" resistor placed across collector plates. The normal bias inductor snubbers are also included.

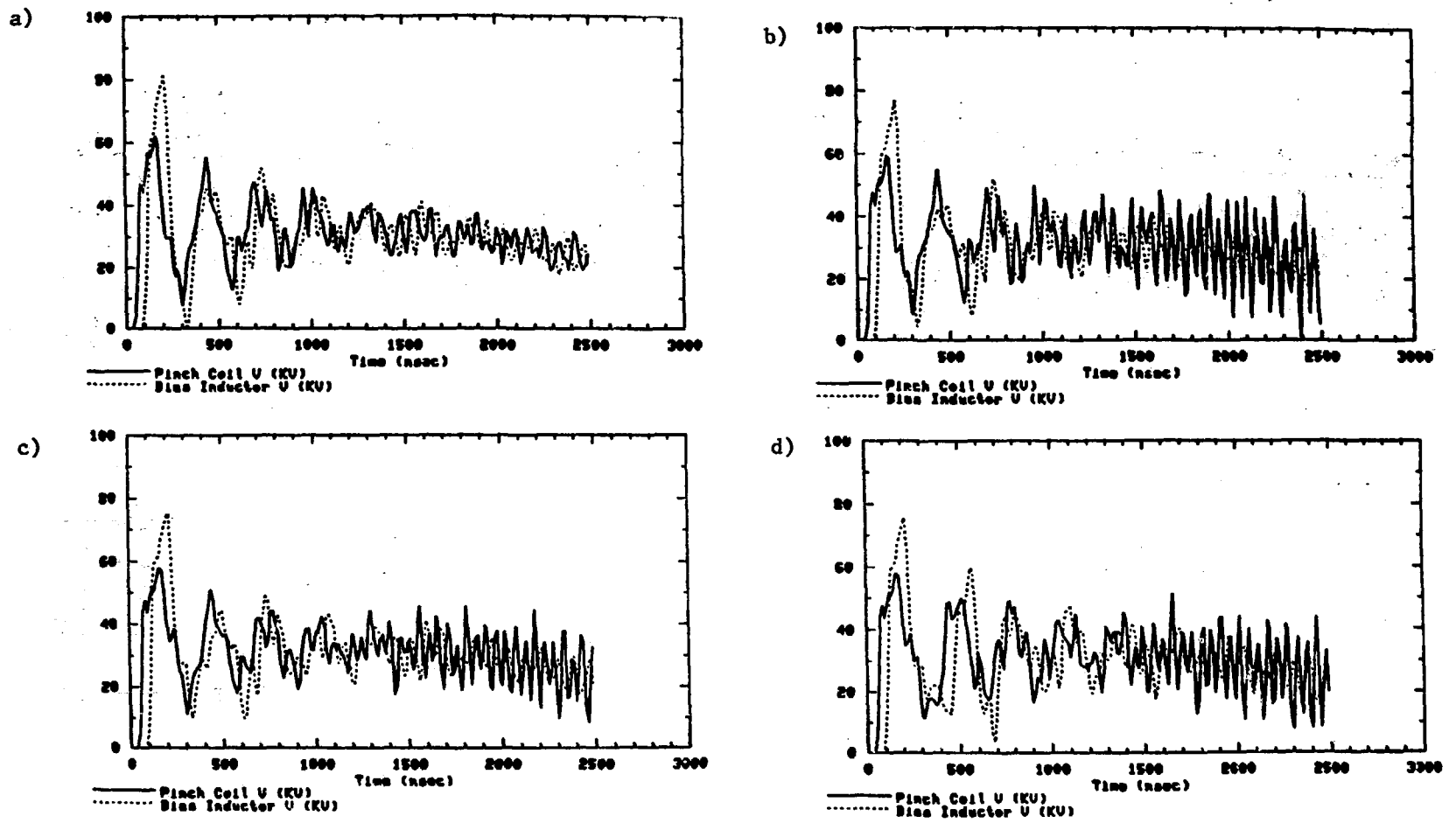


Fig. 8. Effect of main-bank jitter: calculated voltages for cases when 10% of the main bank discharges a) 50, b) 100, c) 200, and d) 500 nsec late.

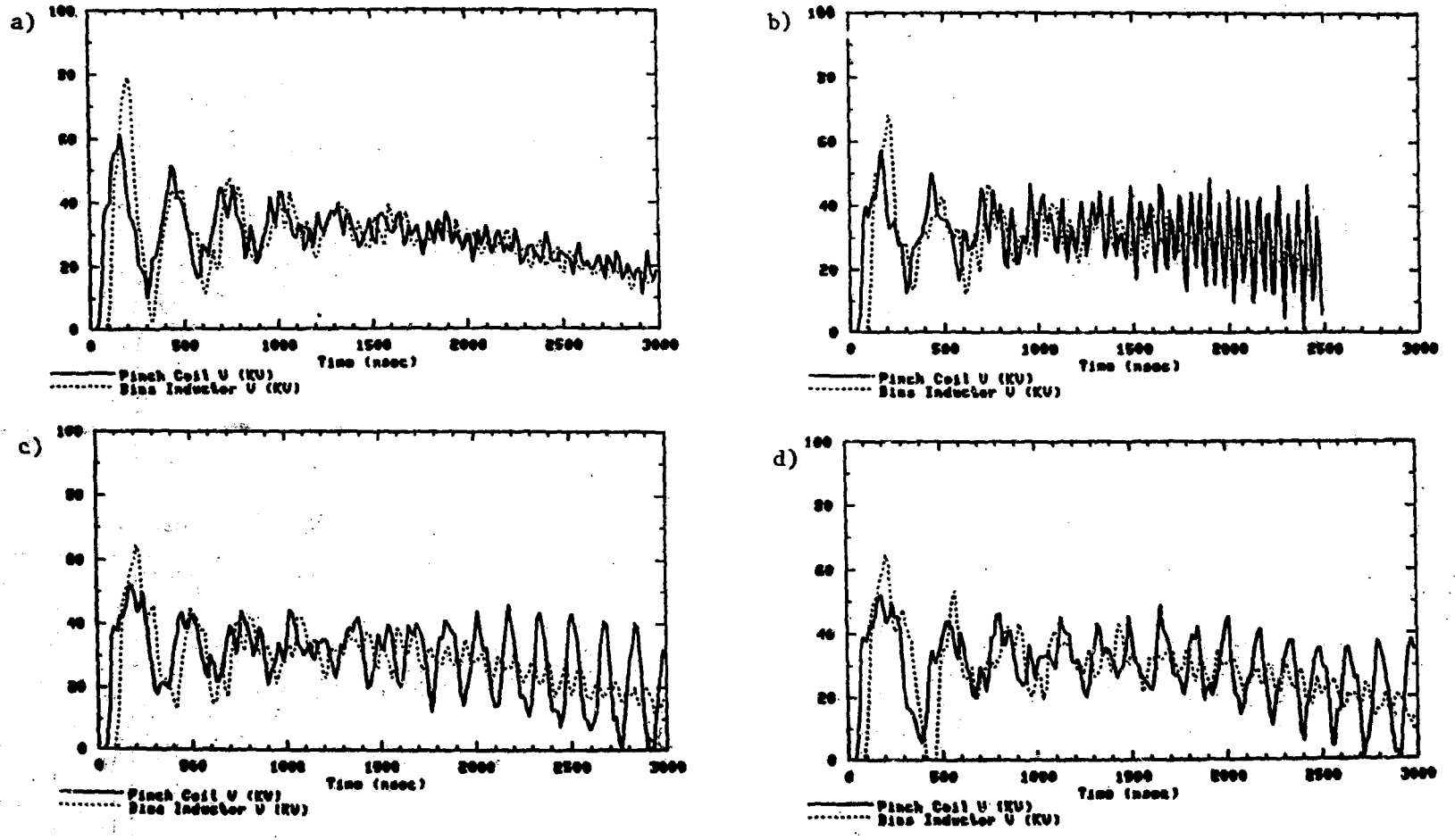


Fig. 9. Calculated voltages for the cases when 25% of the main bank discharges a) 50, b) 100, c) 200, and d) 500 nsec late.

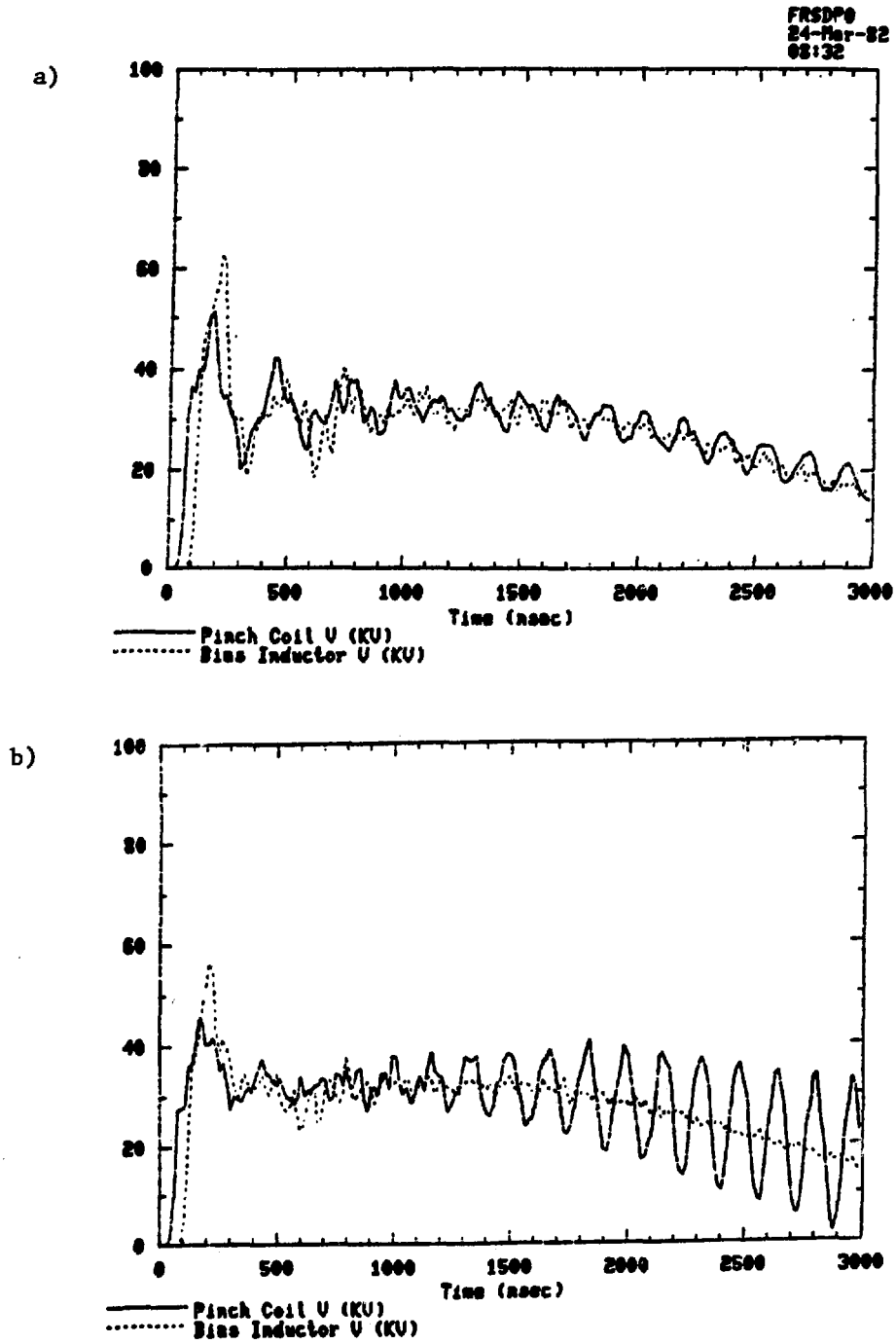


Fig. 10. Calculated voltages for the case when 25% of the main bank discharges 100 nsec late: a) 0.7-Ω damping resistor added; b) each main-bank capacitor equipped with a 3.6-Ω, 0.05-μF, 80-nH snubber.

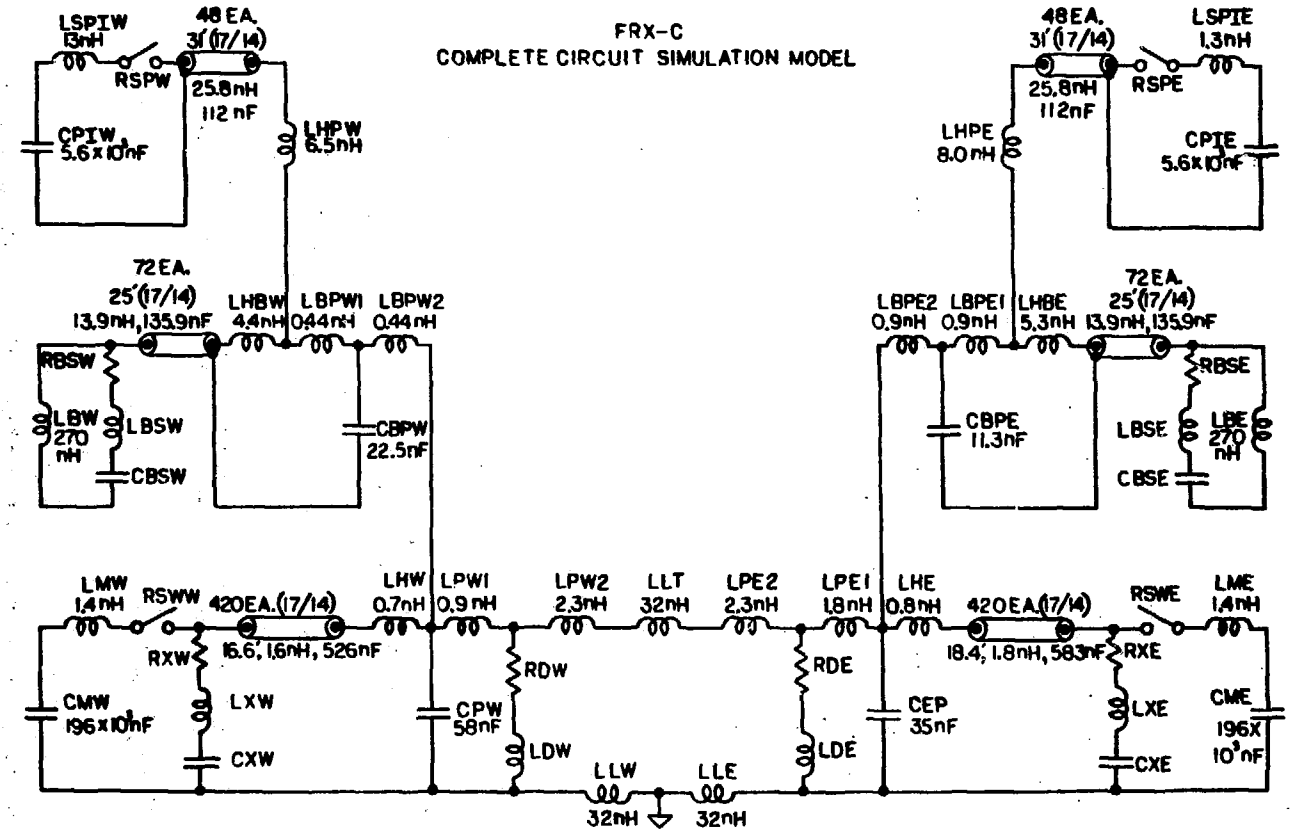


Fig. 11. Schematic diagram of circuit used in full FRX-C circuit capacitor bank calculations.

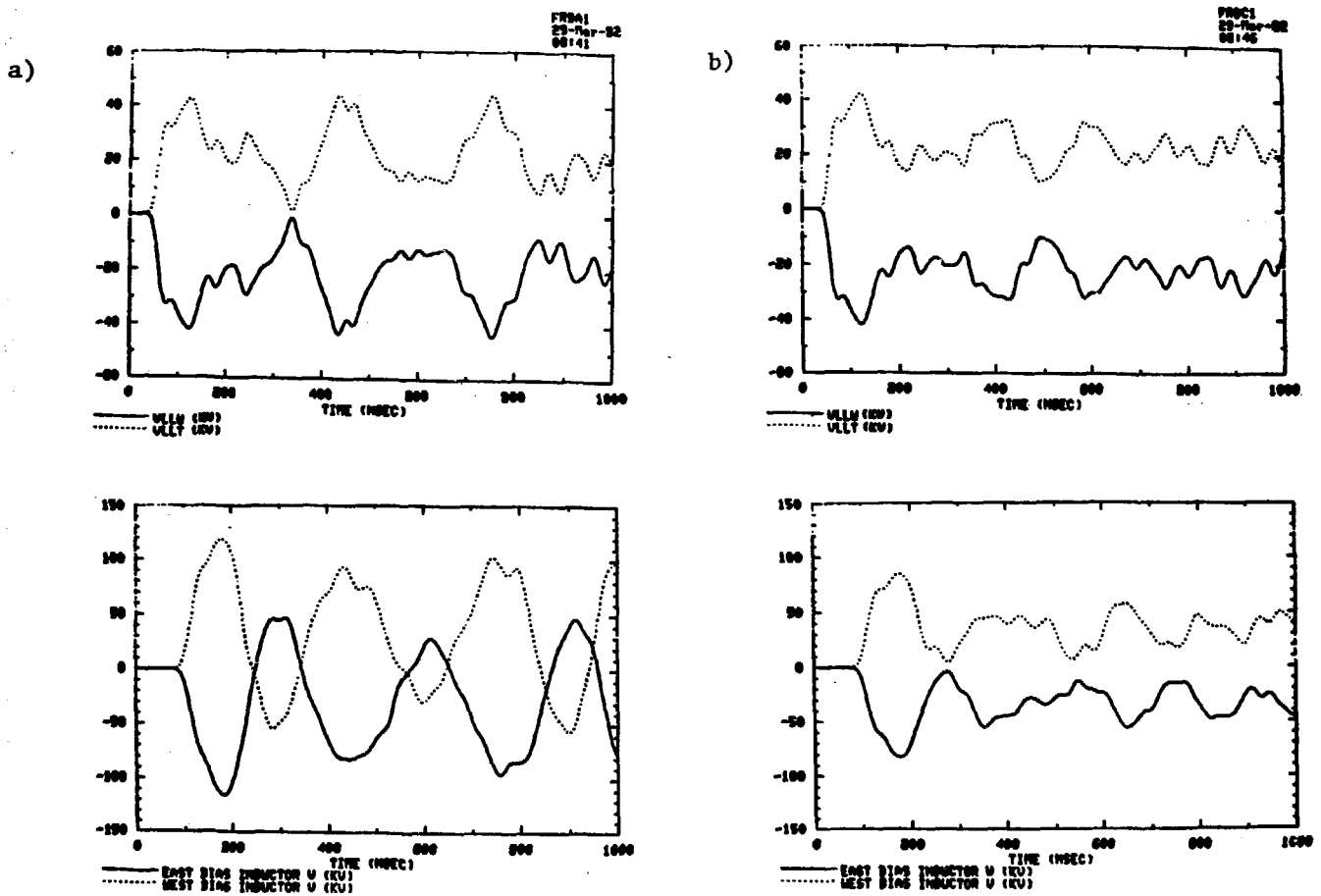


Fig. 12. Full bank calculations: load and bias inductor coil voltages a) with no snubbers; b) with normal bias snubbers.

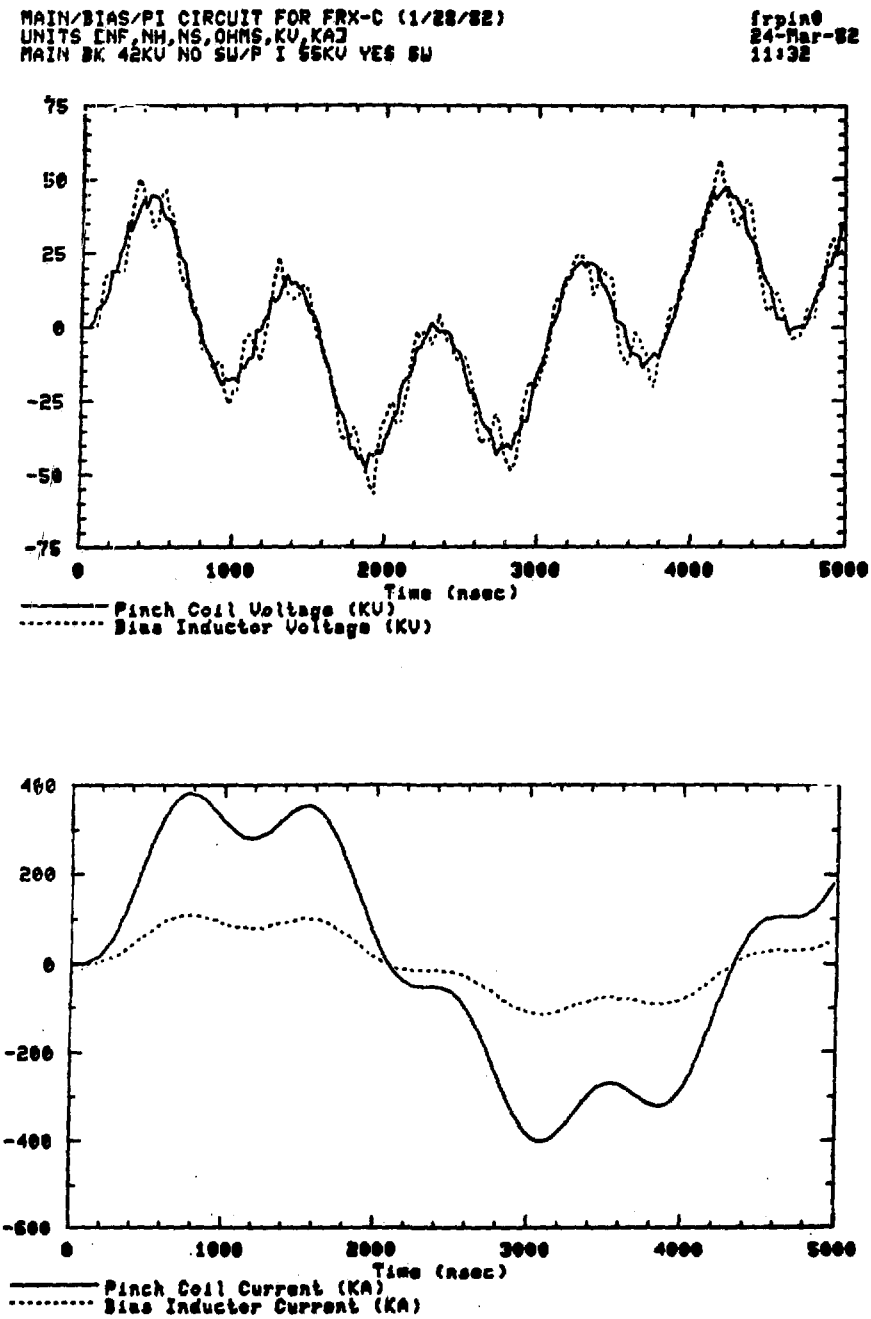


Fig. 13. θ-pinch studies: load coil and bias inductor voltages and currents calculated for a 55-kV PI-bank discharge. There are no snubbers or damping resistors.

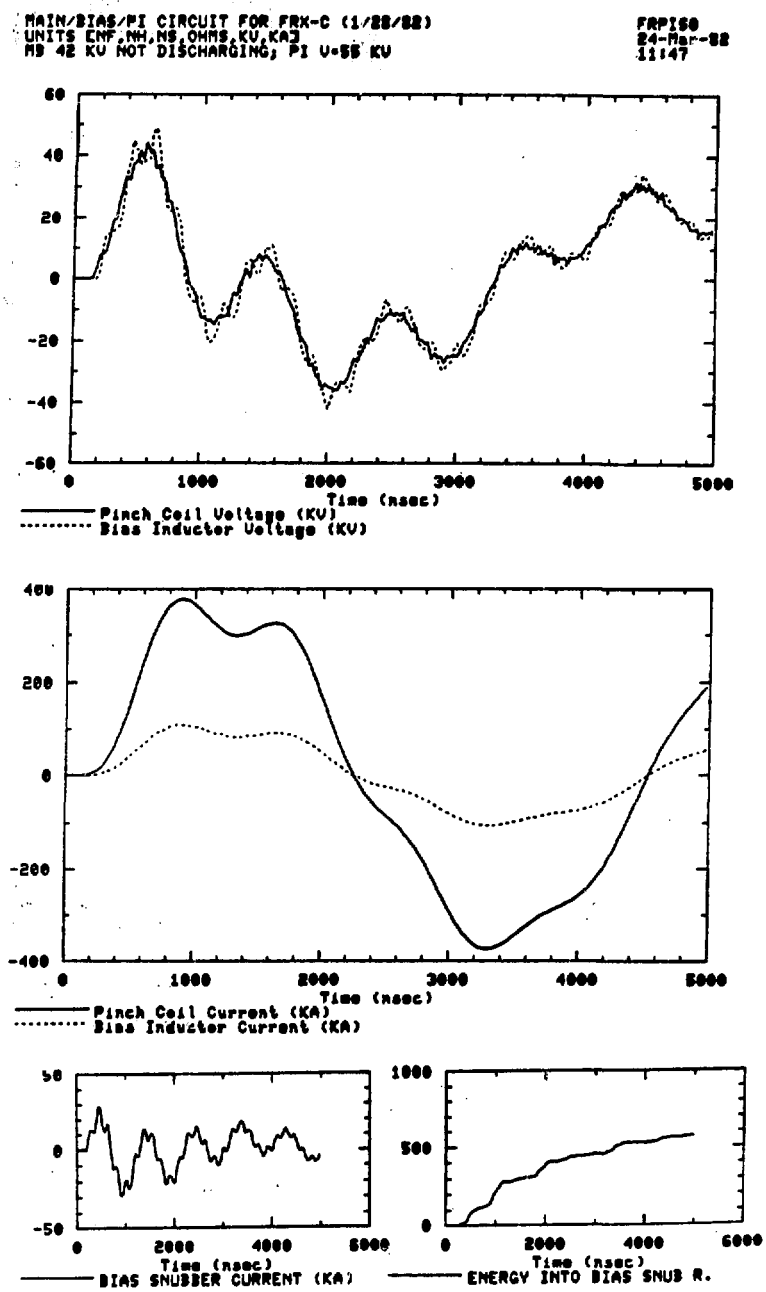


Fig. 14. Calculations for a 55-kV θ-PI discharge including the normal bias inductor snubber.

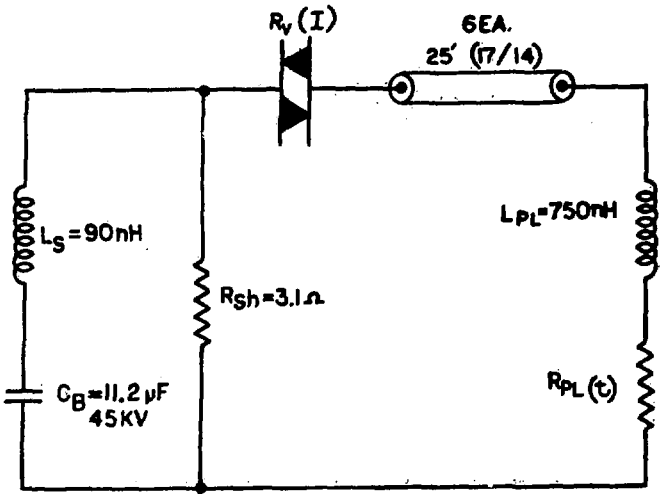


Fig. 15. Schematic diagram of z-pinch circuit.

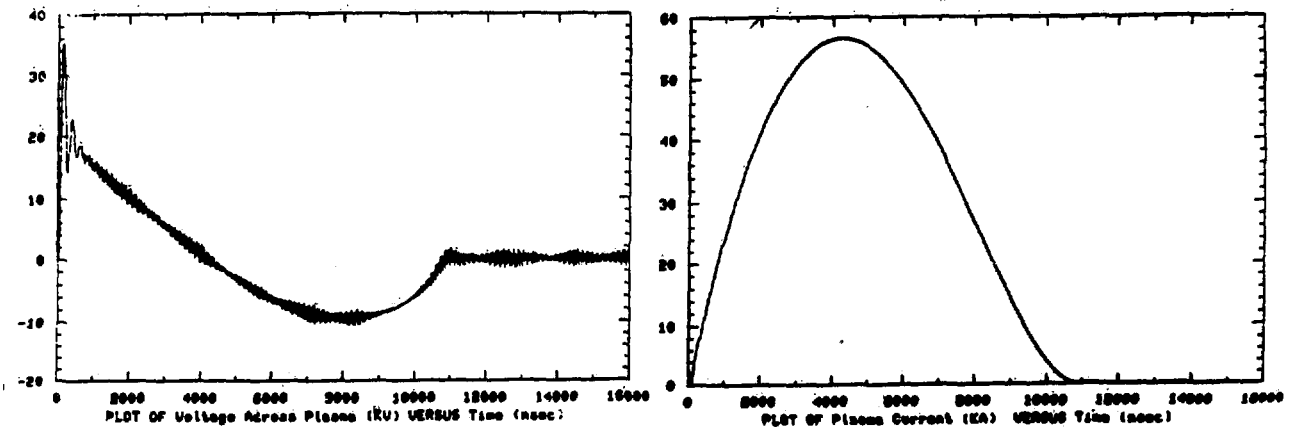


Fig. 16. Calculated voltage and current for a z-pinch PI discharge.

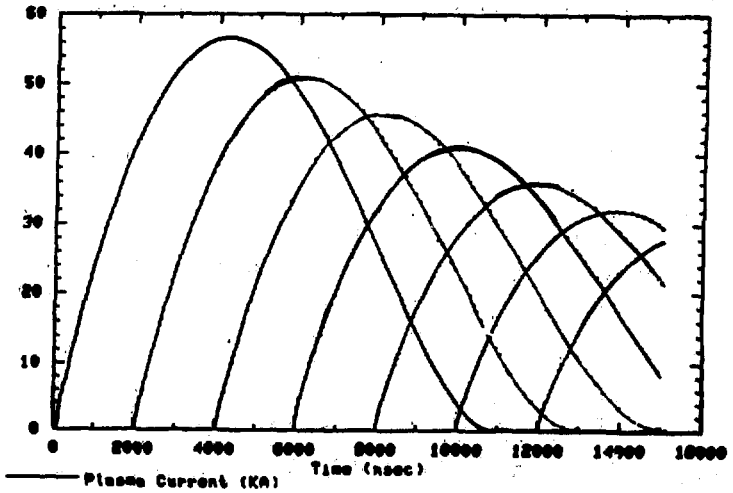


Fig. 17. Effect of delayed plasma breakdown on a z-pinch PI plasma current.