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A. GOSSÁNYI
E. VÉGH

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Hungarian Academy of Sciences

CENTRAL RESEARCH INSTITUTE FOR PHYSICS

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A. Gossányi, E. Végh

Central Research Institute for Physics
H-1525 Budapest 114, P.O.B.49, Hungary

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AFSTRACT

A computerized reactor control system has been operating at a 5 MW WWR-SM research reactor in the Central Research Institute for Physics, Budapest, for some years. This paper describes the power controller used in the SPC operating mode of the system, which operates in a 5-decade wide power range with ±0.5% accuracy. The structure of the controller easily limits the minimal reactor period and produces a reactor transient with consta..t period if the power demand changes.

АННОТАЦИЯ

Исследовательский ядерный реактор Центрального института физических исследований с мощностью 5 МВт управляется с помощью системы с ЭВМ. В докладе описывается аналоговый регулятор мощности, который используется в режиме SPC (управление задатчиками) системы с ЭВМ.

Регулятор мощности реактора работает в пятидекадном диапазоне с точностью ±0,5%. Построение регулятора позволяет просто обеспечивать ограничение по минимальному периоду, и при изменении мощности реактора создает переходный процесс с постоянным периодом.

KIVONAT

A Központi Fizikai Kutató Intézet 5 MW-os WWR-SM kutatóreaktora mellett számitógépes irányitórendszer üzemel. A dolgozat ismerteti a rendszer SPC üzemmódjában használt teljesitmény szabályozóját, amely 5-dekádos teljesitmény tartományban +0.5%-os pontossággal képes a teljesitmény tartására.
A szabályozó felépítése egyszerüen korlátozza a minimális reaktor periódust, és állandó periódusu reaktor tranzienst hoz létre teljesitmény változtatás esetén.

INTRODUCTION

A computerized reactor control system has been operating at a 5 MW WWR-SM research reactor in the Central Research Institute for Physics, Budapest for some years. This system can operate in SPC and DDC operating modes [1]. In the SPC regime it needs a power control unit which

- has the same dynamic behaviour over a wide power range,
- can maintain continuous operation throughout many decades of power without changing the measurement range,
- is simple and suitable for digital computers.

The described controller can be used over a 5-decade range with about 0.5% accuracy throughout in the whole range.

When the computer, operates in DDC mode the control system is used as a backup controller.

THEORETICAL BACKGROUND

Since the gain of the transfer function of a nuclear reactor is proportional to the actual power, if we wish to produce a level independent power controller, then its error signal has to be inversely proportional to this level. Let the result of comparison between the actual power and the power demand, the error signal, ε, be

$$\varepsilon = \frac{P_D - P}{P} = \frac{P_D}{P} - 1 = e^{\ln(\frac{P_D}{P})} - 1$$

$$\text{if } \left|\frac{P_D - P}{P}\right| < 10\%$$

$$\varepsilon \simeq \ln P_D - \ln P \qquad (1)$$

where P_D is the power demand and P is the actual level. If we introduce a power reference P_O, and the quantities in Eq. 1 are expressed in these units, we get

$$\varepsilon = \ln \frac{P_D}{P_O} - \ln \frac{P}{P_O} \qquad (2)$$

According to Eq. 2 we get a power independent controller if we compare the logarithmic values of the existing power level with the power demand instead of the linear ones.

The noise behaviour of a logarithmic comparator is virtually the same as that of a linear one because the logarithmic function can be regarded as a linear relationship in the vicinity of $(\frac{P_D}{P}) = 1$. Due to the logarithmic characteristic of the comparator, the noise on the measured value is almost the same in a wide power range.

The logarithmic characteristic has another great advantage over the linear one: this is the simple realization of a reactor transient with constant period if the power demand changes. The power demand must be changed according to an exponential low of time for a constant reactor period, i.e. its logarithm is a linear function of time. It means that we get a transient with constant period if we alter the logarithmic power demand with constant speed, and this speed is inversely proportional to the reactor period.

REALIZATION PROBLEMS

The block diagram of the logarithmi: power controller is presented in *Fig.1.*

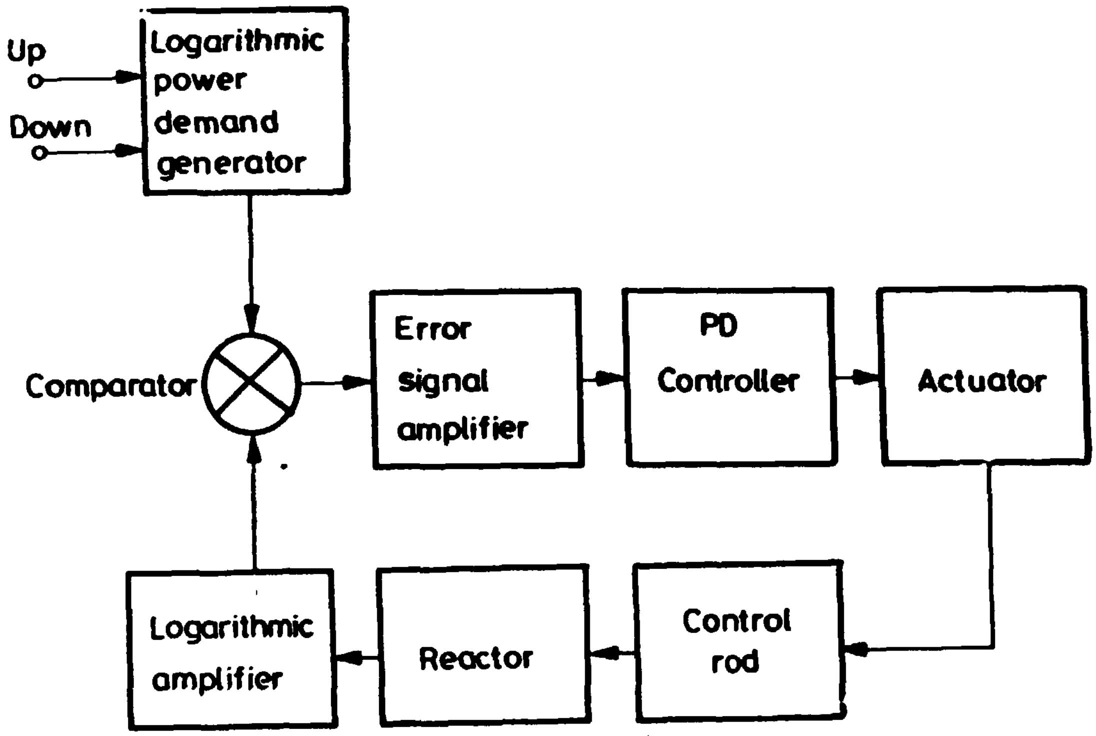

Fig.1

It can be seen that all the elements of the control loop are conventional expect for the logarithmic power demand generator. This generator consists of a simple up/down counter and a connected D/A converter.

The content of this counter is regarded as $\log(P_D/P_o)$. Let N be the content of the power demand counter

$$N = K_1 \lg \frac{P_D}{P_o} = K_2 \ln\frac{P_D}{P_o} \qquad (3)$$

where K_1 represents one decade and K_2 stands for an interval e. It is evident that

$$K_1 = K_2 \cdot \ln 10 = 2.3025\ K_2 \qquad (4)$$

The value of K_1 is determined from the necessary power resolution of the power demand generator. From Eq. 3 the value of one bit in the power demand register represents

$$h = \frac{P_D}{P_O} - 1 = 10^{\frac{1}{K_1}} - 1 \qquad (5)$$

that is, h is the smallest distinguishable step which can be produced with this unit. The accuracy of this generator h versus K_1 is shown in Table 1.

Table 1.

h %	0.1	0.2	0.3	0.4	0.5	1.0
K_1	2304	1152	768	577	461	231

The controller will produce a transient with constant reactor period if we change the content of the power demand counter by a constant rate n. Since K_2 represents an interval e, a very simple relationship exists between n and T, viz.

$$T = \frac{K_2}{n} = \frac{K_1}{2.3025 \cdot n} \qquad (6)$$

The comparator determines the difference between the output of the logarithmic current amplifier of our neutron detector and the output of the logarithmic power demand generator. It is evident that the two logarithmic elements must have the same characteristics, i.e. they must be fitted to each other. This fitting means the adjustment of two parameters of the D/A converter to those of the logarithmic current amplifier, namely

- the reference voltage,
- the zero point setting.

The voltage representing one decade must be adjusted to the reference; the power reference level P_o must be fitted to the logarithmic measuring channel with the zero point setting.

A simplified block diagram of the logarithmic power demand generator is given in *Fig.2*.

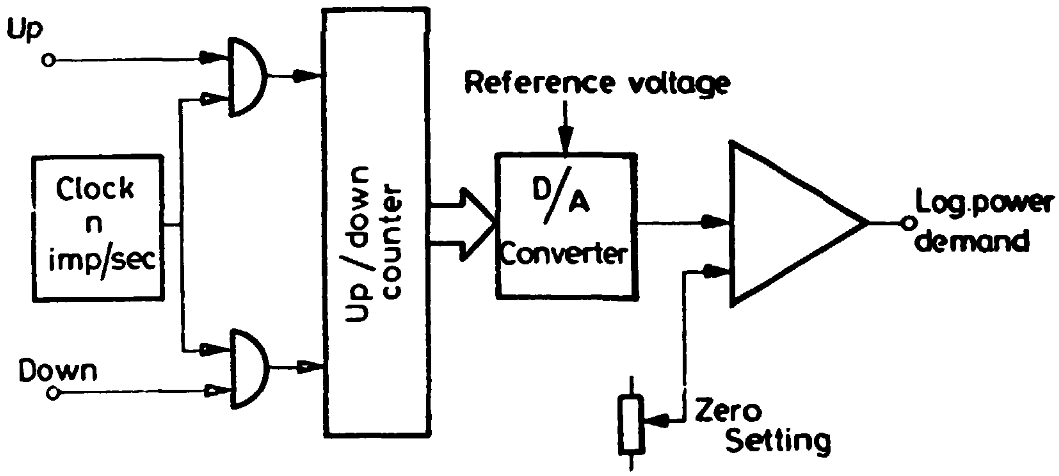

Fig.2

The gates of the up/down counter regulate the change in the power demand by controlling the pulse train of a clock. The clock has a pulse rate f which belongs to the permissible minimal reactor period T, in this way the period is easily limited.

The last problem to be solved is drift compensation. For various reasons the current of the neutron detector and the output of the logarithmic amplifier change slowly even at constant neutron level. In view of this, the controller needs to be calibrated to the thermal power of the reactor from time to time. The computer calculates the reactor power from the current of the neutron detector and determined d, the ratio of measured thermal power to nuclear power. If this ratio is not equal to one, it can be regarded as if the reference power P_o had changed to dP_o. In this case we change the value of P_o to this new one, so the content of the power demand counter will differ from the operator's demand and the controller will then change the power to the calibrated level.

DESCRIPTION OF THE LOGARITHMIC CONTROLLER

The nominal power of the reactor is 5 MW in our case and the controller can be used in a 5-decade power range. We chose P_o = = 50 W and K_i = 800. The power demand counter is 12 bits long, the output of the D/A converter changes in the 0 - 10 V range. The clock frequency was selected to 10 pulse/sec, which determines a 34 sec minimal reactor period.

The controller has two operating modes: "FOLLOW" and "CONTROL".

When the computer is in DDC regime or the reactor is controlled manually, the control unit operates as a backup and it works in the unusual, "FOLLOW" mode. In this case the unit does not perform the regulation but the content of the power demand counter is changed until the error signal becomes zero, i.e. the level base follows the actual power of the reactor. In this way the controller can search for the actual power and manual adjustment of the level base is not needed before switching it into "CONTROL" mode (see *Fig.3*). When the computer operates in SPC regime, the controller is in "CONTROL" mode and it is regulated by time modulated pulses at the "up" and "down" inputs. These pulses are produced by the SPC control program.

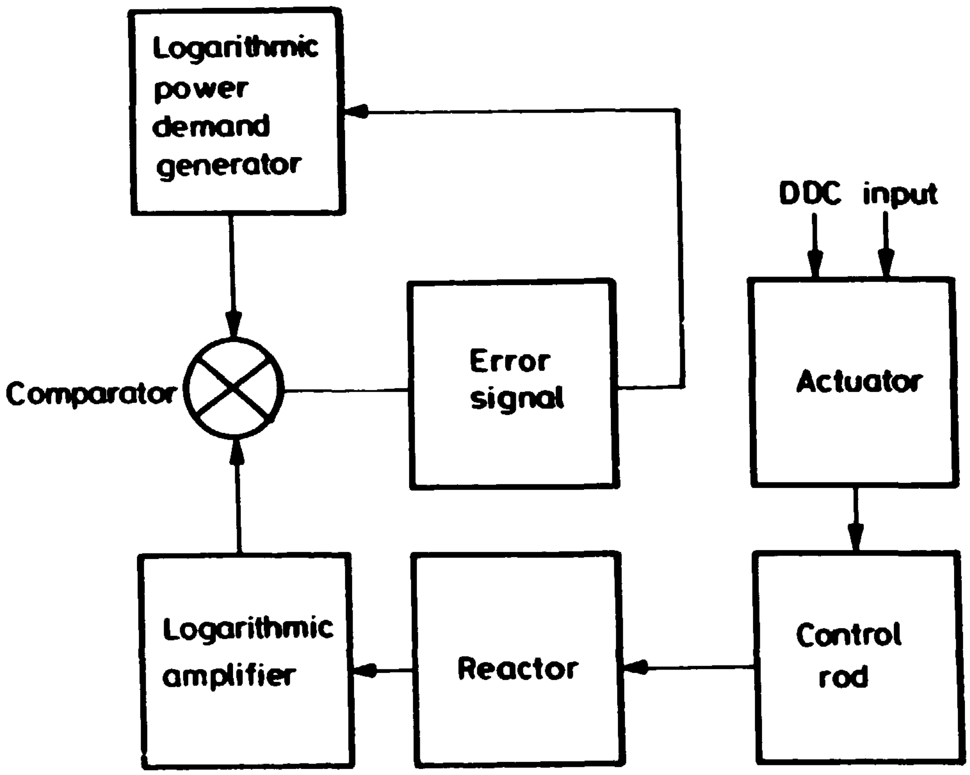

Fig.3

SPC ALGORITHM

Once second the SPC control program calculates the required power level using three different algorithms, viz. carry, hold, brake. If the difference between the operator power demand and the actual power is greater than 6% the carry algorithm gains control and it changes the power with constant period. The carry algorithm controls the reactor power near to the set point (6%), then the brake algorithm is activated. The brake algorithm gives control to the hold algorithm in the vicinity of the selected set point [2].

If the error signal is too large (greater than ± 3%) the controller automatically switches to "FOLLOW" mode and signalizes to the computer that it is out of control.

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Kiadja a Központi Fizikai Kutató Intézet
Felelős kiadó: Gyimesi Zoltán
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Nyelvi lektor: Harvey Shenker
Gépelte: Beron Péterné
Példányszám: 320 Törzsszám: 82-519
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