CONF-811012--67

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IPNS DISTRIBUTED-PROCESSING DATA-ACQUISITION SYSTEM

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J. R. Haumann, R. T. Daly, T. G. Worlton,
and R. K. Crawford †
Argonne National Laboratory
Electronics Division D817
9700 S. Cass Avenue
Argonne, Illinois 60439

Summary

The Intense Pulsed Neutron Source (IPNS) at Argonne National Laboratory is a major new user-oriented facility which has come on line for basic research in neutron scattering and neutron radiation damage. This paper describes the distributed-processing data-acquisition system which handles data collection and instrument control for the time-of-flight neutron-scattering instruments. The topics covered include the overall system configuration, each of the computer subsystems, communication protocols linking each computer subsystem, and an overview of the software which has been developed.

Introduction

The IPNS Facility

The Intense Pulsed Neutron Source (IPNS) began operation at Argonne National Laboratory in May, 1981. This facility provides a source of slow neutrons for neutron scattering and of fast neutrons for neutron radiation damage studies. At IPNS a heavy-metal target is bombarded with protons from a 500 Mev accelerator at a 30 Hz repetition rate, producing pulses of fast neutrons by the spallation process. For neutron scattering studies these neutrons are moderated by small hydrogenous moderators to produce pulses of slow neutrons.

From its conception IPNS has been intended to be a "user-oriented" facility with major emphasis placed on satisfying the needs of an outside user community, many of whom are only occasionally involved in neutron scattering. The facility provides 12 horizontal beam lines which can accommodate 12-15 instruments, some of which have not yet been defined.

Data Acquisition Requirements

Although physically the time of flight instruments vary considerably, they all involve qualitatively similar data acquisition and control requirements. Each of the instruments appears to the data acquisition system as a collection of detectors or detector elements, from which data is collected concurrently. Each event detected must be identified with a space and time descriptor. The spacial descriptor corresponds to the physical location of the detector, or detector element in the case of position sensitive detectors, in the instrument. The time descriptor corresponds to the time of arrival of the event at the detector with respect to the time of arrival of the protons at the heavy metal target. This time of flight of the neutrons is a function of their energy and the total flight-length. The energy range and flight-length needed for some instruments mandate a time descriptor with a magnitude up to 0.1 seconds, while the desired resolution for some instruments requires the time descriptor to resolve 1/8 microsecond time increments. The number of detector elements per instrument can vary from a few to as many as 2^{16}. Each event detected is binned in a position-time histogram according to a user-defined algorithm. These histograms can contain from a few hundred to several million bins, depending on the type of instrument and the spacial and time resolutions desired. The average data rates expected at the various instruments vary from a few hundred to 20,000 events per second with instantaneous rates reaching as high as 1 MHz.

In addition to data acquisition functions, the system must include user-friendly interfaces between the users and each of the instruments. Each such interface must provide for control of the instrument, for preliminary data reduction, for display of data, and also for data storage and backup of the raw data. During experimental runs, these user interface functions should not affect the rate at which data can be acquired.

Since all of the instruments are not yet defined, the hardware and software for the data acquisition system were designed so that future expansion of the number of detector elements and data rates can be accomplished as the need arises without requiring a major redesign effort. Also since the manpower available to implement the data acquisition system within the allotted time was limited, the system was designed with the intent of purchasing as much of the equipment as possible from commercial vendors.

System Description

To fulfill the requirements of the data acquisition system it was decided to provide each instrument with a number of processors dedicated to specific tasks. The tasks were divided into five main categories:

1. Data acquisition and histogramming.
2. User interface and instrument control.
3. Video display of data.
4. Data analysis and bulk storage.
5. Communication between the various processors.

Figure 1 contains a block diagram of the distributed processor configuration used for the data acquisition system at IPNS. The separate subsystems are discussed in turn below.

Data Acquisition

The data acquisition hardware used for event time digitization is implemented in CAMAC, with each data acquisition module containing a First-In First-Out (FIFO) buffer to accommodate the instantaneous data rates expected in some of the instruments. This custom designed CAMAC hardware allows for easy expansion as the number of detector elements increases, and provides a standardized interface into the data acquisition processor.

The MULTIBUS (Trademark of Intel Corp.) was chosen as the system bus for the data acquisition

computer because of the large array of support products available for this bus structure. The data acquisition Multibus system is made up of four boards plus memory. The four boards are:

1. A Z8001 based single board computer.
2. An interface to the CAMAC controller.
3. An interface to the communications processor.
4. An I/O board containing both serial and parallel I/O ports.

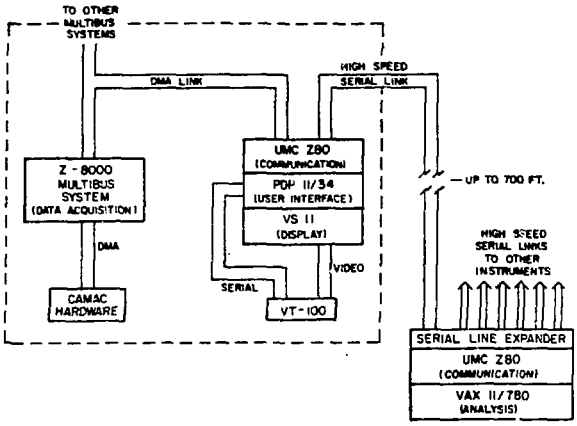

Figure 1 A block diagram showing one instrument computer system (within dotted lines) and its link to the analysis computer.

The two interface boards, along with the CAMAC modules noted above, are the only custom designed hardware in the system. Memory boards with capacities of 128 Kbytes and 512 Kbytes are used, with the amount of memory contained in each system being dependent on the instrument. Each Multibus system has at least 256 Kbytes of RAM memory which is used for both program and data storage.

The data acquisition computer uses a 16-bit Z8001 microprocessor. This processor was chosen mainly for its ability to directly address the large amounts of memory needed for building the space-time histograms which can contain several million elements. The data acquisition computer is a Multibus compatible product built by Central Data Corporation. This computer board provides 24 memory address lines to allow addressing of up to 16 megabytes of memory, which is sufficient for all instruments currently envisioned. It also contains a 2K word PROM monitor which on power-up is written into and executed from RAM. This monitor provides on-line debug capabilities for the data acquisition programs.

The data acquisition programs for the Z8001 are written and assembled using the PDP-11 user interface computer as a program development system. The histogramming programs are basically table-driven routines to allow flexibility in the formatting of the histograms. These tables are generated by routines on the PDP-11 when the user sets up the run, and are then down loaded to the Z8001 at run time.

During a data acquisition run, detected events fill the FIFO buffers in the CAMAC hardware causing LAMs. A special scanning module determines the crate and slot number of the module which is requesting service and passes this ID as an 8 bit byte to the Z8001 via a parallel I/O port. Loading this port causes an interrupt to the Z8001. Upon receipt of this interrupt, the Z8001 programs the CAMAC controller for a DMA transfer of the data from the FIFO in the CAMAC module requesting service to a 2K byte software-controlled circular buffer in the processor data memory. This block of data is then given a header containing the number of bytes in the block and the crate and slot number of the module from which the data was read. During a run the data acquisition computer gives highest priority to inputting the raw data from CAMAC and building histograms from this data.

For non-area-detector modules, the raw data stored in each module's FIFO is organized as 24 bit words which contain 3 bits of input ID along with the time information. These 3 bits are combined with the crate and module number stored in the block header to make up the position data for the event being stored. The Z8001 then uses this position data as an index into a table which contains the address of the start of the histogram for that detector position. This table also assigns a type number to each detector position, and this type number is then used as an index into a second table which contains histogramming parameters and limits for the time portion of the data. The processor uses these parameters to adjust the time data for the resolution desired for that detector and also to test that the data falls within a time range of interest. Two additional tables addressed according to position and to time respectively, provide scaling parameters and shifting parameters which may also be applied to the time portion of the data. The scaled and shifted time data is then used as an index to the proper bin within the histogram, which is then incremented to account for the event. In this way a completed histogram is a 2-dimensional array of the form I(p,t), where "p" is the position of the detector and "t" is the time of arrival of the event at that position. This software also has the unique capability of storing a given event more than once. This is equivalent to having parallel time-of-flight analyzers. This multiple histogramming allows the data to be collected with and without scaling or shifting corrections. It also permits collection of high-resolution data over special time regions.

This histogramming software is designed so that various options in time scaling and limit checking can be eliminated to allow acquisition of data at higher average rates. If all options are chosen, the average data rate that can be histogrammed is about 2000 events per second. Slightly different data organization and histogramming software are used for area detectors. In this case the CAMAC modules encode each event as 16 time bits and 16 position bits. Histogramming is again table driven, but in this case using a direct mapping scheme with minimal computations made on the incoming data word. In this mode the average data rates can reach 16,000 events per second.

User Interface

The user interface computer is a DEC PDP 11/34 containing 256 Kbytes of memory, two RL-02 10 Mbyte disk drives, a VT-100 raster scan video terminal, and an LA-120 hard copy terminal. This computer runs under DEC's RSX 11/M multi-tasking operating system. It also contains an interface to a second CAMAC controller which is used to control various devices associated with the instrument, such as stepping

motors, sample changers, or shutters.

All communication between the user and the data acquisition system takes place through the VT-100 terminal. The commands are executed under control of the RSX Monitor Console Routine (MCR) or a special command interpreter.

All data collection is organized around the concept of a run. All parameters defining a particular run, including the histogramming tables discussed above, are set up in a run file header, and the histogrammed data is later appended to this header to make a complete run file which contains the information necessary for subsequent data analysis. User commands have been implemented to set up histogramming tables tailored to a specific experiment; to schedule, start, and stop data acquisition for a run or a series of runs; and to print or display data or other run information in various formats on the graphics display terminal. Additional commands are available for diagnostic and maintenance purposes.

Set up of the run file headers has been kept as simple as possible consistent with the wide flexibility offered. As much of this information as possible is obtained automatically. If the method of data collection is the same as in a previous run, only the title and user name are required as input to create a new run file. However the user has the option of selecting minimum and maximum times of interest and the resolution desired, as well as time-scaling and time-shift corrections for each detector. If desired, the resolution may be halved after a given number of channels to allow compression of the lower energy portion of the spectrum where there are not many peaks. Time-shift corrections can be linear or can be given as a function of time to allow energy dependent corrections for neutron emission-time delays from the moderator.

Display

The display processor is a VS11 bit slice processor produced by the Computer Special Systems group of DEC, which provides for raster graphics display with a resolution of 512 x 512 pixels with up to 16 colors or intensities.

The basic DEC VS11 video graphics system consists of a Sync-generator/Cursor-control module, an Image Memory module, and a display Processor module, and also includes a joystick assembly. On most of the systems the VS11 interfaces to the VT-100 video terminal. Software controlled split-screen viewing then allows the VT-100 to serve as both a video terminal and as a graphics display monitor simultaneously.

The display processor is microcoded to provide an instruction set including vector, point, graphplot, run-length, and bitmap instructions as well as image memory readback and joystick/cursor instructions. The pixel data output by the display processor is stored in the image memory modules, from which it is continually "read" to the video monitor.

Instructions and graphic data are placed in a "display file" in the PDP-11 memory, where they are accessed in a DMA operation by the image processor. Programming of graphic displays consists of setting up the appropriate display file which can be updated concurrently with its access by the VS11 image processor. The VS11 operation is synchronized to the PDP-11 software, where necessary, by the appropriate use of "start" and "stop" commands to the VS11. Otherwise the VS11 and PDP-11 operations are asynchronous.

The existence of the "point" and "vector" graphic modes makes it relatively simple to interface the VS11 to standard "pen-plotting" graphics software packages. We have interfaced the VS11 instruction set to such a pen-plotting software graphics package, and this package is used for display of histogram files stored on disk. However, "live" data updating is programmed directly with the VS11 instruction set to achieve greater plotting speed. The "bitmap" graphic plotting mode is used for "density plot" representations of two-dimensional slices through histograms.

The display of "live" histogram data being accumulated in the MULTIBUS memory involves the concurrent and asynchronous operation of the four front end processors. The PDP-11 determines, on the basis of user input, which portion of the histogram is to be displayed. The communication processor supervises the transferring of this histogram data to a static common region in the PDP-11 memory several times per second. Continuous-loop applications software operates on the data in this static common, performing scaling, changes of units, etc., and then places this data in proper format in a display file. The display processor in the VS11 cycles through the display file and converts the data to pixel information and stores it in its image memory. This software produces rapid display updates which provide a good sense of the "live" nature of the data, as it is being histogrammed by the Z8001.

Data Analysis

A DEC VAX 11/780 is used for complex data analysis and shared I/O with all instrument systems. This data analysis computer includes 1 Mbyte of RAM memory, a floating point accelerator, a 516 Mbyte disk (RP07), a 67 Mbyte disk (RM03), a 10 Mbyte disk (RL02), a 800/1600 bpi magnetic tape drive, a Versatec printer-plotter, a Printronix line printer, modems, a number of VT-100 terminals, and a VS11 graphics display.

This data analysis computer is meant to receive data from the various instrument computers via the communication interface. The data is then either stored or analyzed by routines provided by the user. After reduction the data can be plotted and/or printed by the various output devices connected to the VAX or it can be shipped back to the instrument system for display or further manipulation.

Communication

The communication links between the various processors are fundamental to the success of any distributed processing system. In the IPNS system communication is handled by yet another set of processors which control two functionally different data links.

1. PDP 11 - Z8001. This is a Direct Memory Access link between the Unibus and Multibus which includes the mechanisms necessary to coordinate the activity of the tightly coupled PDP 11/34 and Z8001 processors. Its operation is essential for control of data acquisition.

2. PDP 11 - VAX. This is a serial high speed synchronous link between the loosely coupled PDP-11 and the VAX. Its main function is to move large data files between the two processors and its operation is not essential to data acquisition.

PDP 11/34-Z8001 Link. The PDP 11/34 - Z8001 link is implemented with two boards, a Unibus Micro Controller (UMC) from Associated Computer Consultants on the Unibus and a custom Multibus interface on each Multibus. The UMC board can control seven Multibus interfaces, thus allowing each PDP 11/34 computer to link with up to seven independent Z8001 Multibus systems.

As shown in Figure 2, the UMC provides a Z80 micro-computer with compatible Z80 peripheral chips together with Unibus DMA circuitry, 32 single byte registers accessible from the Z80 and PDP-11, and a programmable PDP-11 interrupt vector. The local Z80 bus from the UMC is extended via a flat cable to interface cards in each linked Multibus. Each Multibus interface provides a bidirectional 64 word FIFO thru which data flows asynchronously between the local Z80 bus and the Multibus, DMA control logic and addressing registers for Multibus to FIFO transfers, 2 single-byte registers accessible as I/O ports from the Z80 and Multibus, and controls to reset the Multibus and generate a low priority Interrupt on the Multibus.

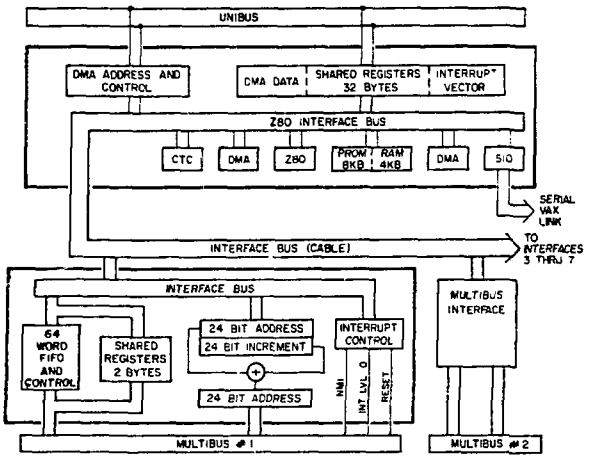

Figure 2 The communication link between the PDP-11 and Multibus computer systems.

Each new 24 bit Multibus address is generated by hardware addition of a 24 bit increment register and a 24 bit address register. This addressing scheme allows the DMA transfer of non-contiguous data and is used, for instance, to transfer time slices through space-time descriptor organized histograms. The data path for large block transfers between Multibus and Unibus is, MULTIBUS to FIFO to Z80-DMA to UNIBUS, and is handled entirely in hardware. The Z80 CPU is used mainly to accept I/O parameters from the PDP 11 in order to set up MULTIBUS and Unibus address registers and to program the Z80-DMA. The Z80 CPU also uses shared registers and interrupts as mechanisms to handle DMA initiations and completion sequences.

Besides transferring large data blocks directly between the Unibus and MULTIBUS the communication processor system also passes short command blocks to the Z8001 from PDP-11 tasks. The command and the parameters needed to complete the command are located in the Subfunction byte and 6 Parameter words which are included in every PDP 11 RSX I/O request (i.e. the QIO executive directive). The Z80 passes these command blocks to fixed Multibus locations and interrupts the Z8001 at a low priority. The PDP 11 I/O completion then awaits the interpretation and implementation of this command block by the Z8001. The communication processor can handle up to 32 separate PDP-11 I/O channels. Since the PDP-11 needs only one channel per MULTIBUS for sending a command block, all MULTIBUS systems attached to the PDP-11 may be executing commands simultaneously.

PDP 11/34-VAX Link. The functional layering of the PDP-11 to VAX link can be viewed as in Figure 3. All operations at the transport layer are handled by hardware and software located in separate Z80 microcomputer systems. One Z80 computer system is located at each end of each physical link shown in Figure 3. Higher levels in the figure are handled entirely by software in the host PDP 11 or VAX computer. The software for this link is now under development.

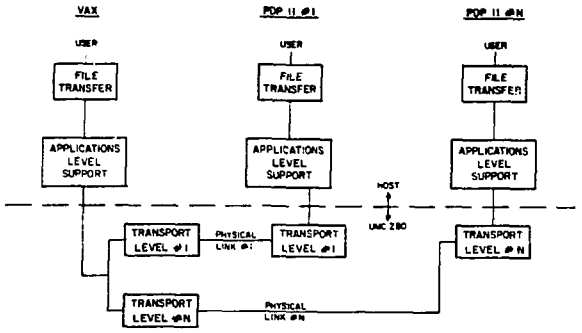

Figure 3 The high speed serial link between the VAX and PDP-11 computer systems.

Conclusion

The IPNS data acquisition system described, including the CAMAC hardware necessary to operate 600 proportional counter detectors, and one area detector has gone from conception to operation in 2-1/2 years. Only two custom interface boards were necessary to bring the distributed processing system into operation. This can be attributed to the design philosophy of using an architecture based on industry standards and supported by various manufacturers. The system, including instrument subsystems for five instruments has been operational since May of this year. During this period of operation, the system has performed up to the design specifications.

Future Plans

Expansion of the data acquisition system to include more instruments is now underway. In this expansion the user interface PDP-11 computers will be shared with several Multibus data acquisition processors. By using separate Multibus systems for each instrument, there will be minimum interaction in data collection between instruments. Future plans also include increasing the data rates that can be histogrammed by implementing processor boards with higher speed CPU's and on-board program memory, which permits the use of multiple processors on one Multibus.

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† Work performed under the auspices of U.S. Dept. of Energy.