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APPLICATION OF LOCAL AREA NETWORKS TO ACCELERATOR CONTROL SYSTEMS AT THE STANFORD LINEAR ACCELERATOR*

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Summary

The history and current status of SLAC's SDLC networks for distributed accelerator control systems are discussed. These local area networks have been used for instrumentation and control of the linear accelerator. Network topologies, protocols, physical links, and logical interconnections are discussed for specific applications in distributed data acquisition and control sytems, computer networks and accelerator operations.

Introduction

This paper describes SLAC's experience with local networks that are implemented with synchronous data link control protocols. These networks have been developed over a four year period and have been used for distributed instrumentation and control functions as well as for interprocessor communications. This paper provides a tutorial description of the SDLC protocol and a brief discussion of several data encoding schemes used at SLAC. Selected applications of these networks are presented to illustrate some of the organizational possibilities of SDLC networks, and the specific electronic hardware used in these networks is discussed.

Discussion of the SDLC Protocol

The SDLC (Synchronous Data Link Control) is a bit oriented protocol for the transferral of serial information over a physical data link. It corresponds to Layer 2, the data link layer, of the International Standards Organization Open Systems Network Model. The protocol frames the beginning and the end of all messages with a special control character (FLAG), and ascribes a positional significance to the bits, organized into various fields, following the opening FLAG. Figure 1 represents the basic serial structure of an SDLC message.

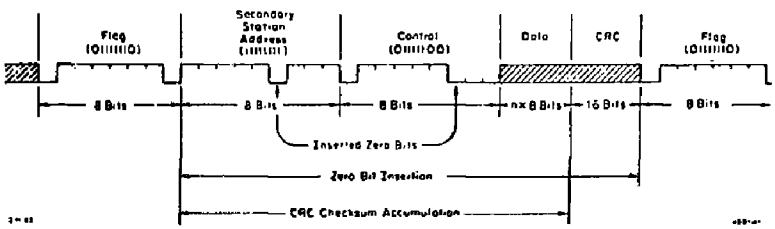

Fig. 1. SDLC Protocol

Referring to Fig. 1, the FLAG is the eight-bit pattern '01111110', the SSA is an eight-bit secondary station address used to identify the sender or to direct transmission to a specific receiver, the CONTROL field is an eight-bit user defined field, the DATA field (as implemented at SLAC) is an arbitrary number of eight bit bytes, and the CRC field is a sixteen-bit cyclic redundancy checksum, calculated from the SSA, CONTROL, and DATA fields which are appended to the message before the closing FLAG.

To prevent the data field from possibly containing the special FLAG character, the SDLC protocol specifies a zero-bit insertion in the transmitter after transmitting any five consecutive one-bits, and also specifies the zero-bit deletion in the receiver upon receipt of five continuous ones followed by a zero. This bit-stuffing and bit deletion is transparent to the external link user.

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Certain advantageous features of the SDLC protocol are obvious. Each message contains an implicit message destination (or source) in the address field, and this allows point-to-point communication over a party line common communications channel. The address-specific messages eliminate irrelevant messages in the unaddressed receivers. A special secondary station address (FF hexadecimal) is implemented to allow "broadcast" messages to be received by all receivers

Another feature of the SDLC protocol is error checking. The sixteen-bit CRC (cyclic redundancy checksum) word appended to each message provides each receiver with a direct check on data integrity, and allows the receivers to request another copy of the message if it is received damaged

The zero-bit insertion algorithm, in conjunction with NRZI data encoding insures that data transitions will occur at least once every seven bit frames and allows AC coupling of the physical data link.

The availability of commercially developed LSI SDLC controllers and complete board level products speeds design and development of SDLC networks. Also, the specification of the data link protocol allows varied hardware units to communicate over varied physical links simply by changing the interfaces. It is this flexibility to interconnect dissimilar hardware that we have found to be among the most useful of the SDLC protocol features.

Baseband Encoding Schemes

The interface from the data link level of protocol (SDLC) must take into account the unique characteristics of each physical link. The simplest case takes place when the physical link can accept unencoded SDLC data. There are two issues which still need to be dealt with, bandwidth limitations and receiver synchronization. NRZ encoding requires a bandwidth from 0 to (bits/sec)/2 Hz, but the receiver obtains timing information only when a transition in the bit stream takes place, necessitating moderately complex clock recovery and synchronization circuitry. Using NRZI encoding, SDLC's zero-bit insertion generates transitions during both long strings of ones and zeros, while still being economical in terms of bandwidth. Clock information may also be sent along with a bit stream, as in PDM, which generates a transition at the start of every bit frame. A variant of PDM, called RO (Return to One), in which zero-bits are sent as a low-going pulse and one-bits leave the line at the high level, allows simple clock recovery and frequent clock resynchronization, but with twice the required bandwidth of NRZ encoding. As SDLC controller integrated circuits have tight specifications on receive clock duty cycle, care must be exercised in the choice of the baseband encoding scheme, as distortions will occur due to nonlinearities in the physical link (as in modems with AGC) or dispersion.

SLAC's networks have utilized several data encoding schemes. The original PEP network uses a pulse duration modulation (PDM) technique, which is easy to generate and inexpensive to recover, as the data stream is self-clocking. However, PDM encoding is quite wasteful of bandwidth, requiring a modulator-demodulator bandwidth four times the data rate.

Later networks use a variety of encoding, including biphase, NRZ, and RO (Return to One). Each technique has it's own trade-offs in ease of implementation and required modulator bandwidth. Figure 2 illustrates several of these encoding techniques.

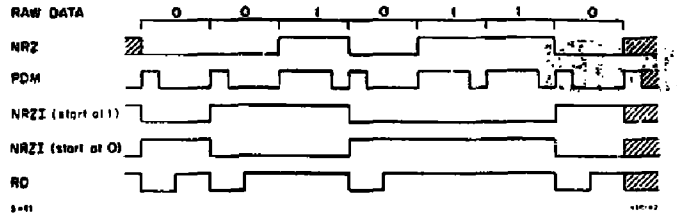

Fig. 2. Baseband encoding schemes.

Baseband Electrical Specifications

The SDLC transmitter/receiver modules described use either baseband TTL or differential TTL (RS-422) levels to encode the SDLC messages. These formats are not well-suited to data transmission over long distances, and to allow remote communication both RF and baseband network systems have been developed at SLAC. The RF networks have utilized commercial modems and commercial CATV components, and are described in a paper at this conference.[1] The baseband systems designed at SLAC (i.e., the long line driver and PDM multiplexer) utilize a bipolar logic level encoding that encodes the edges in the input signal. This encoding system produces no dc component in the encoded data, and allows transformer coupling and ground isolation of network nodes. This network technique also allows duplex communication over a single coaxial cable, and reduces the cable plant required to a single RG-214 cable between nodes.

By way of example, we have selected a few networks which illustrate the applications of these techniques.

PEP SDLC CAMAC System

The Positron-Electron-Project at SLAC uses 48 CAMAC crates for I/O control of the storage ring hardware. These crates are physically distributed over the 2200 meter PEP ring, and the computer system is implemented with a distributed network with seven remote ModComp II minicomputers acting as data concentrators.[2] Each ModComp II uses a link controller[3] to communicate with its remote CAMAC crates[4] up to 200 meters away. These SDLC networks operate at 1 megabaud data rate, and use a PDM modulation encoding on a differential TTL RS-422 link implemented over twisted pair cables.

VAX-ModComp Link

During the development of the PEP I & C system, it became desirable to add additional computing power (a VAX 11/780) to the original ModComp computer network. These two dissimilar machines were connected via a SDLC network that is illustrated in Fig. 3. This network is used for refreshing the VAX I & C data base via the ModComp IV's and for direct I/O operations on the remote crates that originate in the VAX. This network uses a VAX CAMAC Channel (VCC) — SDLC link driver[5] combination to communicate with a link controller connected to the I/O bus of the ModComp IV. This system uses the PDM data format and RS422 signals on twisted pairs to implement the link.

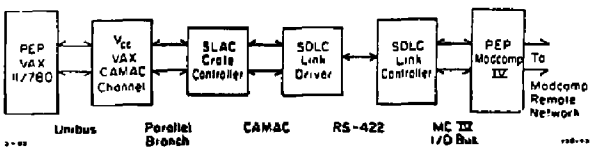

Fig. 3. VAX-ModComp link.

SLC Interim CAMAC System

Development work on the Stanford Linear Accelerator and the need to instrument the linac for the SLC ten-sector tests required a distributed CAMAC system to be installed and operational in September 1982. This network, which uses twenty CAMAC crates distributed over ten sectors (1 km), controls the SLC damping ring and the linac focusing magnets and provides CAMAC I/O functions from the VAX 11/750 in the main control center 3 km distant. Figure 4 is a block diagram of this system, and shows the RF link between MCC and Sector 1 and the baseband link between Sector 1 and the CAMAC crates from Sectors 0 through 10. A VAX CAMAC Channel — SDLC link driver-modem combination is used to connect the VAX to the 1 Megabaud SDLC network, and PEP SDLC crate controllers are used to provide the SDLC — CAMAC interconnection.

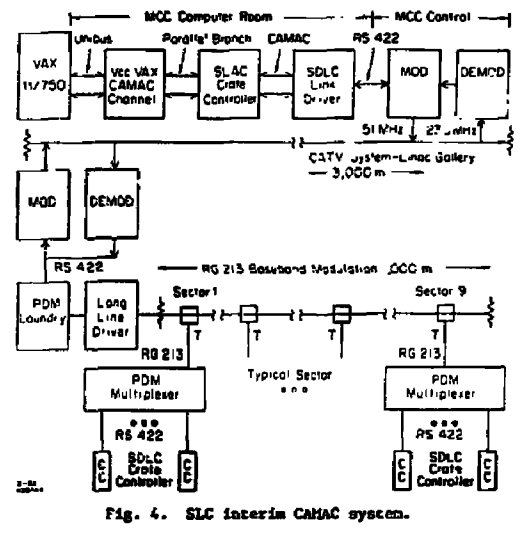

Fig. 4. SLC interim CAMAC system.

Pattern Distribution System

Operation of the SLC requires that all thirty sectors of the linear accelerator, each sector containing eight klystrons, receive timing information, known as a pattern, before each pulse. Sending a pattern before each pulse allows multiplexed operation of the linac for several experiments with differing energy and repetition rate requirements. Pattern distribution for the SLC is accomplished by two types of CAMAC modules, a CAT (Cable Access Transmitter) and a CAR (Cable Access Receiver). As configured for use in transmitting pattern information (see Fig. 5), the CAT accepts pattern information as a sixteen-bit data word from CAMAC, and transmits it as a SDLC broadcast message at a 2 Mbaud data rate by means of an RF transmitter attached to the SLCNET Cable.

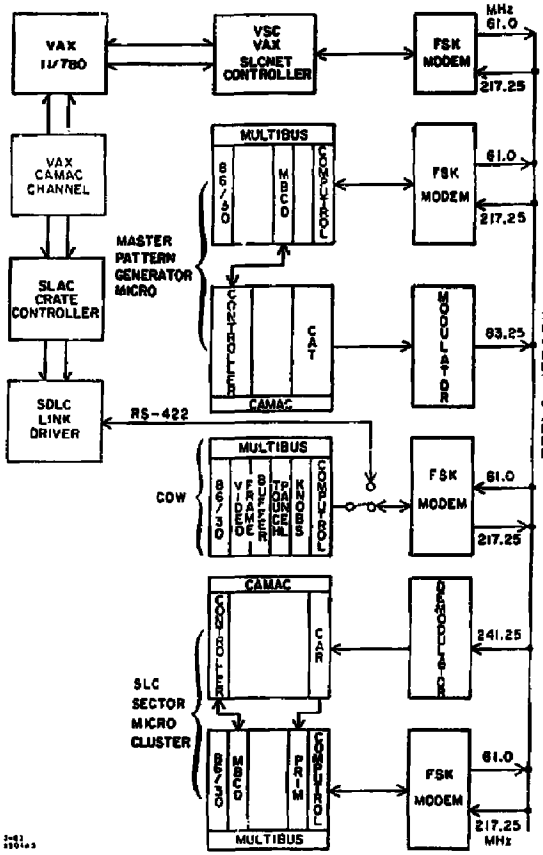

Fig. 5. SLC pattern system.

In each sector an RF receiver demodulates the serial bit stream, and the CAR makes the sixteen bits of pattern information directly available to the sector microcomputer by means of parallel data interface to the PRIM (Pattern Receiver Interrupt Module).

Of primary importance is the ability of the sector micros to be alerted to the fact that errors have occured during transmission or reception of the pattern by means of the CRC. Through the use of the SSA, the CAT, under appropriate software control, may initialize or interrupt individual sector micros. Use of these modules is envisioned for data transmission in fast feedback control loops and point-to-point communications within the SLC. Provisions have been made in the CAT to allow loading of transmit data through a parallel bus on the front panel, reducing the overhead associated with CAMAC operations. As a complementary module, the CAR makes receive data available to CAMAC.

SLC Console on Wheels

The COW, or Console on Wheels, is a portable single-board computer based operation and control station for the SLC. It consists of a color graphics monitor, a monochrome graphics monitor with touch panel, programmable shaft encoders, and various annunciacors. Information for the graphics displays and annuciators must be transmitted to the host computer, and operations requests must be received from the COW by the central computer. A commercially available board[6] with suitable modifications for our physical data link is used to communicate SDLC formatted messages at 1 Mbaud to and from the COW's local memory. Prototype development was done over an RS-422 interface to an SDLC Link Driver, and subsequent integration into the SLCNET network has been accomplished, with the physical data link being FSK modems on the SLCNET Cable. The primary benefit obtained has been the ability to achieve the high speed communications necessary for display of graphics information at several independent stations, concurrent with the accelerated development and integration time made possible by using existing hardware and commercially available equipment.

Conclusions

An evident feature of these networks is their flexibility. A mixture of SLAC designed and commercial hardware has been interconnected to produce intercomputer communications and distributed CAMAC I/O functions. The SDLC protocol supports this sort of ad hoc network, and allows the rapid implementation of useful systems that are configured from a few standardized modules and system components.

Acknowledgments

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References

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