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Radiation effects in semiconductors : Technologies for hardened integrated circuits.

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Abstract.

Various technologies are used to manufacture integrated circuits for electronic systems. But for specific applications, including those with radiation environment, it is necessary to choose an appropriate technology or to improve a specific one in order to reach a definite hardening level.
The aim of this paper is to present the main effects induced by radiation(neutrons and gamma rays) into the basic semiconductor devices, to explain some physical degradation mechanisms and to propose solutions for hardened integrated circuit fabrication.
The analysis involves essentially the monolithic structure of the integrated circuits and the isolation technology of active elements.
In conclusion, the advantages of EPIC and SOS technologies are described and the potentialities of new technologies (GaAs and SOI) are presented.

1. Introduction.

Integrated circuits are widely used in the design of logic and memory functions of electronic systems. They are particularly well adapted to solve miniaturization and low power comsumption problems. For specific military, space and even civil (nuclear industrial field) applications, their use is conditionned by their ability to work under high level radiation environment.
Degradations are induced by this environment into materials and components and are dependent on incident radiation type, semiconductor characteristics and time.
The nuclear environment taken into account here involves essentially:

- a neutron burst with fission and fusion neutrons
- an ionizing X and gamma radiation pulse, the energy of which is about 1 MeV.

Available technologies to manufacture integrated circuits are divided in two families: The bipolar family, where the junction transistor is the basic element and the unipolar family with the MOS transistor (Metal-Oxide-Semiconductor).
After having described the main radiation effects induced in these two types of components, their influence upon the integrated circuits of various technologies will be analysed and actions to improve their behaviour under radiation will be discussed.

2. Interactions and damages in semiconductors.

Radiation effects are generally divided in two classes taking into account the energy deposition process inside the matter; energy can be transferred either to electrons (ionization) or to nucleus (atomic displacements). Ionization is the process of removing electrons from their parent atoms and thereby positive ions and free or unbound electrons are created. Free electrons can be due to charged particles (electrons, protons, recoil atoms...) and to photons, directly or not according to three types of interactions: photoelectric and compton effects and pair production. The figure 1 shows the relative importance of the three types of photon interactions in function of absorbing material and photon energy.

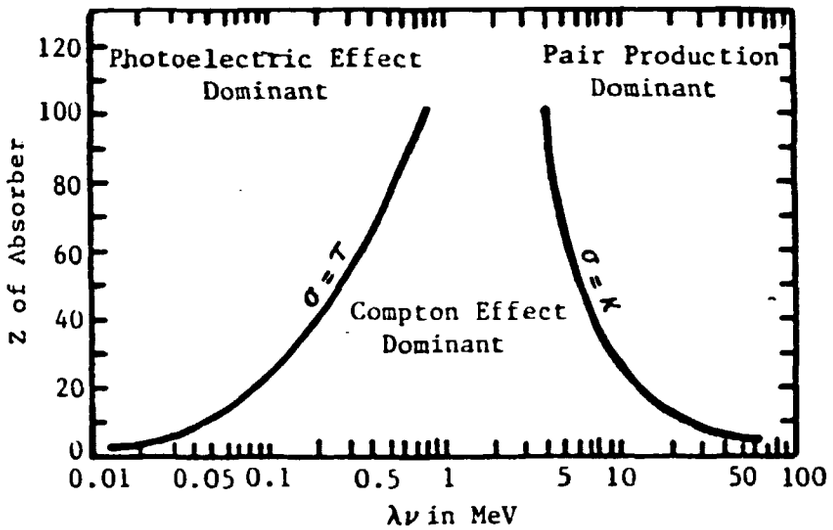


Fig. 1

Displacement effects are due to the interaction of charged particles or neutrons with the nucleus. Recoil atom so created possesses enough energy to collide with other lattice atoms and to induce others displacements in cascade during its slowing down.

Electronic disturbances lead to macroscopic effects the more important of which are:

- the build up of a positive charge in the oxides and specially in the SiO_2 layers
- the creation, during ionization, of positive and negative charge carriers into semiconductor which can move by diffusion or conduction to induce photocurrents.

Atomic perturbations (density and spatial distribution of displaced atoms depend upon incident particle type and energy) give rise to common defects (vacancies and interstitials), unstable and chemically reactive. The final stable state of semiconductor is characterized by the existence of donor and acceptor levels into the forbidden gap. This modified state has consequences on fondamental parameters of active elements.

In qualitative terms, the degradations of the semiconductor components are proportionnal to the radiation absorbed dose in Gy(Si) or to the radiation fluence in particles/cm^2 and lead to permanent dammage. The defects and the associated perturbations are defined as transient or remanent when the radiation is time-dependentand that the induced effects end up with the cause or more slowly than the cause.

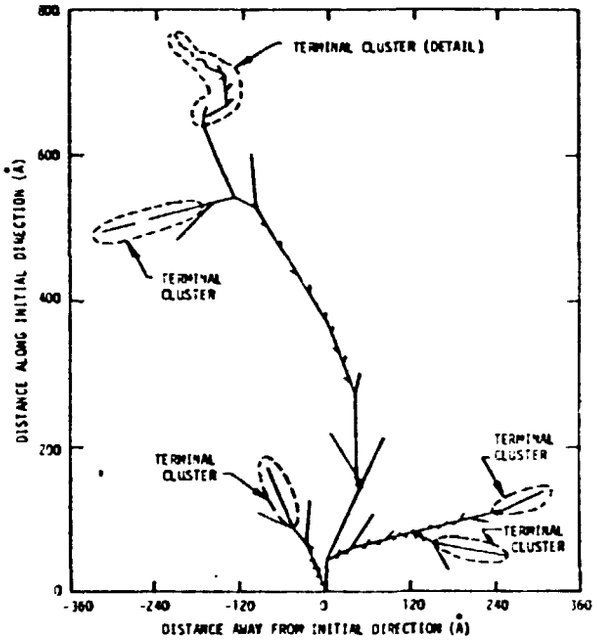


Fig. 2 Defect generation Picture of typical recoil-atom track, with primary energy of 50 KeV.

after V.A.Van Lint and R.E.Leadon.

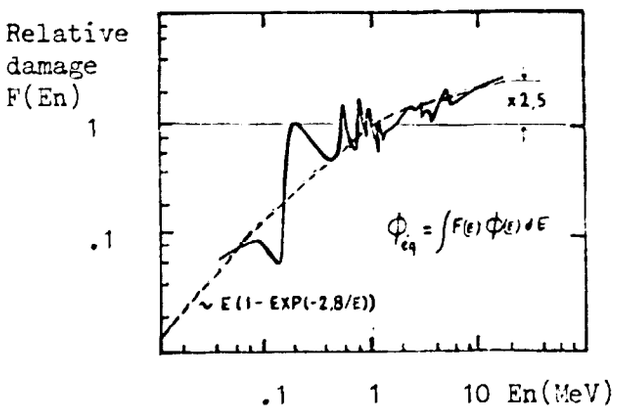


Fig. 3 Damage function (Silicon)

after E.C.Smith and J.Sauret.

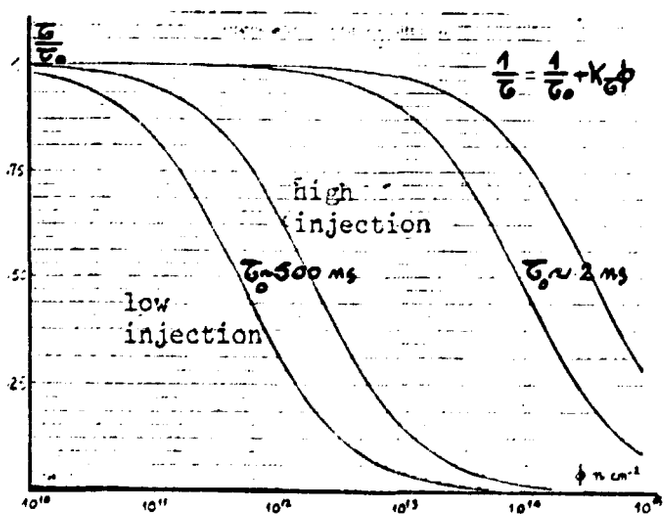


Fig. 4

Typical relative variations of lifetimes τ

3. Neutron effects.

Neutrons are characterized by their energy spectrum (> 10 KeV) and their fluence measured in n/cm^2.

The relation is not direct between the initial phenomenon, the neutron-semiconductor material (Si) interaction, and the final consequence, the modification of the component electrical performance; several steps have to be considered.

3.1. Displacement damage. [1-4]

The displacement of a silicon atom from its lattice position requires about 15 eV. An incident neutron with a sufficent energy arriving inside the lattice can displace one atom, delivering to it a part of its energy in an elastic collision. This displaced atom (recoil atom) and incident neutron can displace again other atoms if their energies are still sufficent.

The effects of displaced atoms in a silicon lattice are due to the creation of simple defects and defect clusters (figure 2). The number of defects created by the recoil atom and the dimensions of the clusters depends on the neutron energy (about 1000 displacements for one 1 MeV neutron).

It is interesting to note that the dimensions of a cluster is comparable to the dimensions of an integrated circuit basic transistor ($\sim$ 1 micron for one 14 MeV neutron).

The damage function into the silicon versus the neutron energy is displayed infigure 3. One can see that the displacement effects become significant for En = 100 KeV and for En = 14 MeV they are about three times more important than for En = 1 MeV. Usually, the neutron fluence is expressed in equivalent 1 MeV fluence via the damage function (silicon).

3.2. Electronic induced effects.

The defects created by atom displacements act as carrier recombination centers and therefore modify the silicon properties.

Minority carrier lifetime.
The relation between neutron fluence and minority carrier lifetime is:

$$\Delta\left(\frac{1}{\tau}\right) = \frac{1}{\tau_\Phi} - \frac{1}{\tau_0} = K_\tau \Phi$$

τ is the preirradiated lifetime
τ_0 is the postirradiated lifetime
K_τ is the lifetime damage constant (in $cm^2 s^{-1} n^{-1}$)
Φ is the neutron fluence

K is dependent on the type and impurity content of the semiconductor, injection level, neutron spectrum ... (figure 4).
An average value of K for silicon is about $K \simeq 10^{-6} cm^2 s^{-1} n^{-1}$.

Majority carrier density.
Defects result in the introduction of allowed energy states within the forbidden gap of silicon, reducing the number of carriers in the conduction band.

The variations of majority carrier concentrations in silicon canbe written empirically according to Buelher [5]

$$N = No\ e^{-\frac{\Phi}{444\ No}^{0.77}}$$

$$P = Po\ e^{-\frac{\Phi}{387\ Po}^{0.77}}$$

Majority carrier mobility.
The semiconductor mobility is determined by collisions of carriers with vibrating lattice atoms and long range coulomb collisions with ionized donor and acceptor atoms. In increasing the number of donor and acceptor defects, the number of collisions is therefore increased and the mobility decreases following the relation

$$\Delta\left(\frac{1}{\mu}\right) = \frac{1}{\mu_\Phi} - \frac{1}{\mu_0} = K_\mu \Phi$$

$$K_\mu = 10^{-19} V^{-1} s\ n^{-1}.$$

3.3. Neutron effects on bipolar transistors.

All of the above effects may be important, but the one that is often of most concern in bipolar transistors is the decrease of the current gain produced by the reduction in minority lifetime. An order of magnitude decrease in current gain, say from 100 to 10, may be observed in transistors that have been exposed to a neutron fluence of 10^{14} n/cm^2.

The reciprocal of transistor gain (h_{FE}) is a function of neutron fluence as:

$$\Delta\left(\frac{1}{h_{FE}}\right) = \frac{1}{h_{FE\Phi}} - \frac{1}{h_{FEO}} = t_b\ K'\ \Phi$$

where h_{FEO} is the preirradiated gain
$h_{FE\Phi}$ is the postirradiated gain
t_b, is the base transit time
K', is the gain damage constant
Φ is the neutron fluence

Note that the base transit time is inversely proportionnal to the gain bandwith product F_T and hence $\Delta\ (1/h_{FE}) = K''\ \Phi\ /\ F_T$.
It is also possible to place the emitter current into this relation in order to show that the gain degradation is a function of the injection level.

$$\Delta\ (1/h_{FE}) = K'''\ \Phi\ /\ F_T . I_E^{0.3}$$

The increase of the collector resistivity ($\rho \propto 1/N\mu$) causes the breakdown voltage and VCE(SAT) to increase.
The breakdown voltage increase is here an improvement over the pre-irradiation value. The corresponding increase in VCE(SAT), however, is undesirable since VCE(SAT) is an important parameter in logic and amplifier circuitry.

In conclusion, transistors with good resistance to neutron fluence will have very thin bases and shallow emitters, with high F_T. It will be necessary to minimize the collector resistivity and to adjust the base doping.

3.4. Neutron effects on MOS transistors.

MOS transistors, wether N-orP-channel are majority carrier devices and for that, not susceptible to neutron irradiation below 10^{15} n/cm^2. Ionizing effects associated to neutrons at high level fluence, will be taken into account with the ionizing total dose.

4. Photon effects.

Photons as neutrons are indirectly ionizing; but in account of the pulsed character of photon radiation considered, the transient and remanent effects are more varied.

For high energy photons (= 1 MeV) Compton effect is directing; it can generate a rather oriented electron current (Compton current) at which is associated an electromagnetic field. This one is able to induce particular disturbances in the component behaviour.

For lower energy photons (1 KeV - 200 KeV) photoelectric effect is predominant. It gives rise to important charge variations at the interfaces.

The generation of a positron-electron pair becomes predominant when the photon energy is of several MeV.

Under gamma or X rays (and neutrons above 1 MeV) , free carriers generated can -undergo random motion
-diffuse to regions of lower carrier concentration
-drift with applied electric field
-be trapped at impurity atom sites
-recombine with their mates.

4.1. Total dose effects.

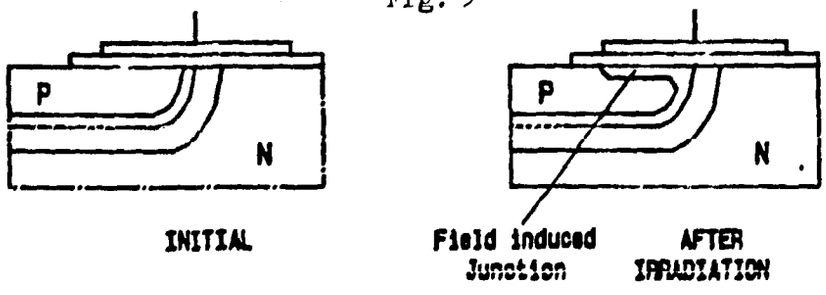
The main effects due to ionizing total dose are the buildup of positive charges in the oxide layer, an increase of electronic states at the interface Si-SiO_2 and the creation of electron traps into the oxide.

4.1.1. Bipolar transistors.

For diodes and transistors, positive charges induced into the protection oxide can invert the doping of the underlying silicon layer, giving rise to leakage currents between the two parts of the junction or into the base of a transistor. This last effect reduces the transistor gain. (figure 5)

But now, with good oxides, those effects are minimized so that no influence is seen below doses equivalent to 10^4 Gy(Si). It is not the same thing with MOS technologies.[7]

Fig. 5



4.1.2. MOS transistors.

Charge buildup into the gate oxide is the principal reason of the sensitivity of MOS transistors to an ionizing radiation. Under radiation, free electrons and holes are created into the oxide which move with the applied voltages. Electrons are mobile and can usually be swept out of the SiO_2 while the holes, less mobile, are trapped in the gate insulator. The result is a net positive space charge which induces negative charges in the underlying silicon which modify the electronic characteristics of the semiconductor in the channel region. [6]

The basic electrical parameter that measures this effect is the threshold voltage (V_T).

In addition to the trapped charges, electronic states may be created at the silicon-oxide interface. In p-type silicon (N-channel transistor) , the interface states are charged neutral or negative; they can compensate the positive chargein the insulator. In N-type silicon (P-channel transistor) the interface states are neutral or positive; they tendto add to the positive oxide charge.

The contribution of these radiation effects can be introduced into the expression of the transistor threshold voltage which is before radiation

$$V_T = - \frac{Q_{ox} + Q_{ss}}{C_{ox}} + \Phi_{MS}$$

where Q_{ox} is the oxide charge
Q_{ss} is the interface state charge
C_{ox} is the gate capacitance
Φ_{MS} is the silicon-metal work function

and which becomes after radiation

$$V_T = - \frac{(Q_{ox} + Q_{rsc}) + (Q_{ss} + Q_{rss})}{C_{ox}} + \Phi_{MS}$$

where Q_{rsc} is the radiation induced positive charge

Q_{rss} is the radiation induced interface state charge

The figure 6shows the shifts of the transfer curves (I_D-V_G) for N-andP-transistors. It can be seen that an enhancement N-channel transistor with $V_{TN} > 0$, can become "ON" at $V_G = 0$ and work in the depletion mode. At the contrary, the P-channel becomes more "OFF". For N-channel transistor, the contribution of the interface states shows that the transfer curve can come back toward its initial position.

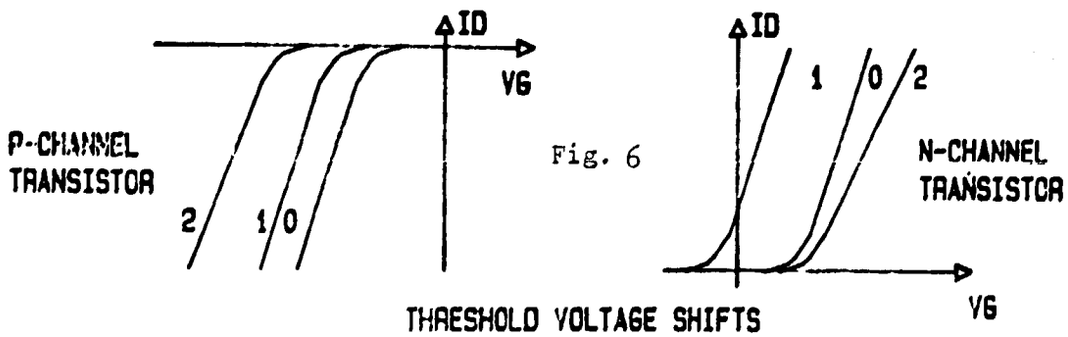


Fig. 6

An other effect produced by the interface states is the decrease of the carrier mobility which is depicted by a decrease of the transfer curve slope.

As in bipolar transistors, leakage currents can be induced at the interfaces and into the field oxides.

At the technology level, the fabrication of MOS transistors with a good resistance under radiation is bound to the oxidation process and post-oxidation annealing treatment. Many studies have been carried out on: dry oxygen SiO_2, wet oxygen grown SiO_2, steam grown SiO_2, anodically grown SiO_2, deposited SiO_2 glasses and silicon-nitrogen compound (Si_3N_4)...Each manufacturer has his own process but the experiments concerning the relation of structure, processing and radiation effects have shown that the very clean oxides with regard to certain contaminants and having, as result low initial interface states and oxide charges are the best under radiation.

The reduction of the gate oxide thickness also will improve the radiation resistance.

It is to note that the deposit method of aluminium is important in the hardening process. Electron beam deposition can irradiate a MOS structure up to 1.10^4 Gy(Si) and create defects which are annealed during the post-oxidation thermal process but which become again quickly apparent during a further irradiation. RF heating or crucible deposition methods will be preferred.

4.2. Dose rate effects.

The main effects induced by an ionizing radiation pulse are well described from the behaviour of irradiated reverse biased PN junction.

The figure 7 shows a cross section of a PN junctionsubmitted to a radiation pulse. Electrons and holes are generated homogeneously into the semiconductor.

Under influence of high electric field in the depletion zone and of the diffusion process, associated to the high concentration variations (doping profiles) near the junction, the charges are separated and flow across the junction, giving rise to a photocurrent. [8]

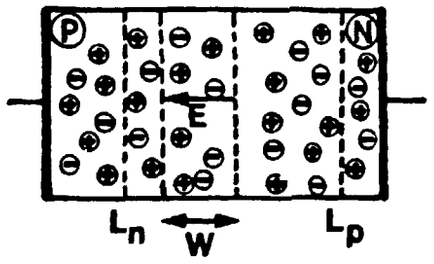


Fig.7

This photocurrent I_p is described by the relation

$$I_p(t) = q.g_o.V_c.\dot{D}(t)$$

where $q = 1.6\ 10^{-19}$ C

$g_o = 4.10^{15}$ carriers / cm^3. Gy(Si)

g_o is the carrier generation rate conversion factor

$\dot{D}$ is the dose rate in Gy(Si)/s.

V_c is the effective collection volume from which excess carriers can drift or diffuse to the junction before recombining.

To simplify, $V_c = A (W + L_P + L_N)$ where A is the junction area, W the depletion region width and L_P and L_N the diffusion lengths in the N and P regions.

This expression of the photocurrent, $I_P = q g_o V_c \dot{D} (t)$, is ever used to calculate the photocurrents of more complex structures.

In the case of bipolar transistors, primary photocurrents are generated within the depletion regions of the collector and emitter as well as within a few diffusion lengths of the junction in the base-emitter and the base-collector regions. Since the base-collector region is the largest in volume and backbiased, most of the primary photocurrent originates into the collector.

The photocurrent response of a transistor depends upon its application. The simple case to consider is the open base grounded emitter NPN transistor with a positive voltage to the collector. The primary base collector photocurrent makes the base region more positive and forward biases the emitter-base junction. The primary photocurrent acts as a base current which gives rise to a secondary photocurrent by the way of transistor action and the h_{FE} current gain :

$$I_{SP} = I_{PP} (1 + h_{FE})$$

In integrated circuits all of the active and parasitic junctions are the seat of photocurrents. Their contribution is more difficult to evaluate. (Parasitic junctions are the insulation junction of the integrated circuit monolitic structure).

It would be possible to take into account of conductivity changes induced by radiation in dielectrics and insulators; but with a few exceptions (as it will be seen farther with SOS) their effects remain weak compared to junction photocurrents.

In conclusion, the design of components with good resistance to the dose rate ionizing radiation involves:

- the reduction of dimensions of elementary diodes and transistors
- the reduction of carrier lifetimes into base and collector regions (gold doping)
- the use of appropriated isolation techniques of active elements in integrated circuits.

5. Vulnerability of integrated circuit technologies.

Among bipolar technologies, TTL (Transistor Transistor Logic) is the most widely used. Various series allow to choose circuits in function of speed or power consumption. Improvements are constantly brought to maintain them in the competition (Advanced Shottky TTL).

ECL (Emitter Coupled Logic) is the fastest technology but its high power consumption limits its use in embarked systems.

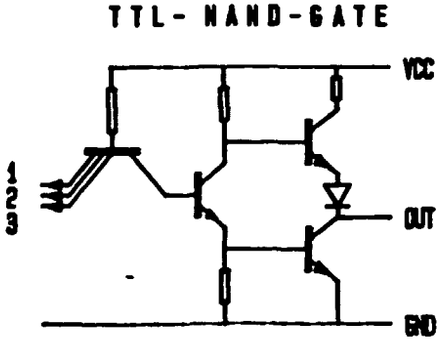
Last born one of bipolar logic, I^2L (Integrated Injection Logic) is full of promises : high integration density and very low power consumption.

In MOS structures, two great technologies are sharing the market of logic and memory circuits : N-MOS and C-MOS. Their evolution trends to the dimension reduction as well as in the channel length as the oxide thickness (VLSI or VHSIC).

All of these technologies have made the object of many vulnerability studies under radiation. It is not the purpose of this paper to give exhaustive results that it will be possible to find from other sources.
But the TTL and C-MOS technologies are sufficiently representative of the two integrated circuit technologies to serve as examples in order to explain their behaviour under radiation and to suggest the possible improvements which can be made.

5.1. T T L .

The TTL basic structure is a three input NAND gate utilizing NPN transistors one diode and diffused resistors. (figure 8)



5.1.1. Neutron effects.

Neutrons reduce the transistor current gains and increase the transistor VCE(SAT). These effects lead to a reduction of the output current.
The figure 9 displays the output current versus output voltage of a lot of NAND gates for two neutron fluences.

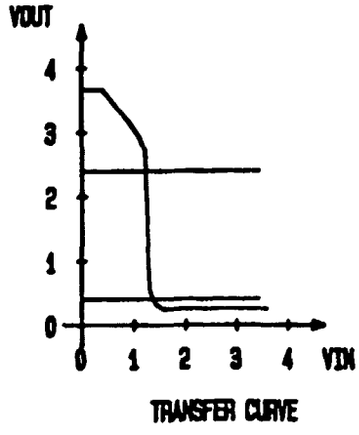


Fig. 8

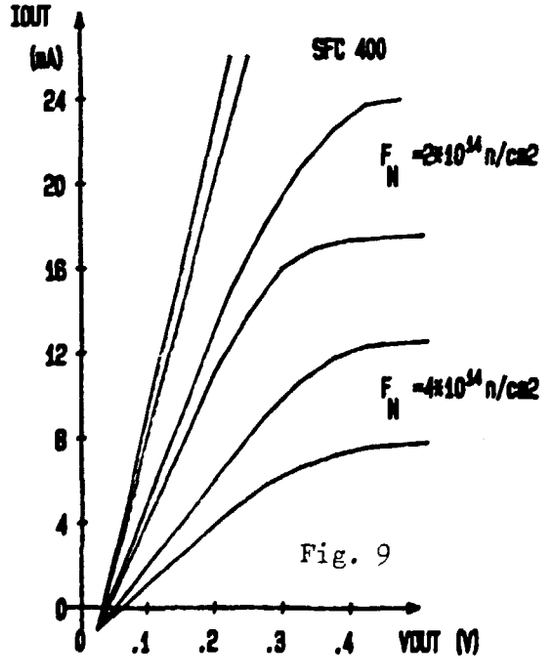


Fig. 9

The vulnerability threshold depends upon the TTL series (Low power , Normal, Schottky ...). It is between 5.10^{13} and 5.10^{14} n/cm^2.

5.1.2. Ionizing dose effects.
TTL is not strongly affected by total dose. If the protection layer is of good quality, the electric performance characteristics only begin to change after 1.10^2 Gy(Si).

5.1.3. Ionizing dose rate effects.

At the contrary, ionizing dose rates induce electric parasites into logic circuits the amplitude of which are susceptible to modify the logic states.

The radiation induced mechanisms are complex and merit analysis.

Standard bipolar integrated circuits are diffused in N-type epitaxial silicon layer. Active elements, transistors and diodes are insulated between them by reverse biased PN junctions obtained by diffusion of P regions into the N epi-layer.

Resistors also are diffused and junction insulated.

So, to each NPN transistor is associated a parasitic PNP transistor and each resistor is shunted by a distributed junction. (figure 10)

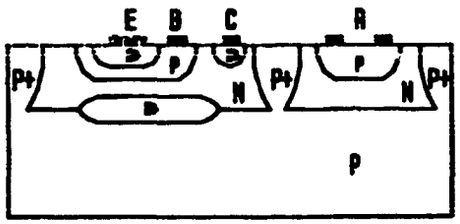


Fig. 10

Under a radiation pulse, photocurrents are generated into all junctions and transistors. But due to the larger area of insulating junctions, their photocurrents are more important and contribute to a relatively modest vulnerability threshold (logic upset) : 2.10^6 to 2.10^7 Gy(Si)/s.

At high dose rate levels, these photocurrents are susceptible to burn-out the junctions and the metallizations.

An other mechanism can be induced into the IC structure and cause catastrophic failure. Known as Latch up, it takes place into four layer structures (NPNP or PNPN) where photocurrents and applied voltages can give rise to thyristor effects, inducing anomalous logic states and extra sustained supply currents.

This effect is difficult to get in TTL but it exists and depends on the integrated circuit design.

In order to become to latch up free, a solution leads to use a dielectric isolation technique of active elements.

The basic technology process (EPIC) Epitaxial Process for Integrated Circuits, is more complex than classical process. It consists to isolate small monocrystalline silicon moats into a polycrystalline silicon layer by silicon oxide layers. The poly-silicon layer (300 µm thick) is used as a mechanical support. Active elements and resistors are diffused into the monocrystalline regions. (figure 11)

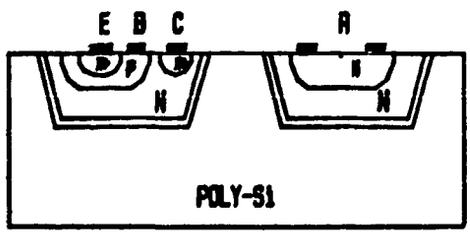


Fig. 11

Other techniques can be associated to the dielectric isolation in order to improve the behaviour of TTL under transient radiation :

- the substitution of diffused resistors by vacuum deposited resistors (NiCr, SiCr,...)

- gold doping, to decrease the base and collector minority carrier lifetimes

- the integration of small geometry transistors with high F_T .

The use of these techniques has allowed to improve the transient vulnerability threshold by at least two orders of magnitude (2.10^8 Gy(Si)/s) and to eliminate the latch up phenomenon. Other improvements can be available with an optimization of the circuit design.

These technologies have been implemented by many manufacturers particularly by Harris, Texas, Motorola, RCA in USA, Toshiba in JAPAN and Thomson in FRANCE.

In an other field, they are really suited to manufacture high voltage or linear circuits with complementary bipolar transistors.(figure 12)

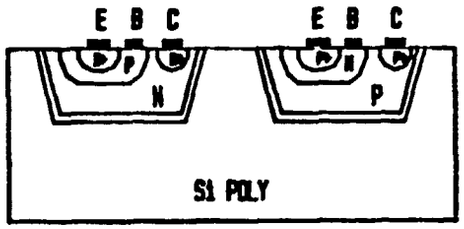


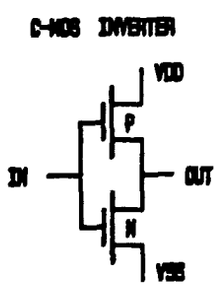
Fig. 12

Remark. This dielectric isolation technique would be advantageously used for I^2L structures. It could improve the PNP lateral transistor which is the weak point of I^2L under neutrons.

5.2. C - MOS.

The basic C-MOS cell is an inverter including two complementary transistors, N-and P-channel, both working in the enhancement mode. [10]

The inverter transfer curve and supply current observation shows the power consumption only is effective during the transition. (figure 13)



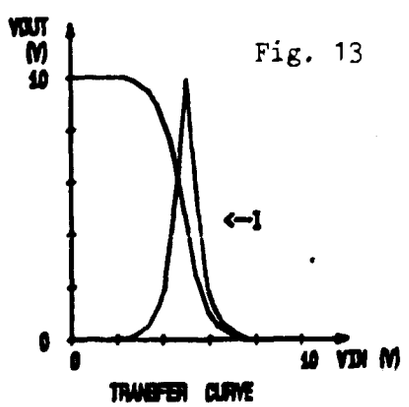


Fig. 13

This structure is very well adapted to high integration density.

5.2.1. Neutron effects.

Because the MOS transistors are majority carrier devices, C-MOS are not too much affected by neutrons. Induced ionizing effects have to be taken into account with ionizing total dose.

5.2.2. Ionizing total dose effects.

The predominant effect of ionizing radiation is the threshold voltage shifts of the both N- and P- channel transistors. As a result, the transfer curve is shifted towards the left. [11]

In addition, surface effects are induced into the field oxides giving rise to leakage currents into parasitic MOS transistors which can disturb the circuit behaviour.

The vulnerability level is strongly dependent on fabrication conditions and circuit type. It will be determined by the maximum variations of the tolerable threshold voltage shifts. So, the total dose limit for commercial microprocessor is not more than 100 Gy(Si); but for simpler logic circuits it can be about 1000 Gy(Si).

In using appropriate processes to manufacture ultra clean gate and field oxides, it is possible to improve the radiation tolerant level up to 10^4 Gy(Si). (example: Rad-hard CD 4000 series with Z suffix.RCA)

5.2.3. Ionizing dose rate effects.

As into the classical bipolar monolithic structure, photocurrents are generated in all of the junctions. The first radiation investigations connected with C-MOS inverter have been carried out by A.G. Holmes-Siedle and al. in 1967 but theyare always of actuality. [12]

Three photocurrents have to be considered as shown in the figure 14
I_W is the photocurrent generated into the P-well junction, where is diffused the N-channel transistor. This one can be important at high radiation rates but flows from supply to ground increasing by this way the supply current.
The two other photocurrents to take into account are I_P and I_N created into the drain junctions of P-and N-channel transistors.

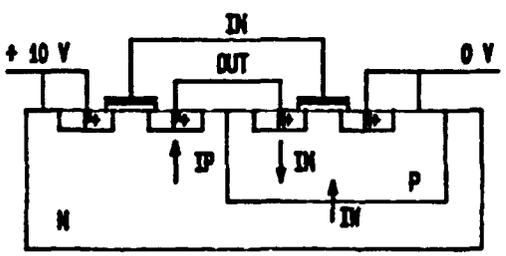


Fig. 14

They give rise to an induced voltage at the inverter output :

$$|\Delta V| = R_{P(N)} \cdot |I_P - I_N|$$

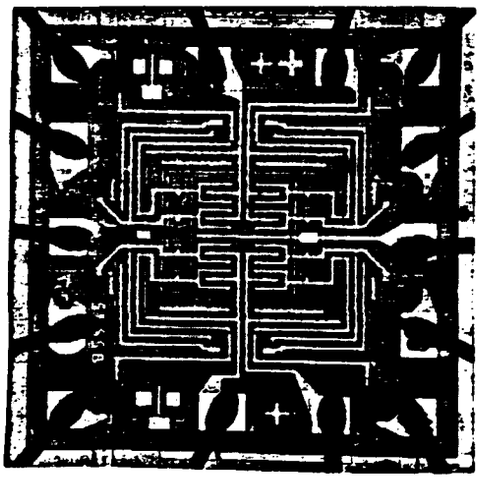
where $R_{P(N)}$ is the ON resistance of the transistor in conduction state.
This equation shows a certain photocurrent compensation due to the complementarity of the transistors.

The small transistor dimensions and this compensation effect would have induced a high dose rate tolerant level. But the radiation analysis have shown that this level was much lower ($\simeq 1.10^6$ Gy(Si)/s) than this one obtained by the contribution of known photocurrents.

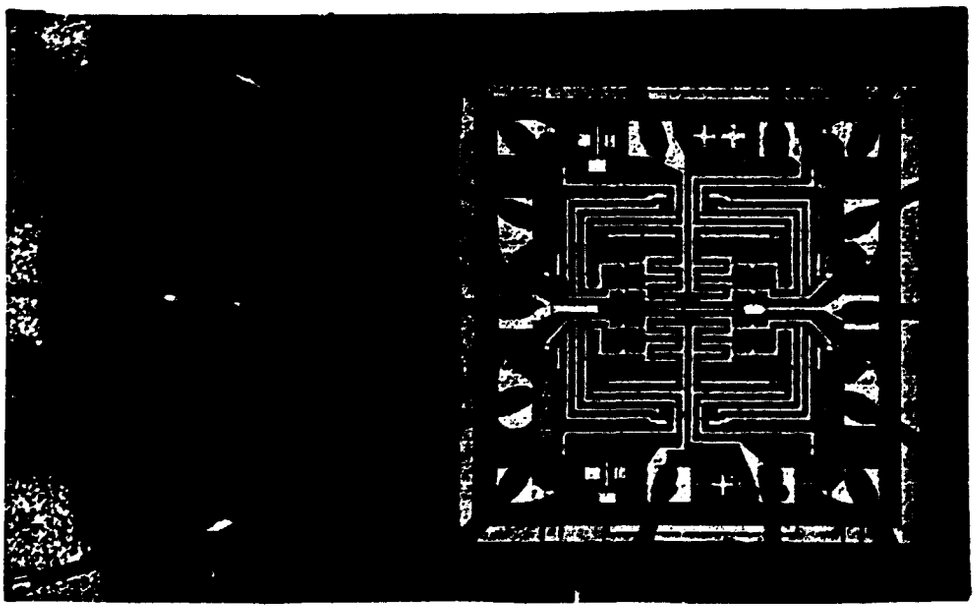
The reason is similar to this one found with the bipolar structure. Latch up takes place in four layer structures giving rise to anomalous photocurrents. Here the effects are more important and can be easily demonstrated. They can lead to burn-out junctions, metallizations and bonding wires (photo)
Many radiation studies and experiments have been implemented . [13]

LATCH-UP INDUCED EFFECTS

Metallization burning-out



Bonding wire burning-out



6. Latch-up free C-MOS technologies.

6.1. Isolation technology.

According to the foregoing, the transient radiation failures are the result of the active element insulation mode into the integrated circuit monolithic structure.

It would be possible to manufacture C-MOS transistors in using dielectric isolation as for TTL. Harris used this technique for CD 4000 series in '73, but it was not suited to high integration level.

Other techniques have been developped which consist on local oxide isolation as is shown in the figure 16

Various names are given to those one: Isoplanar, ISO-CMOS, LOC MOS ... They are the subject of transient radiation investigations. But it is difficult and even impossible to obtain a final proof to a 100 % certainty level to have free latch-up circuits.

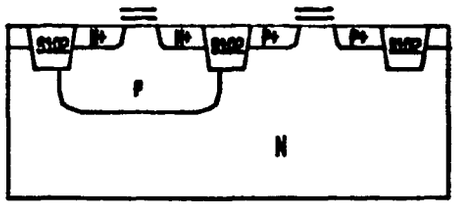


Fig. 16

6.2 Al-gate C-MOS/SOS technology.

The Silicon On Sapphire (SOS) technology allows the total insulation of active elements without semiconductor junctions. It leads to improve the circuit speed in reducing the parasitic capacitances, to increase the integration density and to increase the transient radiation level.
The SOS technology main point lies in the use of monocrystalline alumina substrate (≈ 300 µm thick) with an oriented plane ($1\bar{1}02$) on the top of which a thin silicon layer (0.6 µm) has been epitaxied with (100) orientation.

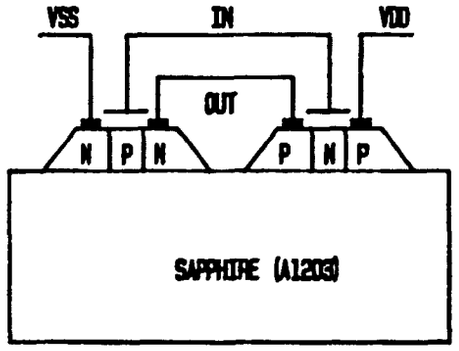


Fig. 17

The first steps of the processing consists of the creation of silicon islands where the transistors are diffused or implanted. The gate oxide is generally thermally grown and aluminium is vapor deposited upon the oxide.

The figure 17 shows the C-MOS/SOS inverter structure.

This technology has been implemented by RCA, Rockwell, Hewlett-Packard and Hughes in USA, by Siemens in Germany and by Thomson-Efcis in France.

6.2.1. C-MOS/SOS radiation vulnerability.

6.2.1.1. Ionizing total dose effects.

To the creation of positive charge into the gate oxide and of the electronic states at the Si-SiO_2 interface, it is necessary to add the same effects created into the sapphire substrate and at the silicon-sapphire interface.

The two first effects give rise to threshold voltage shifts leading to the shift of transfer curve. In addition, leakage currents appear. They are due to the presence of parasitic lateral transistors onto the edges of silicon islands. (figure 18)

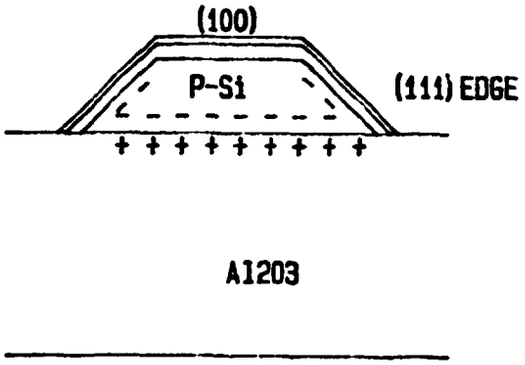


Fig. 18

The radiation positive charge created into the sapphire substrate can induce an electron inversion layer in the silicon near the silicon-sapphire interface, connecting source to drain and giving rise to the so called back channel leakage current. [14]

This current is in general independent of the gate voltage and hence cannot be turned off. Some ion implantation processes are performed to decrease this effect and to allow a good ionizing total dose level (1.10^4 Gy(Si))

6.2.1.2. Ionizing dose rate effects.

Transient effects into C-MOS/SOS circuits are the result of the active junction photocurrents and of the induced photocurrents by the sapphire photoconduction.

Intrinsic junction photocurrents are very small, due to the small junction areas. With the considered silicon layer thickness, the photocurrent value is about 3.10^{-15} A/Gy(Si) per micron of length.

But all of the silicon stripes and aluminium interconnexions are biased at various voltages which induce semi-circular electric field lines into the underlying sapphire. Under the influence of these electric fields, the electrons generated during the ionizing pulse are collected and act as photocurrents (figure 19)

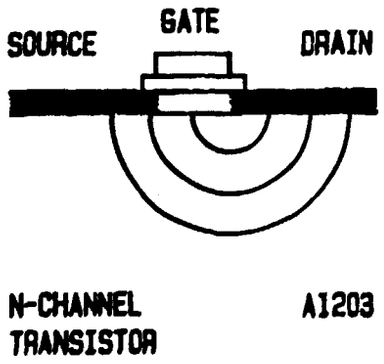


Fig. 19

The involved mechanisms have been described by D.H.Phillips. From this analysis, it results that the sapphire induced photocurrents are 2 to 5 times more important than those issued of the silicon structure. [15]

The logic upset threshold of C-MOS/SOS integrated circuits is found between 5.10^8 and 1.10^9 Gy(Si)/s, showing an improvement of about two orders of magnitude with regard to classical C-MOS circuits; of course, the C-MOS/SOS circuits are latch up free.

6.3. Si-gate C-MOS/SOS technology.

As for all of the MOS technologies, the Si-gate process trends to replace the Al-gate process. That contributes to improve the electric performances and allow the manufacturing of more complex circuits by the way of a dimension reduction (channel length and oxide thickness) inducing a higher integration level (VLSI and VHSIC).

Actually, microprocessor or memory circuits are founded on the market (GPU 001, MWS 5114 ...RCA). Custom and semi-custom integrated circuits become to be available (RCA, HAFO, Marconi ...).

The previous circuits work with the two transistors in the inhancement mode. An other working mode where the N-channel is off when it is deep depleted leads to easier technology (with less masks) which is in processing at Thomson-Efcis and in radiation evaluation at CEA.

Good results already have been obtained under high radiation total dose levels (> 10^7 Gy(Si)). Transient effects are about the same than those found with the Al-gate C-MOS/SOS technology.

7. New trends in radiation tolerant technologies.

7.1. SOI (Silicon On Insulator).

One of the reasons of the want of success of the SOS integrated circuits on the commercial market is the cost of the substrate which requires a lot of preparing work and caracterization. But, the techniques used with SOS to improve the electric properties of silicon (recrystallization by laser annealing or others) have lead to reconsider the substrate problem.

SOI technology consists of growing silicon layers, on the top of silicon oxide layers, which will be recrystallized by various appropriate methods (laser annealing, liquid and/or phase epitaxy, strip heater ...). Those latter are still at the research level and have to demonstrate their ability to be industrial. It is too soon to give an opinion on SOI technology but the whole of the technology processes involved, notably to manufacture 3 D devices, require our attention.

As regards to the under radiation vulnerability of this technology, it is also to soon to pronounce one's opinion.

Many insulating layers and many interfaces will be the seat of well known ionizing effects. But, the hardening techniques used with the SOS technology, which is a particular case of SOI technology will can be implemented without difficulty.

7.2. MNOS. Metal Nitride Oxide Semiconductor.

Generally, the hardening levels of memory devices are low . N-MOS dynamic memories are disturbed after 10 Gy(Si) of ionizing radiation and their logic level at 10^6 Gy(Si)/s.

C-MOS and C-MOS/SOS static memories are better : 10^2 - 10^4 Gy(Si). for prolonged ionization radiation and 2.10^8 Gy(Si)/s for the logic upset (CMOS/SOS).

For specific applications it would be interesting to have a "harder" memory component.

The MNOS, which is a metal-insulator-semiconductor transistor with two insulators (SiO_2 layer = 30 Å thick and Si_3N_4 layer = 500 Å thick) is a non-volatile device. Integral part of a memory cell, this transistor can keep its information up to a memory upset of 10^{10} Gy(Si)/s.

The MNOS technology is compatible with other MOS technologies. Associated to SOS Technology this one would constitute the best radiation tolerant device for Integrated Circuits.

Actually, many manufacturers are involved with C-MOS, M-NOS/SOS technology : Rockwell, Westinghouse [16]. Sandia [17] develops hardened MNOS memory devices associated to a bulk C-MOS technology. Plessey and Phillips have also devices on the commercial market.

7.3. GaAs (Gallium Arsenide).

In the field of the electronic technologies for the future, Gallium Arsenide (GaAs) is well placed.

Already, GaAs field effect transistors have demonstrated their ability to work into power and frequency ranges not accessible to silicon.

As for integrated circuits, GaAs technology is at the beginning of its development and many research laboratories are working on the subject.

In a near future, it would be very interesting to concept electronic systems associating GaAs components such as optoelectronic devices, GaAs linear and digital integrated circuits and GaAs power components.

Ga As Integrated circuits are still under development ; the information concerning radiation effects on GaAs is less voluminous than for the silicon.

However, some characteristics of the technology and the first investigations made on material and devices tend to demonstrate that it is well adapted to manufacture radiation tolerant integrated circuits :
First point, the semi-insulating nature of gallium arsenide constitutes a good material characteristic for a substrate to avoid latch up
Second point, the use of GaAs field effect transistors with PN-junction or schottky barrier gate structure which are not too much susceptible to total dose of ionizing radiation.

Under radiation, GaAs material and devices undergo the same degradation types than the silicon case.

Displacement damages take place into the crystal lattice where are found the two defects : creation of vacancy interstitial pairs damaged regions which are different of those created in silicon (spike zones of quasi-metallic behaviour insteed of defect clusters in silicon. They induce similar effects on carrier lifetimes, carrier removal and mobility degradation. But, due to the fact of carrier lifetimes are very short in GaAs the degradations are relatively less important compared to silicon.

The basic element of GaAs integrated circuits is the MESFET (Metal Semiconductor Field Effect Transistor). There is no active oxide into the structure so that under ionizing radiation the behaviour of GaAs is comparable to the bipolar technology.

R. ZULEEG and K. LEHOVEC [18-19] have shown some results on GaAs JFET where neutron fluence of 1,7 10^{15} n/cm^2 and ionizing total dose of 1.10^6Gy(GaAs) do not have modified strongly the intrinsic characteristics. The same performances are expected for integrated circuits.

Transient effects are also similar to bipolar those one. Photocurrents generated into PN-junction can be approximated by :

$$I_p = q\ g_o\ V_c\ \dot{D} = q\ g_o\ A L_c\ \dot{D}$$

where A is junction area
Lc is an effective collection length
g_o here is the carrier generation constant factor for gallium arsenide. Its value is $6{,}63.10^{15}$ carriers/cm^3.Gy(GaAs). It is 50% larger than that for silicon.

The first results give a dose rate for logic upset in the range of 10^8 to 1.10^9 Gy(GaAs)/s.

Because of the good behaviour under ionizing radiation and the minimum effects of neutrons, GaAs is a fully promising technology for devices and intregrated circuits able to work in severe nuclear environments.

8. Conclusion.

The radiation environment induces in material and devices severe degradations which can be reduced and even eliminated with hardening methods. Those latter are very often improvements of the basic technology. Neutrons and ionizing radiation (total dose) defects are often of most concern in fabrication processes which have to tend to the best quality.

In integrated circuits, the more important defects (latch up) are due to the monolithic structure which in classical technologies consists of a junction isolation of active elements. The dielectric isolation with polycrystalline silicon and the silicon on sapphire.

Technologies have notably improved the behaviour of logic components under radiation pulses.

Actually, the C-MOS/SOS Si-Gate technology is the best one to manufacture complex integrated circuits with a good resistance to the radiation effects.

9. Acknowledgements.

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