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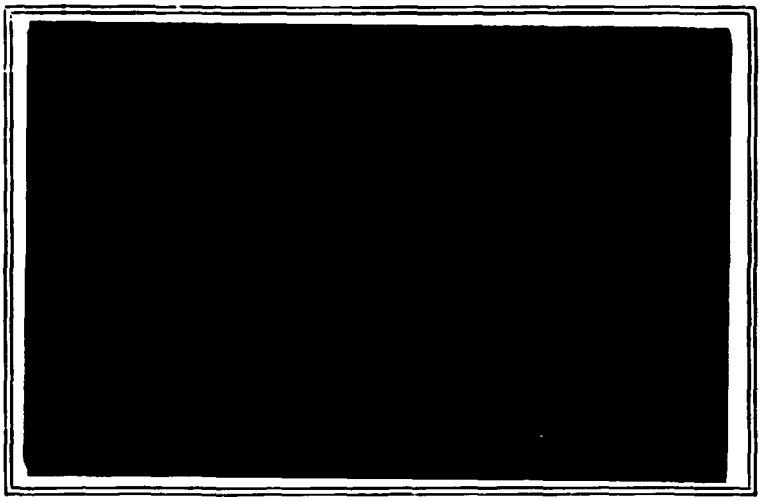

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A high dutycycle low cost multichannel analyzer for electron spectroscopy

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ABSTRACT

A high dutycycle multichannel analyzer has been designed and used in time-of-flight electron spectroscopy. The memory capacity is 64k counts. The number of channels is 8192 with a time resolution of 100 ns. An oscilloscope is used to display the spectra synchronous with the counting. The unit has been built with standard electronic components.

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1. Introduction

Many scientific methods are based on fast signal detection and storage of data which are analyzed with respect to some parameter, like time or voltage, that is varied during the experiment. A necessary or desirable condition may be to handle data of repeated recordings with the same parameter settings. The data storage and handling is usually accomplished by an on-line multichannel analyzer or computer system suitably programmed for the specific experiment. Commercial equipment of this kind is expensive and may furthermore require substancial efforts to become compatible with other parts of the detection system. The present paper describes a simple, inexpensive and effective multichannel analyzer which has been built from standard electronic components. It is designed for a time-of-flight electron spectrometer which combines high resolution with high intensity. The multichannel analyzer has a general performance which makes it useful, with small variations, for various types of experiments.

The present application in time-of-flight electron spectroscopy primarily requires fast handling and processing of large amounts of data. Spectra are obtained by recording the time distribution of electrons emitted simultaneously from a solid target. The time resolution of the multichannel analyzer is 100 ns. The maximum number of counts in a given channel is 64 k. Fig.1 shows schematically the experimental set up with electron spectrometer, multichannel analyzer and display unit. The detailed description of the system and its function is given in the following. In the last sections some preliminary experiments are described and the spectrometer resolution is investigated.

2. Design and function of the multichannel analyzer

2a Block diagram

The block diagram of the multichannel analyzer is shown in Fig. 2. It consists of clock circuits, multiplexer, D/A converter and two identical memories. Each memory has its own address counter, control circuits and arithmetic unit. The number of channels (a channel is defined as a memory cell which stores the total number of counts for a given flight time) of a memory is 4096, which gives a total number of 8192 channels. Each channel stores 64 k counts. The even numbered channels (0,2,4.... 8190) of the multichannel analyzer are located in memory A and the odd numbered channels (1,3,5....8191) in memory B. The memory channels are addressed sequentially by the address counter. During an address cycle the arithmetic unit works in two different modes, a data aquisition mode and an arithmetic mode, and the two arithmetic units A and B are always in opposite modes as will be described below. By the construction involving two memories with associated circuits (address counter, control circuits and arithmetic unit) the deadtime in electron detection when shifting between two adjacent channels is zero. The clock frequency is 5 MHz which gives an address cycle time for a given channel of 200 ns. The data aquisition time of each memory channel is 100 ns.

The address counter is triggered by the clock signal, which also starts the data aquisition of the arithmetic unit. When a channel is addressed, data is read out from the memory to the arithmetic unit. If there is a new count present at the input, after the data aquisition time of 100 ns, it will be added to the previous number of counts in the arithmetic unit. The new number is then written back into the memory. As can be seen in the block diagram memory A is triggered by the positive-going edge of the clock signal while memory B is triggered by the negative-going edge.

A positive-going edge of the clock signal starts the data aquisition of arithmetic unit A and the content of the addressed channel is read out simultaneously. During the second half of the clock period, while data of memory A is processed in the arithmetic unit and written back into the memory, the data aquisition is proceeded in arithmetic unit B. The next positive-going edge of the clock signal starts the data aquisition of arithmetic unit A and shifts the address of memory A while the arithmetic unit B is in the arithmetic mode of operation and so forth. The principle of the overlapping address cycles is shown in Fig.3.

An input capacity of 1 count/channel for each bunch of electrons emitted from the cathode is sufficient in the present application with high time resolution and high repetition frequency. The input capacity can easily be enlarged as will be described below.

The control circuits provide the different control signals to the memories, the arithmetic units and the D/A converter.

The outputs of the memories are fed to the multiplexer which successively selects data from the memories to the input of the D/A converter. The analog output of the D/A converter is used to display the recorded spectrum on an oscilloscope screen synchronous with the recording of the spectrum. The channels are displayed sequentially and the multiplexer alternates between the two memories. The principle is shown in Fig.3.

The multichannel analyzer has two principal modes of operation: INTERNAL and EXTERNAL TRIG. In the INT TRIG mode of operation a pulse provided by the address counter of memory A is used to trigger the electron source of the spectrometer. This pulse is generated when the address counter is in the last channel of the memory. The repetition rate is thus about 1.2 kHz. The EXT TRIG input is provided to make the instrument usable with electron sources that can only be triggered with frequencies of less than

1.2 kHz or are non-triggerable but themselves provide a trigger pulse.

2b The memory with address counter, arithmetic unit and control circuits

Fig.4 shows the circuit diagram of memory A, arithmetic unit A, address counter and control circuits. The corresponding circuit diagram of memory B with associated circuits is identical to Fig.4 excluding IC 4b, IC 6a and b, IC 7a, IC 9a and b, IC 8a and TR 1.

The arithmetic unit consists of the circuits IC 10c and d, IC 5 and IC 2. IC 1 is the address counter and the memory is IC 21. The other circuits in the diagram are to be referred to as control circuits.

The memory is built around Intel's 2147 H-1, a 4096 x 1 bit static RAM/1/. 2147 H-1 is directly TTL-compatible and has an access time of 35 ns. Each memory consists of 16 packages, which gives the capacity of 64 k counts. Tne address counter IC 1(3 x 74S163) provides twelwe parallell address bits. When a channel is addressed, data is read out from the RAM into a latch and clocked through the latch to the adder. If there is a new count present at the Least Significant Bit (LSB) input of the adder (the data aquisition will be described below), it will be added to the previous number of counts and the new number is written into the RAM by the write-pulse, $\overline{WE}$. If there is no new count, the old (previous) number is written back into the RAM. The data hold time of 2147 H-1 is minimum 10 ns and the latch IC2 prevents input data to the adder from disappearing with the write-pulse. 4 x 74S175 with a maximum propagation delay time of 17 ns are used as the latch /2/.

The latch is clocked by the positive-going edge of the output pulse of a monostable multivibrator, IC 3a. IC 3a is triggered by the positive-going edge of the output pulse of another monostable multivibrator, IC 3b, which is triggered by the clock pulse to the address counter. The latter multivibrator is used as a delay to compensate for the access time of the RAM and to

generate the write-pulse, as will be described below. The outputs of the latch are connected to the A-inputs of the adder IC 5 (4 x 74S283). The LSB-input of the adder is connected to the arithmetic unit and the other fifteen B-inputs are connected to ground. The add-time of two 16-bit words is typically 30 ns /2/.

The data aquisition can be stopped either manually or automatically. The STOP mode is selected by the switch S1, which has two positions: AUTO STOP and MAN STOP. In the AUTO STOP position the data aquisition is stopped when any channel is filled (64 k counts). In the MAN STOP position the data aquisition can be stopped at any time, which gives a possibility to study weak features of the spectrum.

The 16-bit word present at the output of the adder is written into the RAM by the write-pulse, $\overline{WE}$, which is provided by the monostable multivibrator IC 4a. The output of IC 4a is taken to one of the inputs of the 4-input NAND-gate IC 11a. The write pulse is enabled to the RAM if the other three inputs of the NAND-gate are at logic high. As will be described below the NAND-gate inhibits the write pulse in three different cases:

i. Protection of the content of a filled channel.

ii. A filled channel stops the data aquisition in the AUTO STOP mode of operation.

iii. External trigger operation.

IC 4a is triggered by the negative-going edge of the output pulse from IC 3b. The 25 kΩ potentiometer connected to IC 3b makes it possible to adjust the start time of the write pulse. The timing diagram of the memories and the arithmetic units is shown in Fig. 5. Due to the mode of operation the inhibition of the write pulse through IC 4a is accomplished in the following three ways:

i. If the switch S1 is in the MAN STOP position and a channel at any

moment stores 64 k counts, i.e. all 16 A-inputs of the adder are at logically high, a new count would give an adder output of 16 zeros, logic low, and a carry out. The result would thus be zero in that channel. To prevent a filled channel from going to zero the carry out signal is used to inhibit the write pulse through the inverter IC 9d and the NAND-gate IC 11a.

ii. If the switch S1 is in the AUTO STOP position a carry out from any channel of the two memories sets the output of the flip-flop IC 6a to logic low. IC 6a lights an OFLOW LED (Light-Emitting Diode), which indicates that at least one of the channels is filled and the data aqusition is stopped by preventing the write pulse to the RAM through IC 11a. In the MAN position of S1 the output of IC 6a is logic high and the data aquisition is not stopped when a channel is filled but the channel is still held at 64 k as described above. S1 is shown in the MAN position in the circuit diagram. When the aquisition is stopped in the AUTO STOP mode, the whole memory must be CLEARED before restart. This is accomplished by pushing the CLEAR button, which resets IC 6a and triggers the monostable multivibrator IC 4b, set to 1 ms. This pulse clears the latch, i.e. sets the latch outputs to zero, and the A-inputs of the adder to zero. These zeros are written into every channel of the RAM. The total length of the two memories is 819.2 μs and the 1 ms pulse is long enough to make sure that the content of every channel is zero after a CLEAR pulse.

The function described above is obtained with S2 in the INT TRIG position, as it is in the circuit diagram, which gives a logic high output from IC 6b.

iii. If S2 is in the EXT TRIG position the output of IC 6b is set to logic low. This logic low inhibits the write pulse to the RAM through IC 11a. The output pulse form IC 7a, with a length of 200 ns, is used to reset the address counters of the memories and to set the output from IC 6b to logic

high. After one memory cycle (8192 address cycles) IC 6b is reset by the ripple carry out pulse from the address counter of memory A. Accordingly it is possible to write counts into the RAM during one memory cycle after an external trigger pulse. IC 6b is reset after one memory cycle to prevent electrons with a flight time of more than 819.2 µs from beeing counted as if they had a much shorter flight time (Second-time-around-suppresion).

The memory can be CLEARED during any mode of operation. Pushing the CLEAR button resets the memories as described above.

2c Data aquisition

The detector pulse is fed to a NAND-gate, IC 10a, followed by a S-R latch, IC 10c and d. The detector pulse sets the latch if IC 10a is enabled. IC 10a is enabled by clock pulses through IC 12a, which is a NAND-gate used as an inverter. The data aquisition time of a channel is determined by the length of the enable pulse, which is set to 100 ns as described above. The corresponding input circuits of arithmetic unit B are identical to those of Fig. 4. When IC 10a of arithmetic unit A is enabled, IC 10a of arithmetic unit B is not and vice versa. To provide adjustment of the window ratio between the two latches, the rise time of the enable pulses to the NAND-gate can be slightly lengthened by increasing the 5-50 pf trimmer on the output of IC 12a. This adjustment is made by connecting a random pulse generator to the input and adjusting for minimum 5 MHz ripple of the display.
The trailing edge of the write pulse is used to reset the S-R latch. It is delayed 10 ns to make sure that the RAM is incremented before resetting. IC 9c (74S04), a 50 Ω resistor, a 100 pf capacitor and IC 10b (74S00) are used to produce a reset pulse with a length of 10 ns.
The input capacity can easily be increased: a double set (one for each

arithmetic unit) of the circuits IC 9a and b, IC 10a c and d is needed for each additional data bit.

2d Clock circuits

Fig. 6 shows the circuit diagram of the clock and output circuits. The clock pulses are generated by a 10.00 MHz crystal oscillator. The 10.00 MHz frequency is divided by two in the flip-flop IC 17a. The function described above is obtained with S3 in the COUNT position, as it is in the circuit diagram. The READ OUT operation will be described below. The 5 MHz clock signal to the address counters is fed through the NAND-gates IC 19a and c. The address counter 74S163 can only be triggered by positive-going edges, but the address counter of memory B must be triggered by the negative-going edges of the clock signal as described above. This is accomplished by the inverter IC 12d, which gives the inverted clock signal to the address counter of memory B.

The pulses taken from b in the circuit diagram of Fig. 6 generate the enable pulses to the arithmetic units through the NAND-gates IC 12 a (cf. Fig. 4).

3. Display of spectra

3a Oscilloscope display

The recorded spectrum is continuously displayed in real time on an oscilloscope screen during the counting. The oscilloscope must have a rise time, $\tau_r \leq 35$ ns. The output circuits are shown in Fig. 6. The sixteen data bits from each memory are taken to IC 13, which is the multiplexer (cf. section 2a). The data selection is accomplished by the clockpulses to memory B. The 8-bit SCALE-switch, operated manually, is connected to

the output of the multiplexer. By the switch eight successive bits of the memory data are selected and fed into the D/A converter, TDC 1016J-8 /3/. The analog output of the converter spans -1 to 0 volt. The converter is clocked by the write pulses to the memories through IC 12b and thus the display is synchronous with the writing.

3b Trigger delay

In a comparator, IC 16 (3 x 7485), the address to memory A is compared to the binary set value set by six address preset manual switches. The A = B output of the comparator is used to trigger the oscilloscope used for the display. With this arrangement it is possible to start the display of the recorded spectrum at any position in steps of 12.8 μs. In order to study a given portion of the spectrum in detail, the time scale can be expanded using the timebase-selector of the oscilloscope.

3c External trigger

An EXT TRIG recorded spectrum can be displayed similarly as described above. However if the spectrum is displayed during the EXT TRIG mode of operation it can look confusing. To exemplify, let us assume that a spectrum is written out to channel 1000 when an external trigger pulse arrives. The external trigger pulse resets the address counters as described above. Then the first part, in this case 1000 channels, will be written out again. Thus, we can not be shure that the real spectrum is displayed in the EXT TRIG mode, but the recorded spectrum is real and can be correctly displayed in the INT TRIG mode of operation after completion of the recording. The problem associated with the EXT TRIG operation can be avoided by connecting a D/A converter to the address bus. The analog output of the converter can then be used for X-deflection of the oscilloscope instead of the internal timebase.

3d. Chart recorder display

IC 18 is a divider with an output frequency of 1 Hz. The 1 Hz-frequency is used to clock the memories when S3 is in the READ OUT position. The change of clock frequency from 5 MHz is triggered by the A=B pulse from the comparator IC 16. It is thus possible to connect a X-Y recorder to the analog output and to start it with the A=B pulse (Trig osc.). By the arrangement with IC 17a we can select the start channel for the read out as earlier described and read out the part of the spectrum which is of interest. The possibility of selecting the start channel of the read out saves a lot of time when the spectrum is proceeded by a long time before anything interesting appears. The READ OUT clock frequency can easily be changed to 2, 5 or 10 Hz by changing the dividing factor of IC 18.

4 Spectrometer operation and investigation of resolution

The time-of-flight electron spectrometer has an axially symmetric vertical magnetic field with $1/r^2$ dependence. The mean radius is 120 mm and the field there is about 0.1 T. In this field electrons with equal energy emitted from a plane, which is determined by a radial and the axial direction of the magnetic field, arrive simultaneously at a similar plane at another radial direction. In order for the electrons to reach the detector the direction of the velocity vector, when they depart from the target, is not limited at all in the horizontal plane and to about $\pm$ 6 degrees in the vertical plane. The drift velocity of the center of the trochodial trajectory is several orders of magnitude smaller than the absolute velocity of the electrons. The flight time τ is proportional to the inverse of the electron kinetic energy E /4/.

The present experimental study has been carried out to determine an upper limit of the spectrometer resolution and to identify different contributions

to the line width. An electron scattering arrangement was used for this purpose. Spectra were obtained by scattering electrons emitted from a non-monochromatized electron gun against a solid target. Fig. 7a shows a photo of a typical time-of-flight spectrum displayed on the oscilloscope screen. The spectrum essentially consists of a sharp peak at a flight time of about 160 μs due to elastically scattered electrons. For longer flight times a weak unstructured background can be inferred due to inelastically scattered electrons and secondary emission. A detailed study of the elastic peak shows that it contains one weak maximum at 145 μs in addition to the main peak at 160 μs. The 25 V pulse, which accelerates electrons from the electron gun into the target region (cf. Fig. 1), gives rise to the main peak. The weak feature at 145 μs arises from an overshot of $\simeq$ 3 V in the accelerating pulse as shown in Fig. 1. The width (FWHM) of these peaks is $\simeq$ 0.7 eV due to the thermionic emission process at the cathode of the electron gun.

In order to study the resolution of the spectrometer it is necessary to monochromatize the electrons to some extent. This is achieved by perturbing the electron packet by a short voltage pulse produced by an electrode assembly inside the spectrometer (cf Fig. 8). By a variable time delay with respect to the cathode pulse the voltage pulse can be adjusted to hit different parts of the electron packet. When the pulse is adjusted to hit the elastically scattered electrons a monochromatization of these electrons is obtained. Repeated recordings with the same time settings gives rise to a narrow peak in the spectrum. The result of such an experiment is shown in Fig. 7b and schemetically in Fig. 8. The electrode assembly is 0.3 mm thick and consists of three mutually insulated vertical metallic sheets. The outer electrodes are connected to an adjustable DC voltage ($\pm$ 1 V) to compensate for contact potentials, and the central electrode is

connected to a 5 V positive pulsed voltage, 50 ns wide. Alternatively an ordinary electrostatic monochromator could have been used. However, due to the intense ($\simeq$ 50 mT) magnetic fields surrounding the spectrometer this type of monochromatization can not be used without extensive shielding arrangements.

The full experimental procedure described above of a single cycle including the monochromatization is summarized in the following three points:

1. Electrons with an energy of 25 eV are injected through a hole in the pole piece along the lines of magnetic flux in a 100 ns wide pulse. The electron packet is then scattered by a solid target.
2. After $\sim$ 1/4 of the flight path the dispersed electron packet passes very close to the electrode assembly. The pulsed voltage produces a perturbation, localized in space, on the electron packet.
3. The electrons are detected by a Multi Channel Plate detector at the end of the flight path. The detector pulses are fed into the multichannel analyzer through an amplifier (cf Fig. 1).

In this study (E=25 eV, τ=160 μs) the resolution limit is about 100 meV. This value can be explained as entirely caused by the cathode pulse width, the initial beam geometric distribution in the flight direction and the fringing field from the electrode assembly.

5 Forthcoming investigations

When feeding the spectrometer with gas at very low preassure, the electrons are scattered by the gas, elastically and inelastically, and the transmission will be changed. The formation of stationary or quasi-stationary states in the collision between an electron and a target gas atom or molecule will be reflected by a change in transmission only at the energy of the state. This will give rise to a peak- or dip-shaped variation in the count-rate for a

continuous energy distribution of electrons passing through the analyzer. The energy width of such peaks or dips will not be influenced by the broadening mechanisms discussed above but will essentially reflect the width of the electron-atom state. In recent studies of this kind, using He as target gas, a quasi-stationary state of He^- has been observed with a line width of less than 40 meV. Further work is in progress along these lines and the results will be presented in a forthcoming report together with a more detailed description of the spectrometer /4/.

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1. Intel 2147H specification, Intel corporation 1980

2. The TTL Data Book, Texas Instruments 1976

3. TRW TDC 1016J-8 specification, TRW Inc 1981

4. K.E. Norell, P. Baltzer, B. Wannberg and K. Siegbahn, in course of preparation.

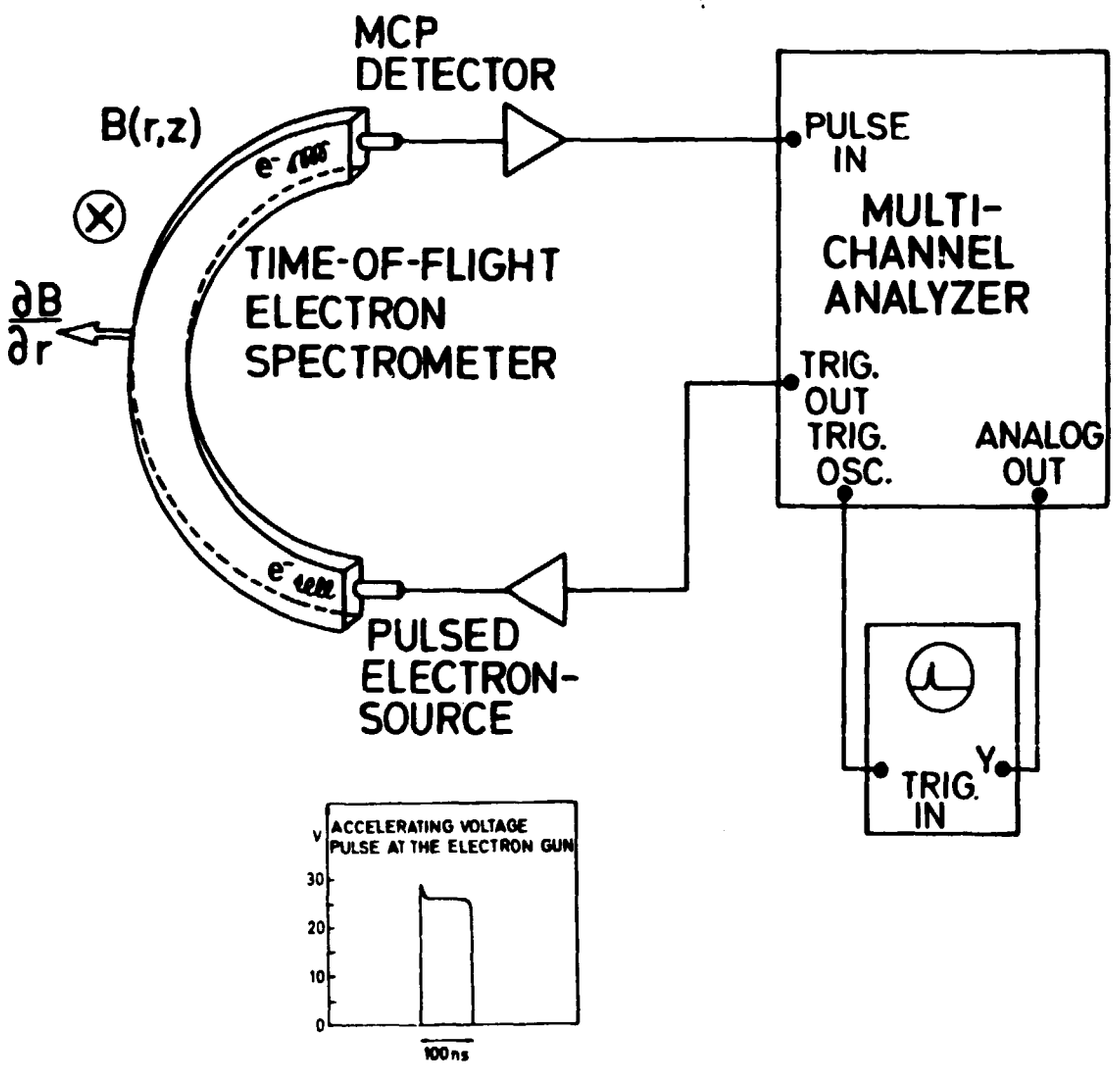

Fig. 1 Experimental set up

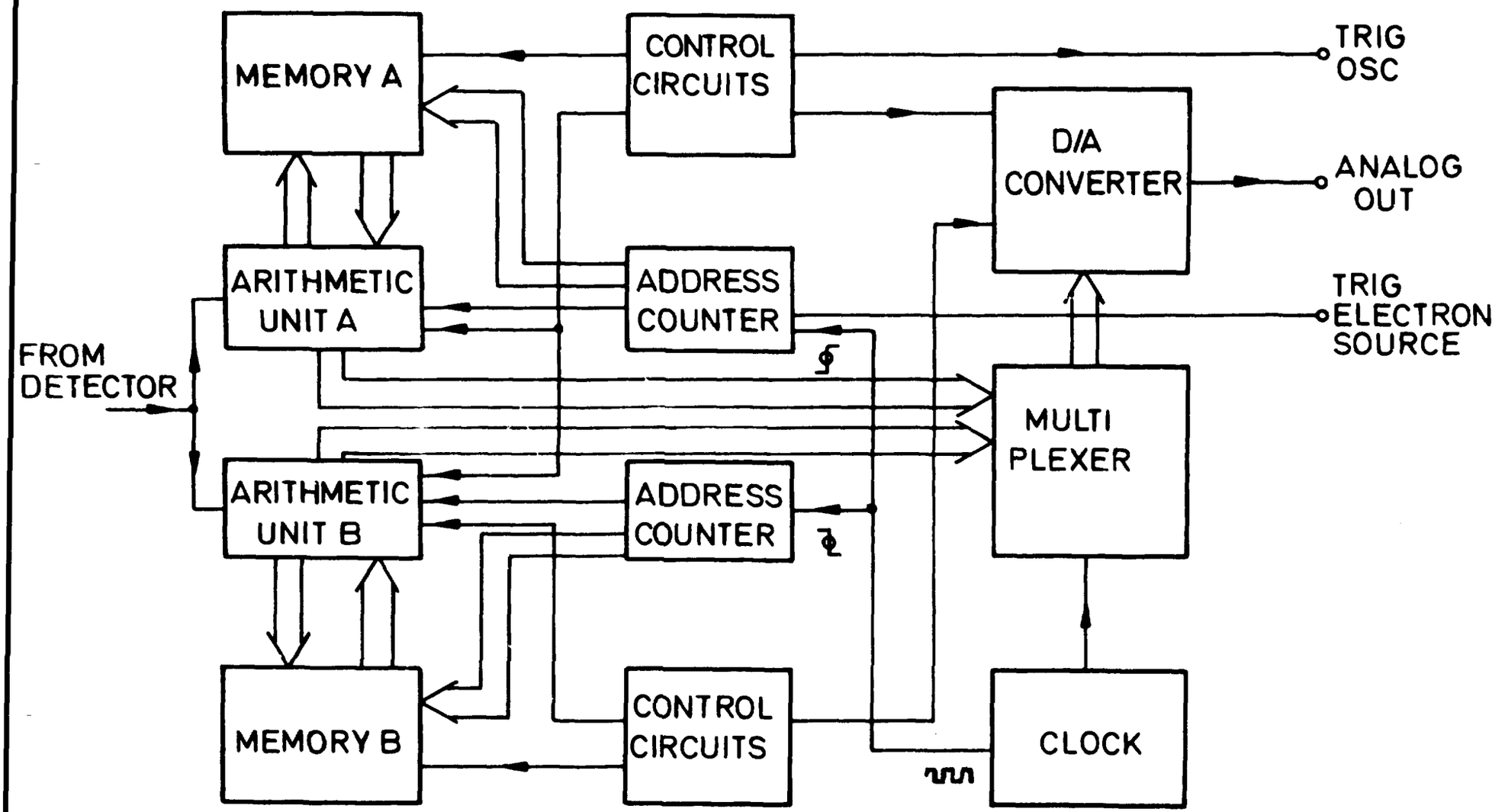

Fig. 2 Block diagram

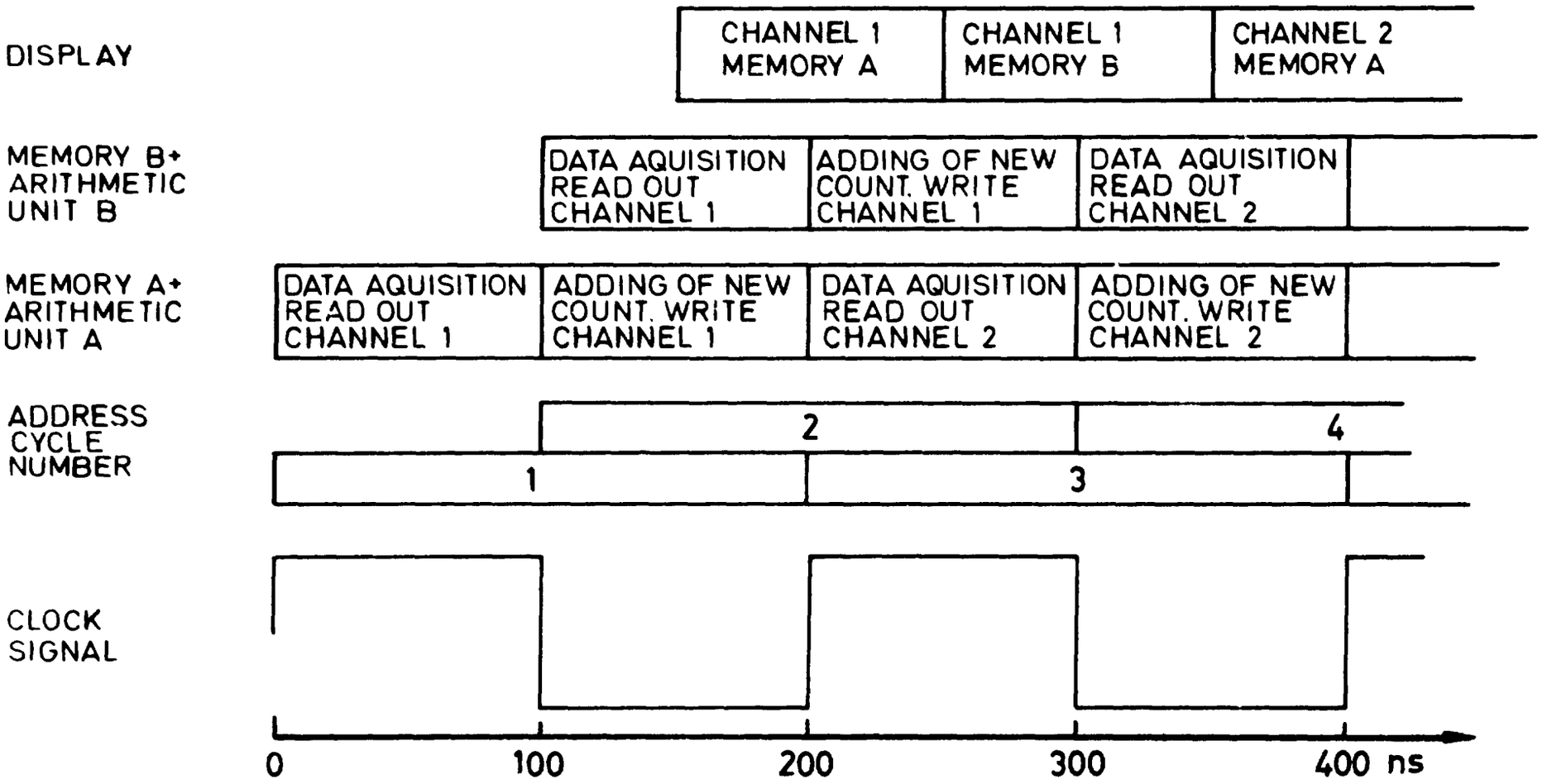

Fig. 3 Clock signal and address cycles of the memories

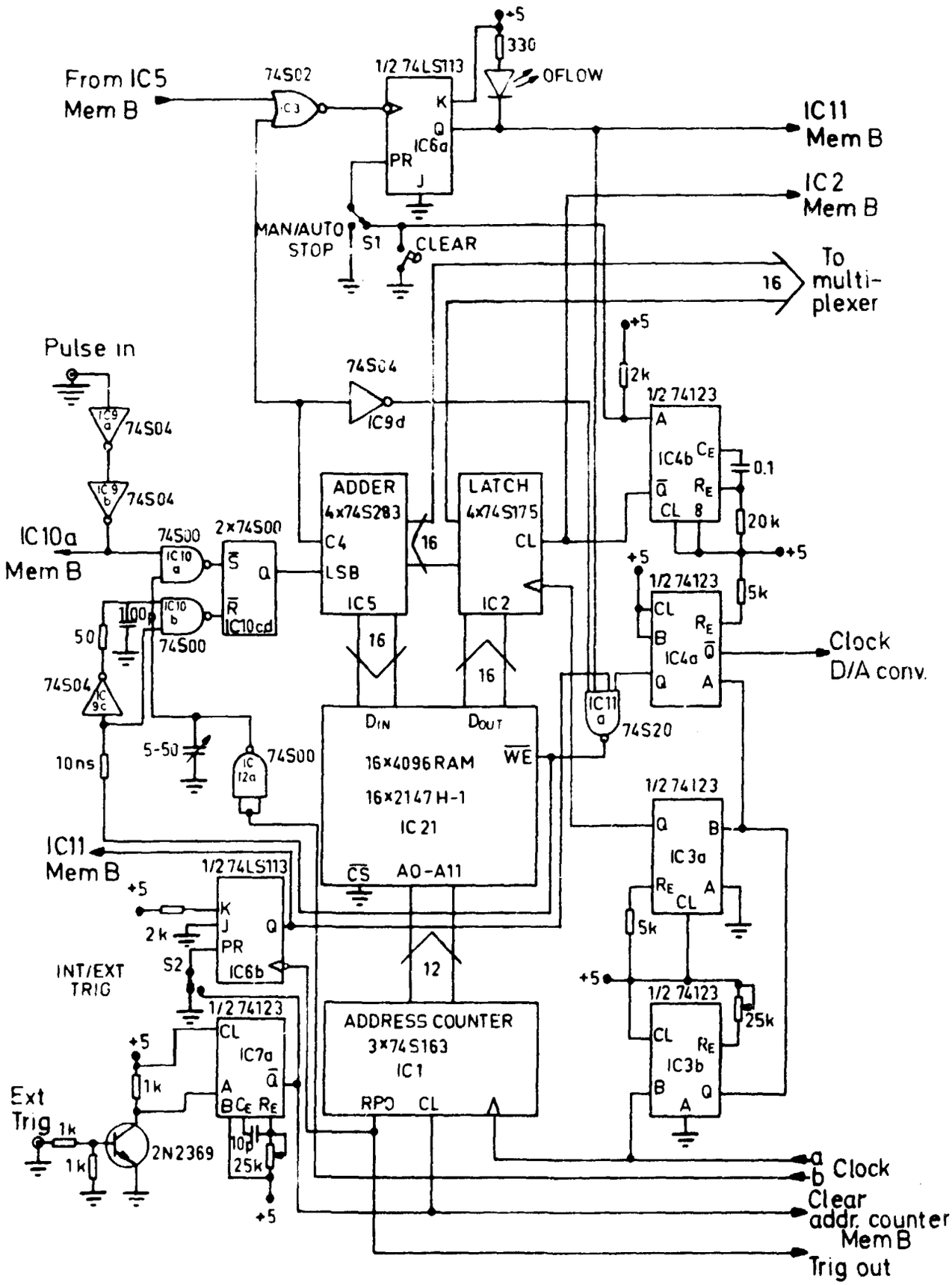

Fig. 4 Circuit diagram of the memory, arithmetic unit, address counter and control circuits

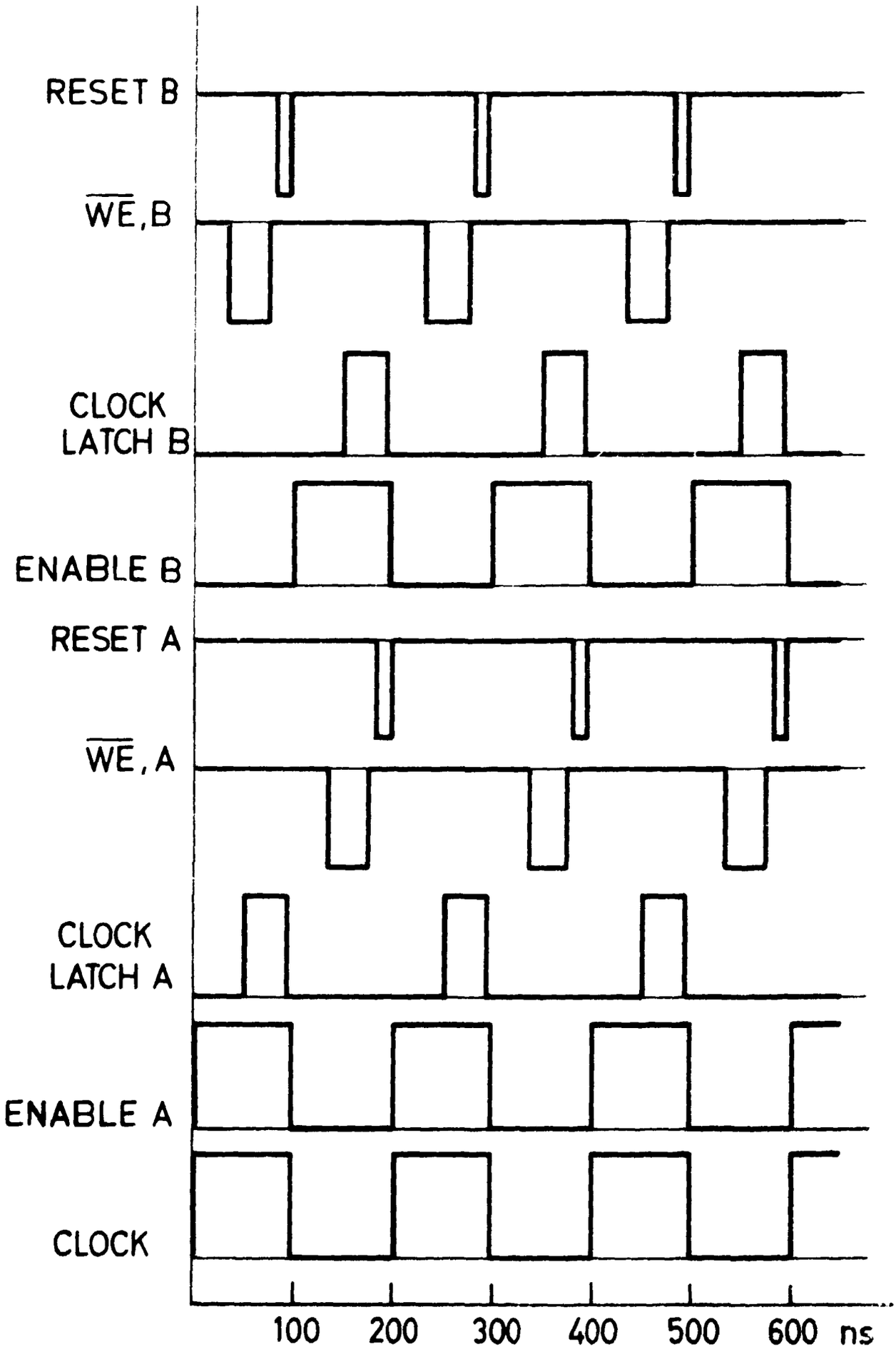

Fig. 5 Timing diagram

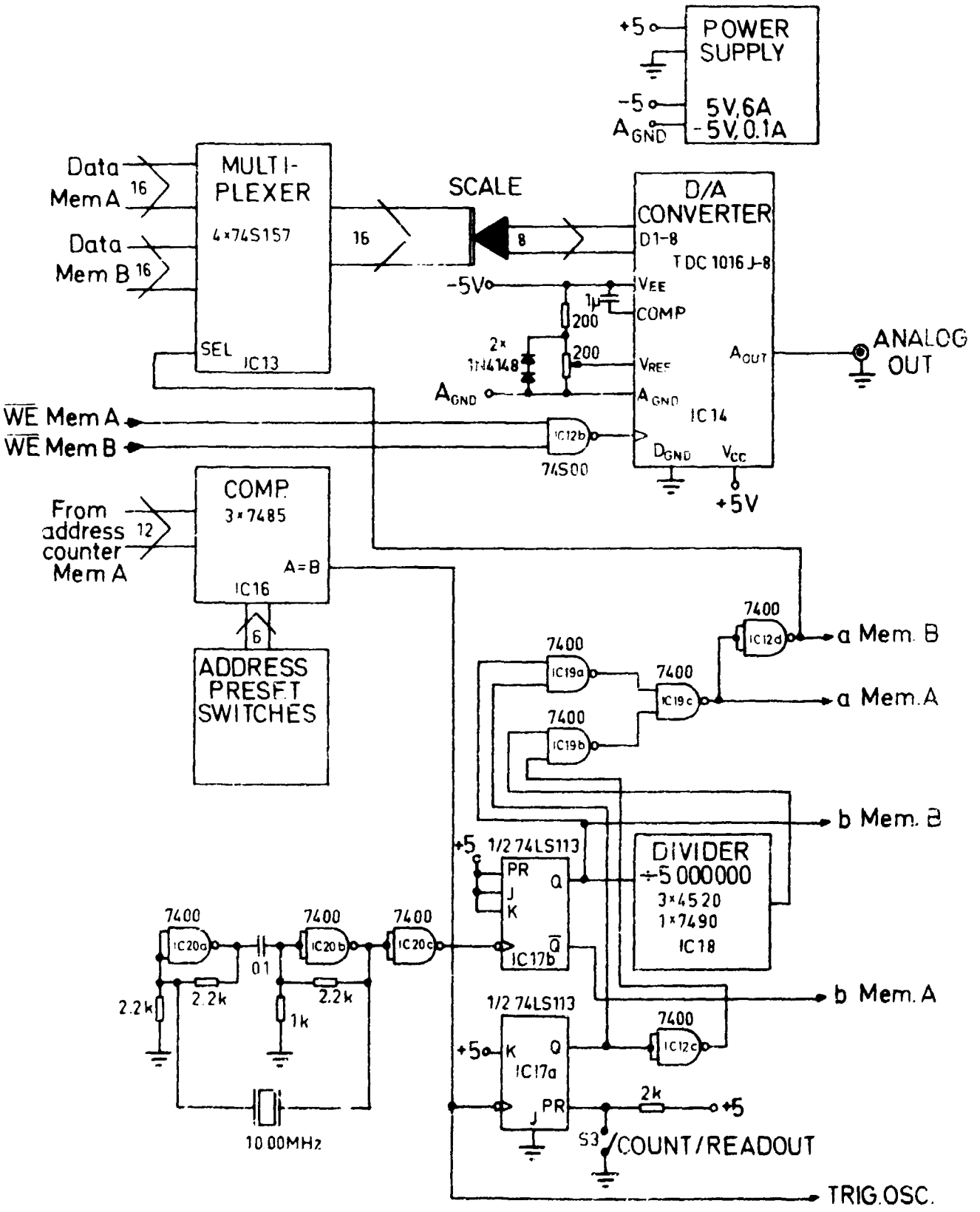

Fig. 6 Clock and output circuits

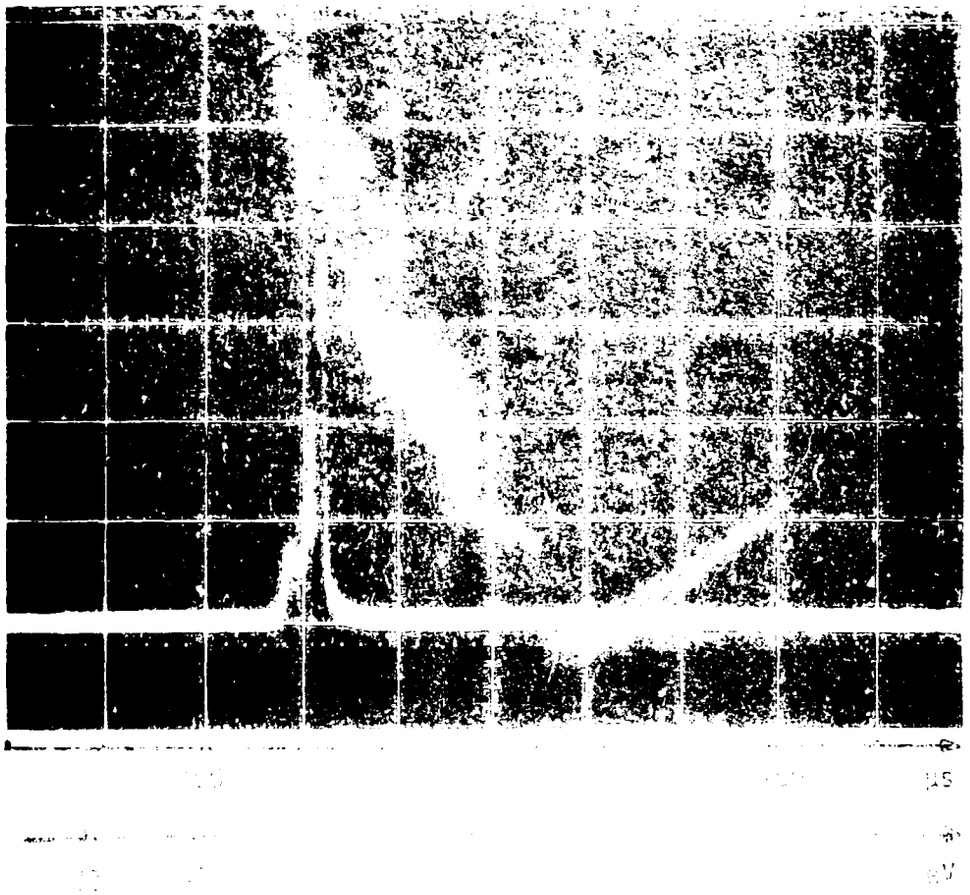

Fig. 7a

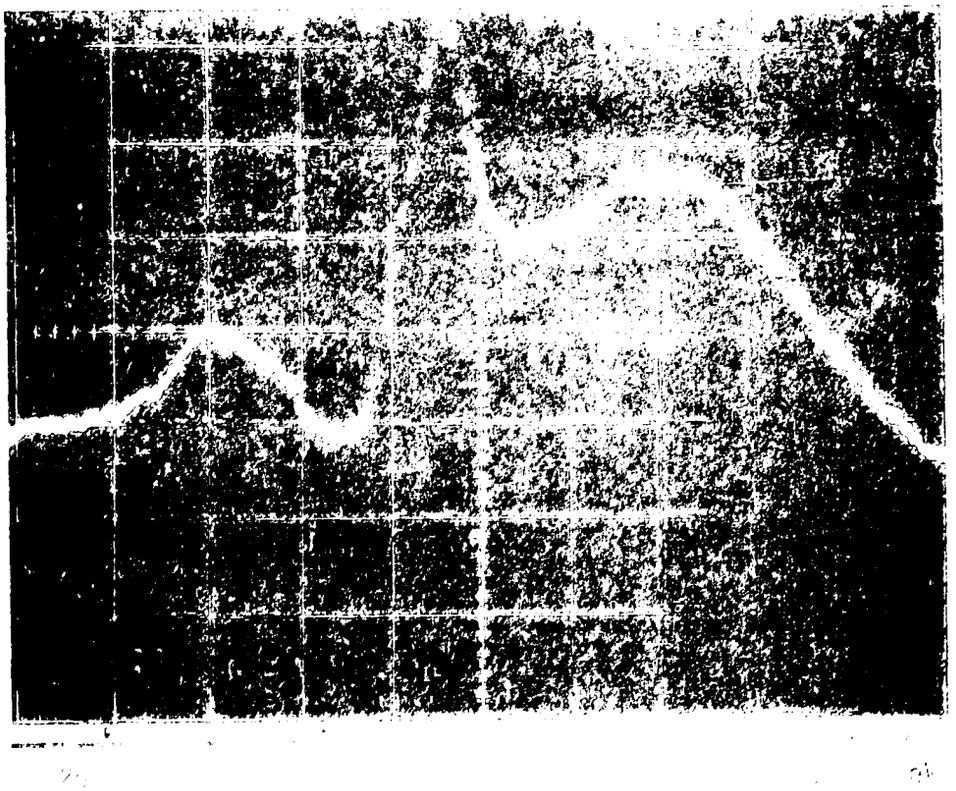

Fig. 7b

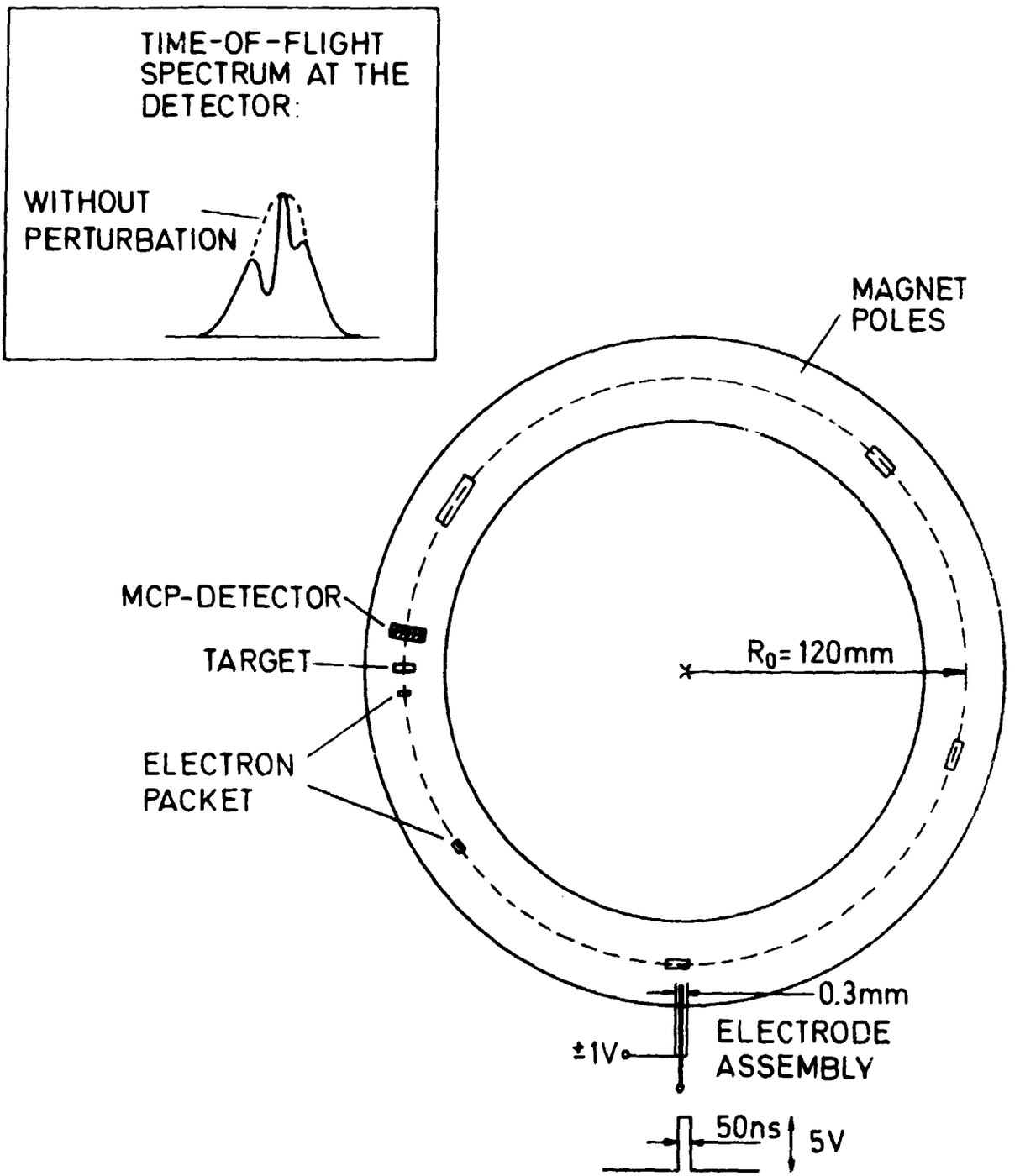

Fig. 8 Top view of the time-of-flight electron spectrometer drawn schematically. The same electron packet is shown in different parts of the flight path.