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THE MARK-II DATA ACQUISITION AND TRIGGER SYSTEM*

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ABSTRACT

The Mark-II Data Acquisition and Trigger system requirements and general solution are described. The solution takes advantage of the synchronous crossing times and low event rates of an electron positron collider to permit a very highly multiplexed analog scheme to be effective. The system depends on a two level trigger to operate with acceptable dead time. The trigger, multiplexing, data reduction, calibration, and CAMAC systems are described.

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1. Data Acquisition System Requirements and Goals

1.1 INTRODUCTION

The SLAC-LBL Mark-II Magnetic Detector is a large solenoidal detector originally designed for the storage rings SPEAR and PEP. The detector includes a large drift chamber system surrounded by Time-of- Flight (TOF) scintillation counters, followed by the solenoidal coil, liquid argon electromagnetic shower counters, the iron flux return, and layers of muon detectors, as sketched in Figure 1.

The basic task of the data acquisition system is to process coherently the front end data from the various detectors and present an optimally compacted and corrected data stream to the on-line computer. Additionally, the trigger system is integrated with the data acquisition system to allow combinations of calorimetric and tracking trigger conditions at reasonable economic and dead-time costs. Finally, the system is designed with calibration systems that are useful for the debugging and periodic verification of system performance as well as calibration.

This paper will describe the Mark II systems as designed for SPEAR and PEP but not the upgrade program for the SLC Collider.

The basic solution to this design problem is to take advantage of the periodic beam crossing times of an electron-positron storage ring to permit the design of inexpensive, synchronous, time to amplitude converters and sample and hold modules, and to take advantage of the low data rate to heavily multiplex the more expensive components of the system. A necessary condition, therefore, is a trigger system which reduces the event rate to at most a few Hz, so that the data acquisition system can be slow compared to those traditionally used with hadronic experiments and still incur little dead time.

1.2 DRIFT CHAMBER REQUIREMENTS

The drift chamber consists of 16 layers with a total of 3204 sense wires. The drift chamber system only measures the drift time for the first track in any cell. The maximum drift time is about 500 ns, and the required precision ~ 1 ns. The front end electronics consists of a hybrid preamplifier-discriminator- differential ECL line driver. No attempt is made to measure the signal amplitude or multiple tracks resulting from a single interaction. (At PEP and SPEAR energies, the probability of multiple tracks in a single drift chamber cell is negligible). Thus, the data acquisition problem is to adequately measure the drift times and, for cells which had tracks, to pass the data to the computer input stream.

1.3 CALORIMETRY REQUIREMENTS

The liquid argon barrel system has about 4000 channels organized as strips which measure orthogonal θ and ϕ coordinates and a third, ambiguity resolving U coordinate running at 45° to the θ and ϕ strips. The system also supported one liquid argon endcap calorimeter and a proportional chamber endcap calorimeter. The liquid argon endcap was eventually replaced by a similar proportional chamber endcap. The preamplifiers are transformer coupled, JFET input charge amplifiers, followed by bipolar shaping and a transformer driven differential output pair of the classic Radeka[1] design. The analog measurement range goal was 30:1 with approximately 1% accuracy, implying a dynamic range equivalent to about 11 bits. The data acquisition problem is to sample and hold these signals and process those sufficiently above the electronics noise threshold for the data stream.

1.4 TIME-OF-FLIGHT REQUIREMENT

The time-of-flight system consists of 48 strips of 2.5 cm thick plastic scintillator between the drift chamber and the solenoid. Each scintillator is viewed by a photomultiplier at each end. The signal from the photomultiplier is carried directly to the data acquisition system by high quality cable (RG-8 equivalent) without any preprocessing on the detector. The data acquisition goal was to design instrumentation that would extract all the useful information from the photomultiplier signal. The result is a measurement of the threshold crossing time for both "high" and "low" thresholds, and a measurement of the signal integral. The accuracy of the timing measurement is better than 50 ps, and the signal integral is measured to better than 5% . The combination of measurements allow correction for the finite risetime of the signals from both light collection effects in the scintillator and light-pipe and electronic effects in the photomultiplier and cable. The discriminator threshold values are in the range of 15 to 100 mV.

1.5 TRIGGERING REQUIREMENTS

The trigger system permits combinations of calorimetric and charged track requirements. The trigger must operate with little deadtime. For the tracking system, the requirement is to find tracks that point to the beam line with high efficiency in the presence of noise from background photons and defective electronics channels. The tracking trigger uses information as to whether a cell has been hit or not (as opposed to when it was hit), and must easily adapt to drift chamber problems such as inefficient layers. The system counts the number of tracks found, so that the trigger requirement might be, for example, "two charged tracks" or "one charged track and calorimeter energy above some threshold."

For the calorimeter, the first task of the trigger system is to add the signals from each of the barrel modules and endcaps until there are only ten sum signals. These signals are then discriminated and fed to logic so that calorimetric counting can be done, and the ten signals are also added to form a detector total energy signal.

1.6 FLEXIBILITY

An additional important system design requirement is flexibility. The detector is sufficiently large and complex that all components do not work perfectly at all times. Consequently the data acquisition system and trigger must be prepared to "ignore" bad channels or subsystems until they are repaired. Additionally, improvements are made in the detector, and the data acquisition system should be designed to gracefully accommodate additions and changes. An example of such a change is the small angle drift chamber system installed at PEP to study two-photon interactions.

2. The General Solution

2.1 INTRODUCTION

The important aspects of the electron-positron storage ring for the trigger and data acquisition system are the synchronous crossings of the beams at relatively high rates (every 780 ns for SPEAR and 2.4μs for PEP) and the low physics event rates of less than 1 Hz at luminosities $\lesssim 1 \times 10^{31}$ cm^{-2} s^{-1}. The solution is a two tiered trigger system consisting of a primary, deadtimeless trigger capable of reducing the crossing rate signal of the machine (1.28 MHz at SPEAR) to at most a few KHz, and a secondary trigger system capable of reducing the primary rate to about 1 Hz. This trigger system is coupled with a data acquisition system that can accept data and then either 1) be reset and ready to accept new data in 200 ns, 2) or hold the data while the secondary trigger and possibly full data acquisition process goes on. If the primary trigger can be complete in the intercrossing period less the data acquisition reset time, then no signal delay cables are needed to "store" the signals while the trigger decision is made. This is an important economic and performance point, but it constrains the detector design so that $\tau_s + \tau_{pt} + \tau_r < \tau_c$, where τ_s is either the maximum drift chamber drift time or calorimeter charge collection time, τ_{pt} is the primary trigger time, τ_r is the reset time, and τ_c is the storage ring crossing time. This constraint is easily satisfied at the larger storage rings, but is moderately challenging at SPEAR!

The data acquisition modules are Time-to-amplitude Converters (TAC's) for the drift chambers, Sample and Hold Analog Module (SHAM)(2) for the calorimeters, and DISCO's(3) for the time-of-flight system. Block diagrams for these modules are shown in Figures 2-4. In all cases, shortly after the beam crossing the data is stored as a voltage on a capacitor. If the primary trigger decision is negative, the capacitor is discharged in time for the next crossing. If the primary trigger decision is positive, the reset and input gate signals are withheld and the secondary trigger is started. If the secondary trigger is negative, then a reset is applied and the process continues. If the secondary trigger is positive, then the resets and gates are still withheld, and a highly multiplexed readout process is initiated, using the organization indicated in Figure 5.

The data acquisition modules contain 32 channels per single width CAMAC module (TAC's and SHAMS) and 12 effective channels per single width DISCO module. Each of the data storage capacitors in the system is buffered by an FET input operational amplifier and multiplexed onto a CAMAC crate wide analog bus under the control of a high speed programmable processor and analog-to-digital converter called the Brilliant ADC (BADC)[(4)]. Thus the relatively expensive BADC is shared among 604 channels in a TAC or SHAM crate. The BADC digitizes each channel and compares it to a stored threshold value ϵ_i. If the data value Q_i exceeds ϵ_i, the processor computes a corrected value $Q'_i = \alpha_i(Q_i - \delta_i) + \beta_i(Q_i - \delta_i)^2$. The four constants associated with each channel are the result of the calibration process and are setup so the Q' is in "physics" units such as 10^{-10} seconds for the drift chambers and 0.1 MeV for the SHAM's. The data is then associated with a logical channel name and placed in an output buffer. Data from channels with $Q_i < \epsilon_i$ are discarded. The BADC's take 5-10 ms to complete the scanning and processing of the data acquisition modules. Finally, the host computer, a VAX 11/780, is interrupted and reads all the BADC's and a few other modules through a VAX CAMAC Channel[(5)] in a total elapsed time of about 40 ms.

The deadtime is simply $R_{pt} \cdot \tau_{st} + R_{st} \cdot \tau_{da}$, where R_{pt} and R_{st} are the primary and secondary trigger rates, typically 1000 Hz and 1 Hz for Mark II at SPEAR, and τ_{st} and τ_{da} the secondary trigger and data acquisition times, about 34 μs and 40 ms respectively, for a deadtime of about 7%. The system design goal was 10%.

2.2 THE PRIMARY TRIGGER

The primary trigger is a simple OR of a charged and neutral trigger. The charged trigger is an AND of a fast system in coincidence with the beam crossing signal and Drift Chamber Majority (DCM). The first signal is used to limit the cosmic ray rate and was originally generated from a scintillation counter covering the beam pipe. This counter was replaced by a precision vertex drift chamber, and the timing window now comes from the time-of-flight counters. The DCM signal is a requirement that some number of the drift chamber layers have at least one hit cell. This signal is generated by ORing the TAC OR outputs for each layer. (This logic is not shown in Figure 2; it is the OR of the 32 flip-flop outputs for the module). A typical requirement is 4 of 9 drift chamber layers, resulting in an adequately low primary rate and a very high efficiency for tracks going through all the layers of the drift chamber, i.e., tracks with $P_T > 100$ MeV/c and $|cos\theta| \leq 0.65$.

The neutral trigger is derived from simple thresholds on the calorimeter sum signals. This is not trivial to do at SPEAR because the τ_{pt} requirement limits the shaping time that can be used with the liquid argon preamplifiers, so that signal to noise in the sum signal is a problem. Additionally, the calorimeter is sensitive to cosmic rays which traverse the calorimeter parallel to the radiator structure.

Other special primary triggers are used to enhance cosmic ray rates and permit calibrations.

2.3 THE SECONDARY TRIGGER

The purpose of the secondary trigger is to find tracks originating from the beam line and going through the drift chambers; Random noise hits should not cause a track to be found. The tracks are helices, and, in transverse projection are arcs of circles going through the origin, as shown in Figure 6. The general track finding principle is to form a road in the chamber, for example the area between arcs ℓ_1 and $\ell-2$ in Figure 6. This road is then rotated about the chamber in steps of drift chamber cells. Multiplicity logic then determines whether a road covers a track. The road finding operation can be carried out in parallel by modules which search with roads of different curvature, thus finding all tracks in one rotation of the roads. A full set of roads is indicated in Figure 7.

The actual implementation uses shift registers to pass the data through Curvature Modules. A simplified diagram is shown in Fig. 8. The shift registers are those indicated in the TAC block diagram of Figure 2. The shift registers are chained together to form complete layers of the drift chamber. The data then passes through a set of curvature modules, one of which is indicated in Figure 8. The widener circuit adds extra bits to the input data and corresponds to the width of the road W between the arcs of Figure 6. The data then go through Variable Length Shift Registers (VLSR) which effectively define the delays d_i of Figure 6 and thus the curvature of the road. The resulting outputs of the VLSR's are used to address a memory which has been preprogrammed with a truth table defining the sets of hits within a road which will be accepted as a track. All possible combinations of VLSR outputs correspond to different locations in this memory, so that any set of requirements may be imposed. (For example, at least 9 of 12 layers must have a hit). The actual implementation used a memory two bits wide, so three different quality classes (as well as no track) could be defined.

A block diagram of the actual system is indicated in Figure 9. The system uses 12 shift registers with data coming from all the axial and the inner stereo layers of the drift chamber and from the time-of-flight counters. About 24 curvature modules are simultaneously used. Outputs from the curvature modules are recorded by three Track Counters. The Track Counter outputs are fed to a trigger control box containing another logic memory to make the final trigger decision, and are also fed to the input data stream. These data contain the azimuthal position and curvature of the track and are used to guide the track-finding software. The entire system is implemented in CAMAC and occupies 3 crates of logic. The system is described in much greater detail in Ref. 6.

The secondary triggers are comprised of about 15% e^+e^- annihilation events at SPEAR, with the remainder being cosmic rays and beam gas or beam wall interactions. Although this trigger performance has been adequate, an important improvement would be to add longitudinal resolution, since the dominant backgrounds are uniformly distributed in Z. This is probably impossible if the only Z information comes from stereo drift chamber wires, but should be possible with a cathode pad or current division system. A simpler improvement would be to add layers from a vertex chamber, as was done when Mark II was moved to PEP, to improve the trigger impact parameter resolution.

2.4 THE MULTIPLEXED DATA ACQUISITION SYSTEM AND CALIBRATIONS

The details of the individual modules of the system have been published elsewhere[2–5] and will not be repeated here. The primary motivation for this multiplexed approach is economy, in that most of the expensive components, such as the ADC, are repetitively used. In addition, the BADC does the initial correction, compaction, and formatting of the data stream, thus significantly reducing the subsequent computational load. For example, about 30,000 constants are stored in the Mark II BADC's that never appear in the analysis program.

A different consequence of this approach is that the need for an effective calibration system can be more serious than in the more traditional, "more digital" approach to instrumentation. For a drift chamber readout, a system that runs off a reasonably controlled digital clock is usually sufficiently accurate so that calibration is unnecessary. For a calorimeter, however, the front end preamplifier gain usually cannot be well enough controlled to avoid calibration, so the question of the performance of the sample and hold circuits versus the use of a high quality ADC on each channel is irrelevant. Calibration also tends to be necessary for high performance time-of-fight systems because of drifts in photomultiplier characteristics. Since it is difficult to avoid calibration systems totally with the "digital approach", the required calibrations seem reasonable.

An additional advantage of the calibration system is that it usually can be a very important part of the testing and maintenance systems, by injecting signals at rates easily visible on an oscilloscope. For Mark II, the drift chamber system is calibrated by coupling a low voltage pulse derived from a Pulse Pair Generator to the high voltage feeds for the field wires. This signal is then capacitively coupled to all of the sense wires by the drift chamber itself. In this way, for example, an open connection between a drift chamber feedthrough and preamplifier is immediately obvious. The liquid argon calorimeter system is calibrated by coupling a voltage step through a measured capacitance directly onto the strips of the calorimeter. The voltage pulse is generated by one precision DAC and pulser, distributed on double shielded twisted pair to each module, and then attenuated by a factor of 100 and distributed to the calibration capacitors for each set of strips. The time-of- flight system is calibrated by light pulses generated by a nitrogen laser and distributed to the center of each counter by fiber optic cables. The precise time of the laser firing is measured by a vacuum photodiode, and the intensity of the pulse going to the counters is controlled by neutral density filters mounted on a remotely controlled wheel. An absolute time scale is determined by switching delay cables into the photodiode signal path.

Calibrations are performed by measuring the system response in raw ADC units from the BADC as a function of the independent variable, then inverting that response function to a form suitable for the BADC data correction and sending those constants to the BADC's. The measurements usually consist of about 50 pulses for each value of the independent variable, and the BADC's are used to calculate the means and variances of the raw data. The VAX then reads in the means and variances, resets the appropriate calibration controllers, and proceeds. The VAX is used to invert the response functions and check that each channel is within reasonable performance limits. The use of the BADC's to reduce the initial data is important in limiting the elapsed time for a calibration. Because of the similar approach, most of the Mark II systems can be calibrated together, in a total time of 10-15 minutes.

2.5 MARK II CAMAC

All major components of the Mark II data acquisition and trigger system are implemented as CAMAC modules. The front end preamplifiers do not adhere to a standard, and the primary trigger and other simple logic uses the NIM standard. The use of a well defined standard, i.e., CAMAC, for the transfer of digital data, is considered essential to the economic success of Mark II.

The Mark II CAMAC system is based on the VAX CAMAC Channel (VCC)[5] to couple several different branch highway systems to the VAX Unibus. This system has gone through much evolution and is now used on about 8 VAX'es at SLAC, including the SPEAR and PEP control systems. The most important warning about this system is that none of the branch highways or associated crate controllers follow the published CAMAC standards, although modification of the VCC to use IA crate controllers would not be difficult.

The system is designed to efficiently transfer data between the host computer and a very large set of CAMAC data acquisition and control modules, as indicated in Figure 10. The VCC is a high speed bit slice microprogrammed processor that couples the Unibus to Branch Drivers residing in System Crates, with each Branch Driver capable of controlling a set of CAMAC crates. The VCC is designed to take its instructions from and use data buffers in VAX main memory, thereby limiting the VAX CPU overhead in CAMAC input-output to setup of the various buffers and passing their addresses to the VCC. A coherent software package is used to integrate the high level language interface, the system driver, and the VCC microcode.

The VCC drives a set of up to 7 system crates using the SLAC Parallel branch Standard. Each system crate may have up to 8 Branch Drivers. The SLAC Parallel Branch Standard may be used with differential cables and Branch Receivers to go long distances, up to a few km, or with single ended cables to go up to 10 m. The parallel branches are used for Mark II, which has a total of about 40 crates and two system crates. The system speed is limited by the Unibus to about 0.7 mbytes/sec. The SLAC Parallel Branch supports up to 7 crates per branch

The VCC and Branch Drivers support subaddress, module, and crate scanning, which can be conditioned by Q and X responses from the modules to easily set up block transfers of data from sets of modules. These features are used to read the Mark II BADC's. Additionally, the VCC can use X and Q to conditionally allow data transfer, or can use lack of X or Q to terminate a particular data transfer. Finally, the VCC can optionally pack 1, 2, or 3 bytes of CAMAC Data into VAX bytes, words, or longwords, respectively. For Mark II, the readout of the entire detector is accomplished by a single command from the VAX CPU to the VCC.

A different Branch Driver and crate controller has recently been developed at SLAC for the SLC control system that may be of interest in new designs. The SLC Serial System connects branch drivers to crate controllers using inexpensive 3-pair cable running a serial protocol at 5 Mbaud. Cable lengths may be up to about 300 m total, and there can be up to 16 crates per branch. For large block transfers, the serial system has about 70% of the speed of the parallel system. The two systems are almost identical to the high level software.

Interrupts (CAMAC LAM's) are handled by a system of System Interrupt Modules (SIM) and Remote Interrupt Modules (RIM) as indicated in Figure 11. This system was developed for Mark II, but is used with most of the VCC's at SLAC. One SIM is used in the first system crate. The SIM is polled by VCC whenever VCC is not transferring data. Up to 7 RIM's may be connected to the SIM by a daisy-chained coaxial line. The RIM's receive LAM signals from the crate controller and also have 6 front panel interrupt inputs. Each interrupt is coded and sent by a serial protocol to the SIM, which will respond to a VCC poll if it has a pending interrupt. The RIM's allow interrupts to be armed and fired via standard CAMAC commands, and the SIM can manage a queue of interrupts. The SIM-RIM system is fully integrated into the VAX software, and can fully support multiple users.

3. Summary

The Mark II data acquisition and trigger system are complementary systems using highly multiplexed analog signal storage data acquisition modules that are read out by a high speed microprocessor controlled ADC in each CAMAC crate. The two level trigger system includes a fast primary trigger so that no delay elements are needed in the data acquisition path, and a track finding secondary trigger to reduce the event rate to about 1 Hz. The overall system deadtime is $\lesssim 10\%$.

4. Acknowledgements

The Mark II data acquisition and trigger system is the result of the dedicated efforts and hard work of many people. Particular credit goes to the SLAC Electronic Instrumentation Group led by R. S. Larsen, and to D. J. Nelson and J. E. Grund of SLAC Group C. Other important contributions have been made by: H. Brafman, E. L. Cisneros, E. Frank, C. D. Granieri, H. K. Kang, J. N. Hall, T. Himel, R. Hettel, D. Horelick, R. Melen, J. F. Patrick, L. J. Weaver. The contributions from all of the Mark II physicists and technicians were vital to the invention and evolution of the system.

DISCLAIMER

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5. D. J. Nelson et.al., IEEE Trans Nucl. Sci. NS-28, No.1, 336 (1981).
6. H. Brafmann et.al., IEEE Tras. Nucl. Sci. NS-25, No.1, 692 (1978). T. Himel, Thesis SLAC Report No.223 (1979).

Figure Captions

1. Schematic of the MK-II Detector.
2. Block Diagram of Time to Amplitude Convertor (TAC).
3. Block Diagram of Sample and Hold Analog Module (SHAM).
4. Block Diagram of Time of Flight Discriminator Module (DISCO).
5. Block Diagram of Data Acquisition System.
6. Track Finding Principle.
7. Typical Set of Drift Chamber Roads.
8. Simplified Block Diagram of Shift Registers and One Curvature Module.
9. Trigger System Block Diagram.
10. CAMAC System Block Diagram.
11. CAMAC Interrupt System Block Diagram.

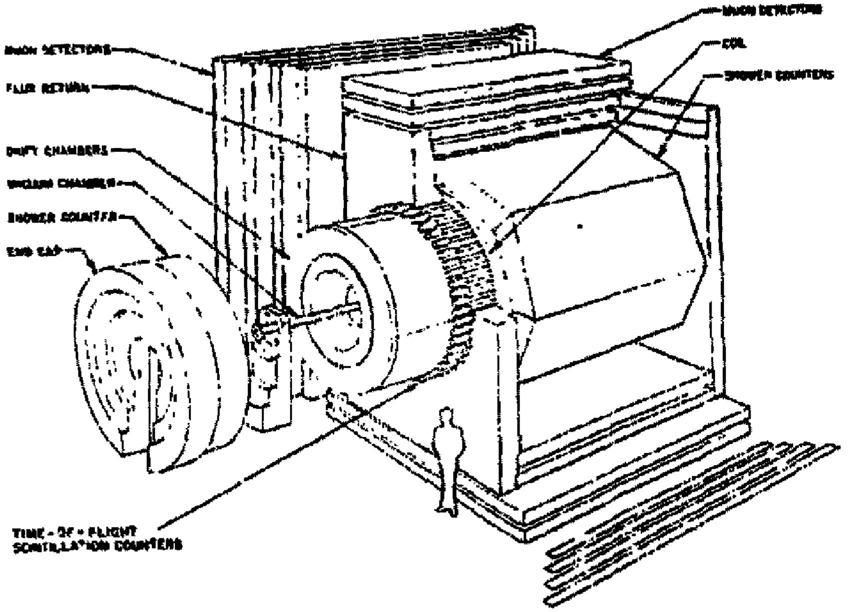
MUON DETECTORS
FLUX RETURN
DRIFT CHAMBERS
VACUUM CHAMBER
SHOWER COUNTER
END CAP
TIME - OF - FLIGHT
SCINTILLATION COUNTERS
MUON DETECTORS
COIL
SHOWER COUNTERS
3499A32
4 74

Fig. 1

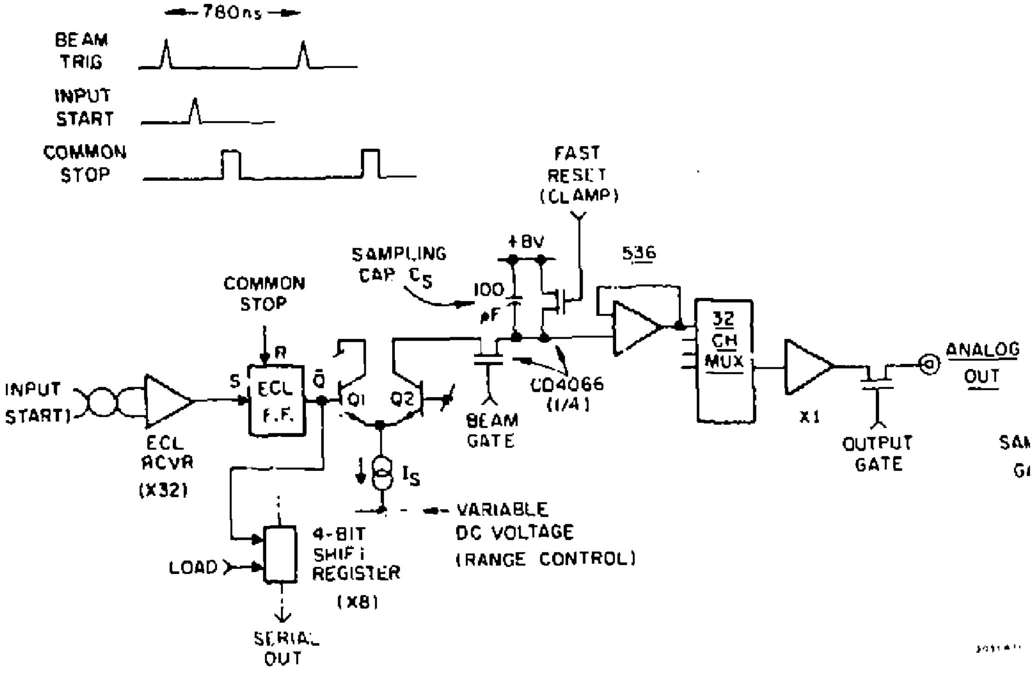
780ns
BEAM TRIG
INPUT START
COMMON STOP
FAST RESET (CLAMP)
+8V
SAMPLING CAP C_S
100 pF
536
COMMON STOP
R
S
ECL F.F.
$\bar{Q}$
Q1
Q2
INPUT START)
ECL RCVR (X32)
BEAM GATE
CD4066 (1/4)
32 CH MUX
X1
ANALOG OUT
OUTPUT GATE
I_S
VARIABLE DC VOLTAGE (RANGE CONTROL)
4-BIT SHIFT REGISTER (X8)
LOAD
SERIAL OUT

Fig. 2

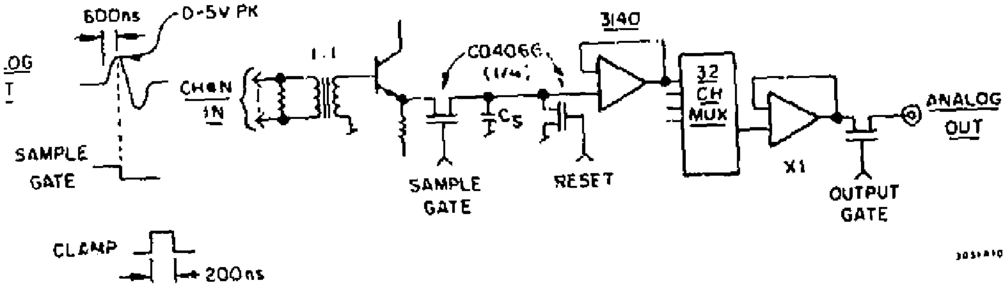
600ns
0-5V PK
.OG
T
SAMPLE
GATE
CLAMP
200ns
CH#N
IN
1:1
CD4066
(1/4)
C_S
SAMPLE
GATE
RESET
3140
32
CH
MUX
X1
OUTPUT
GATE
ANALOG
OUT

Fig. 3

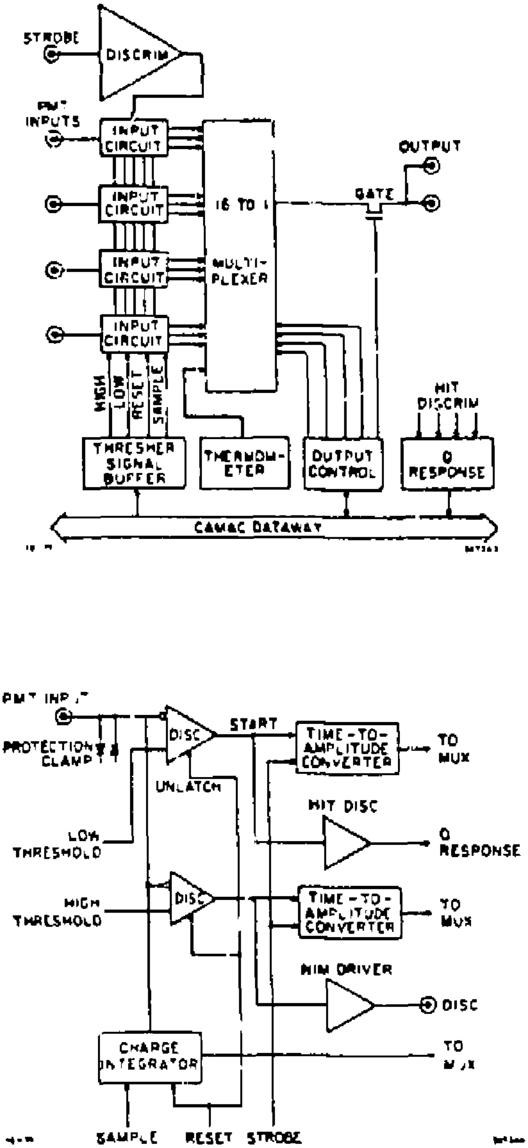
STROBE
DISCRIM
PMT INPUTS
INPUT CIRCUIT
INPUT CIRCUIT
INPUT CIRCUIT
INPUT CIRCUIT
16 TO 1 MULTI-PLEXER
GATE
OUTPUT
HIGH
LOW
RESET
SAMPLE
THRESHER SIGNAL BUFFER
THERMOM-ETER
OUTPUT CONTROL
HIT DISCRIM
Q RESPONSE
CAMAC DATAWAY
PMT INPUT
PROTECTION CLAMP
DISC
START
TIME-TO-AMPLITUDE CONVERTER
TO MUX
UNLATCH
HIT DISC
Q RESPONSE
LOW THRESHOLD
HIGH THRESHOLD
DISC
TIME-TO-AMPLITUDE CONVERTER
TO MUX
NIM DRIVER
DISC
CHARGE INTEGRATOR
TO MUX
SAMPLE
RESET
STROBE

Fig. 4

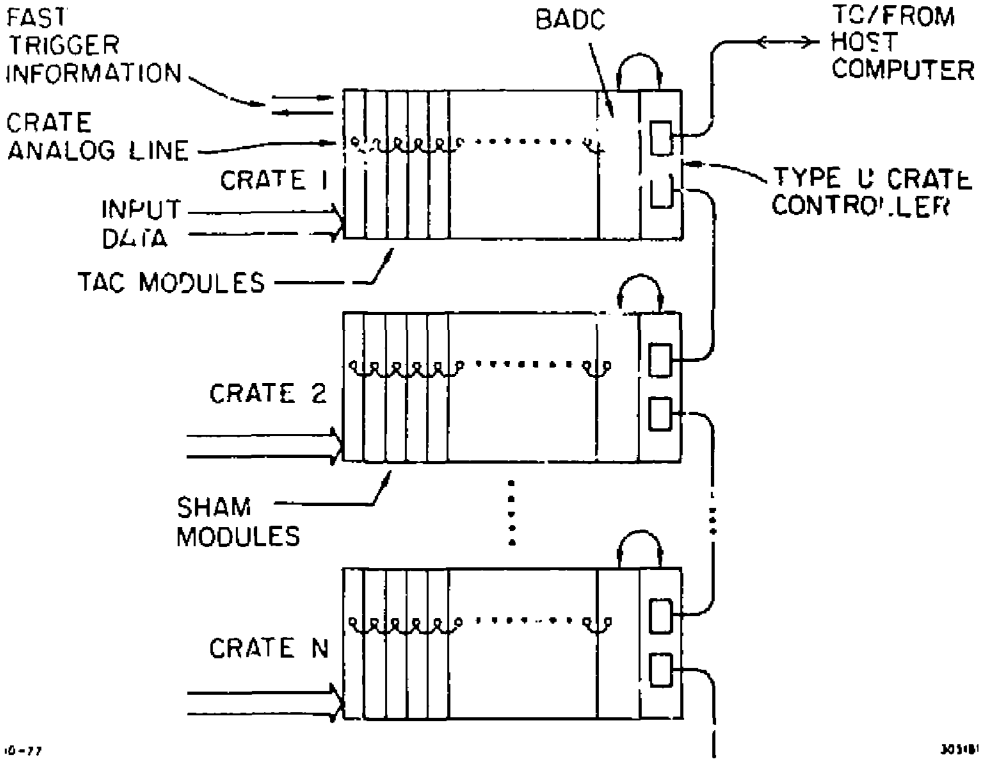
FAST TRIGGER INFORMATION
CRATE ANALOG LINE
CRATE 1
INPUT DATA
TAC MODULES
BADC
TO/FROM HOST COMPUTER
TYPE U CRATE CONTROLLER
CRATE 2
SHAM MODULES
CRATE N
10-77
3031B1

Fig. 5

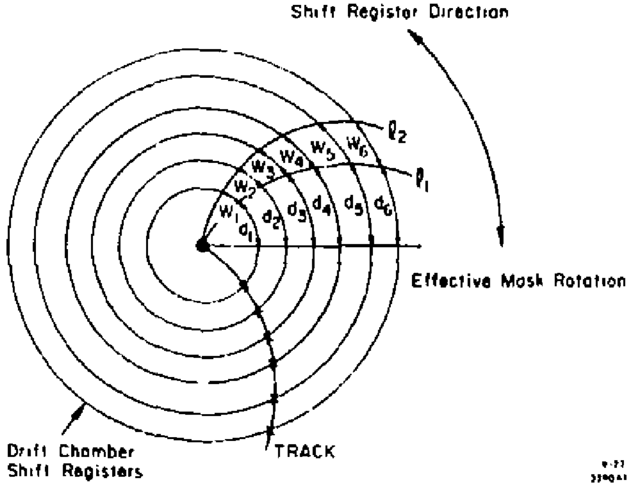
Shift Register Direction
ℓ_2
ℓ_1
W_1
W_2
W_3
W_4
W_5
W_6
d_1
d_2
d_3
d_4
d_5
d_6
Effective Mask Rotation
Drift Chamber
Shift Registers
TRACK

Fig. 6

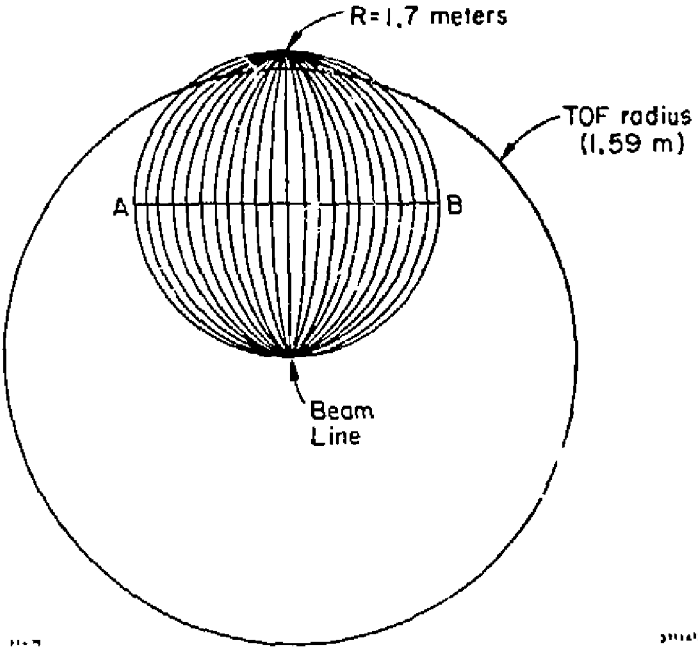

Fig. 7

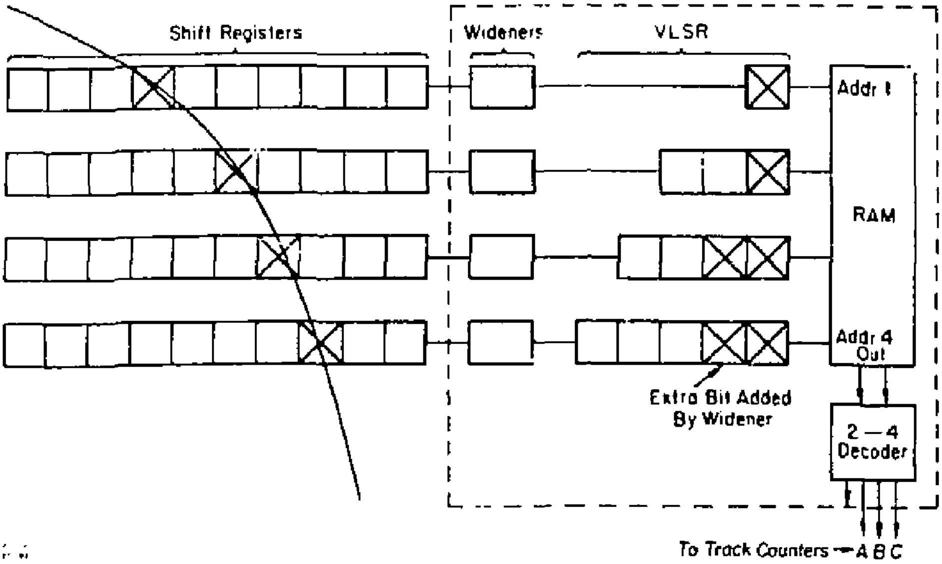
Shift Registers
Wideners
VLSR
Addr 1
RAM
Addr 4
Out
Extra Bit Added
By Widener
2 — 4
Decoder
To Track Counters
A B C

Fig. 8

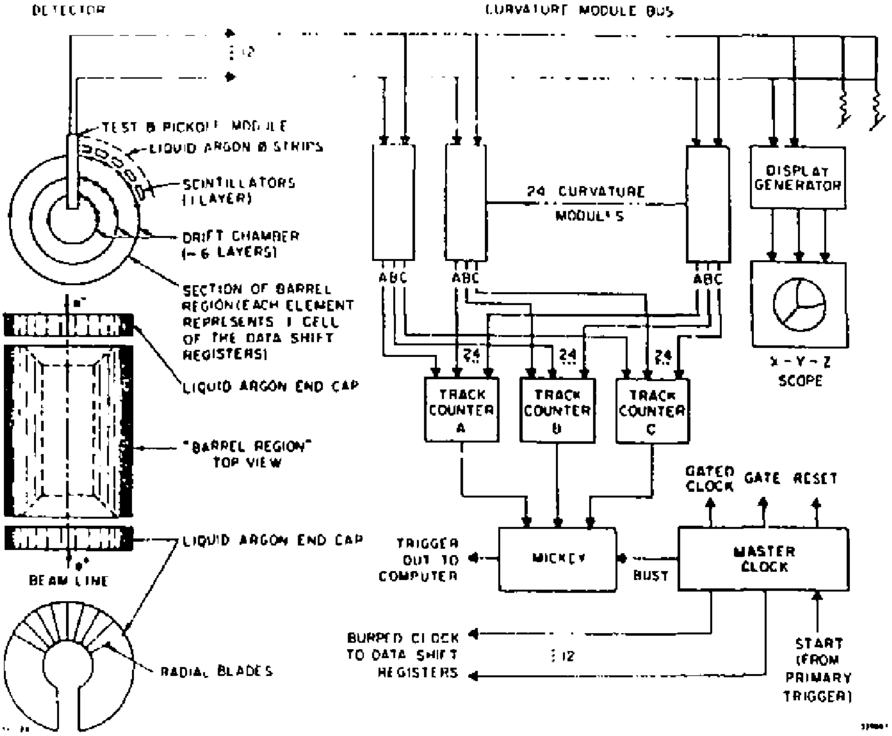
DETECTOR
CURVATURE MODULE BUS
12
TEST θ PICKOFF MODULE
LIQUID ARGON θ STRIPS
SCINTILLATORS (1 LAYER)
DRIFT CHAMBER (~6 LAYERS)
SECTION OF BARREL REGION (EACH ELEMENT REPRESENTS 1 CELL OF THE DATA SHIFT REGISTERS)
e-
LIQUID ARGON END CAP
"BARREL REGION" TOP VIEW
LIQUID ARGON END CAP
e+
BEAM LINE
RADIAL BLADES
24 CURVATURE MODULES
DISPLAY GENERATOR
ABC
ABC
ABC
X - Y - Z SCOPE
24
24
24
TRACK COUNTER A
TRACK COUNTER B
TRACK COUNTER C
GATED CLOCK
GATE
RESET
TRIGGER OUT TO COMPUTER
MICKEY
BUST
MASTER CLOCK
BURPED CLOCK TO DATA SHIFT REGISTERS
12
START (FROM PRIMARY TRIGGER)

Fig. 9

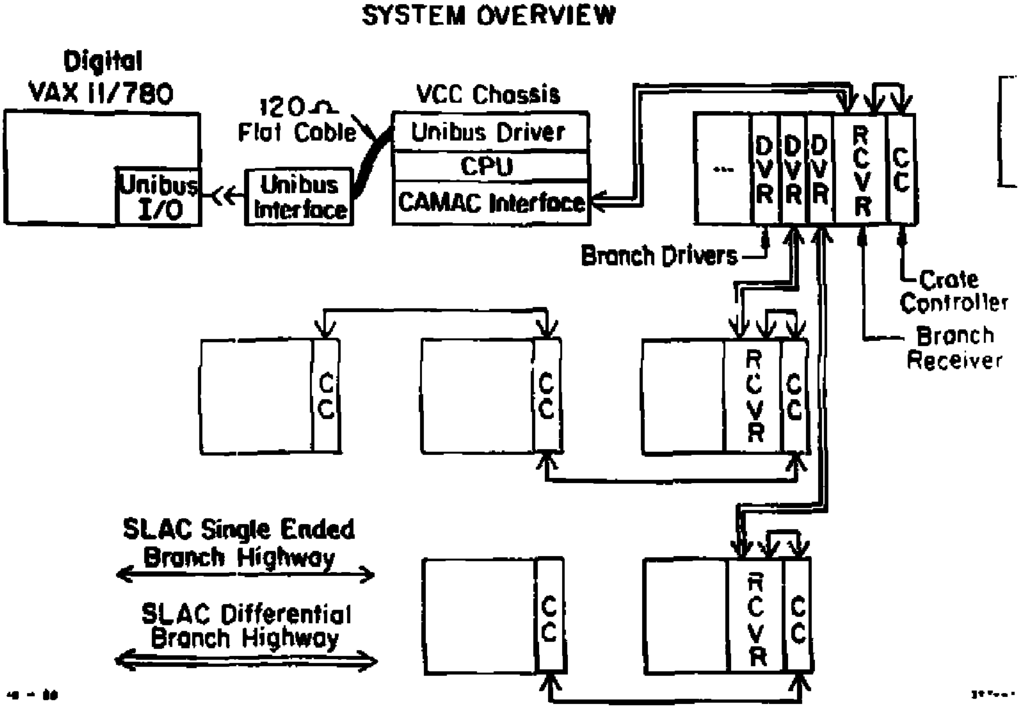
SYSTEM OVERVIEW

Fig. 10

SYSTEM OVERVIEW
WITH INTERRUPTS

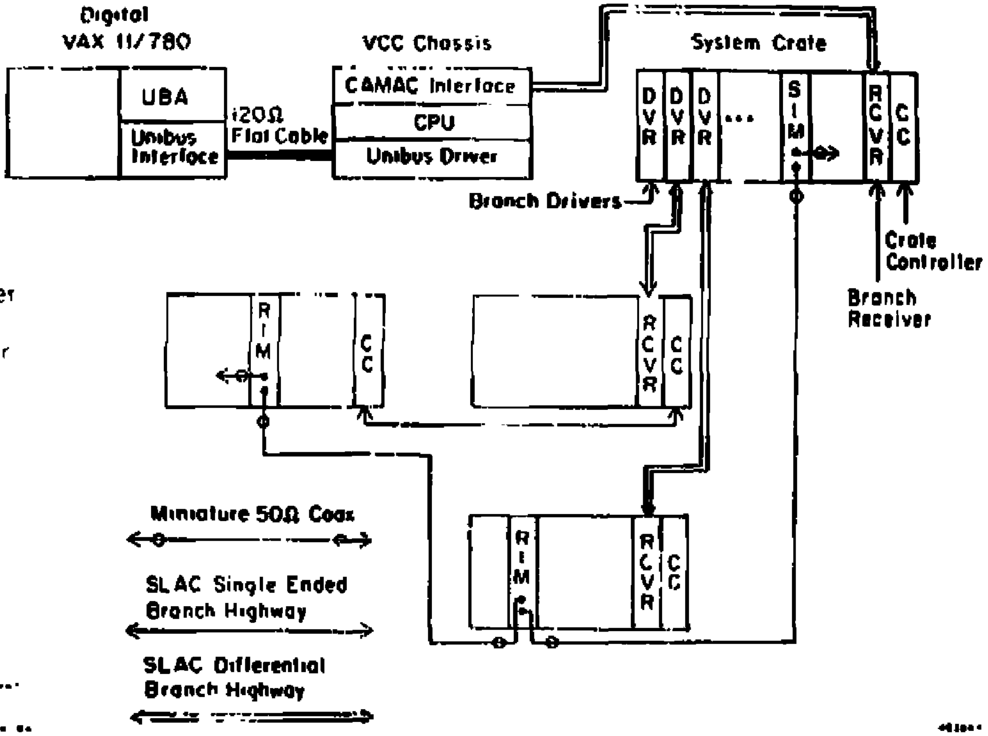

Fig. 11