(12) UK Patent Application (19) GB (11) 2 131 748 A

(21) Application No 8235658
(22) Date of filing 15 Dec 1982
(43) Application published
27 Jun 1984
(51) INT CL³
C30B 33/00
(52) Domestic classification
B6J 703 MA1
U1S 2061 B6J
(56) Documents cited
GB 1544613
(58) Field of search
B6J
(71) Applicant
The Secretary of State for Defence
(United Kingdom),
Whitehall, London
SW1A 2HB
(72) Inventors
Derek Joseph Day,
John Charles White
(74) Agent and/or Address for Service
J. B. Edwards,
Procurement Executive,
Ministry of Defence,
Patents 1A4, Room 2014,
Empress State Building,
Lillie Road, London
SW6 1TR

(54) Silicon etch process

(57) A silicon etch process wherein an area of silicon crystal surface is passivated by radiation damage and non-planar structure produced by subsequent anisotropic etching. The surface may be passivated by exposure to an energetic particle flux — for example an ion beam from an arsenic, boron, phosphorus, silicon or hydrogen source, or an electron beam. Radiation damage may be used for pattern definition and/or as an etch stop. Ethylenediamine pyrocatechol or aqueous potassium hydroxide anisotropic etchants may be used. The radiation damage may be removed after etching by thermal annealing.

GB 2 131 748 A

2131748

Fig.1.

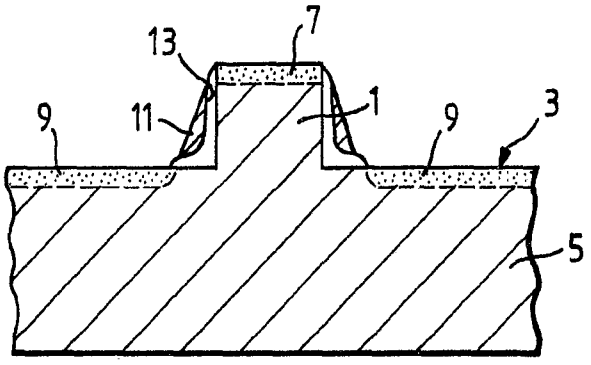


Fig.2.

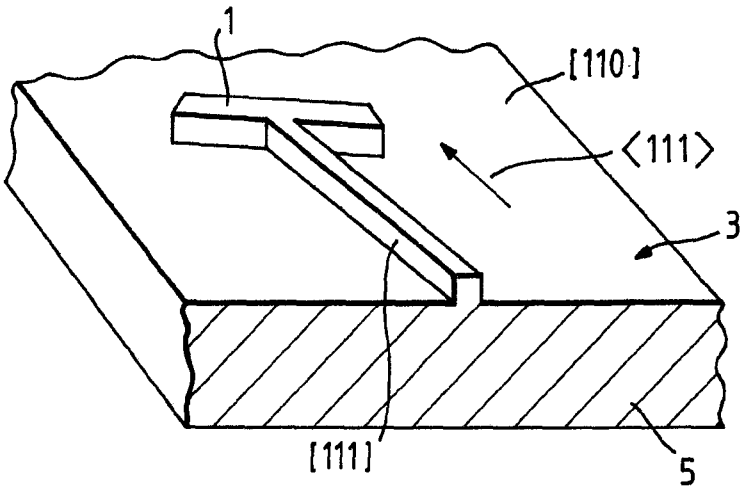


Fig.3.

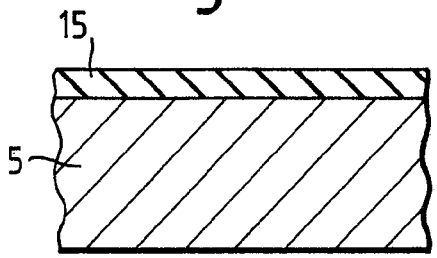


Fig.4.

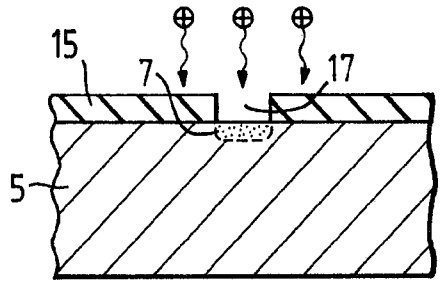


Fig.5.

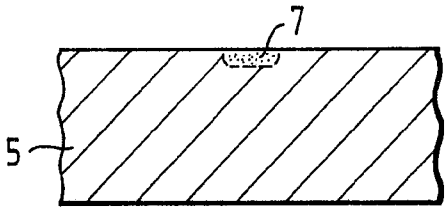
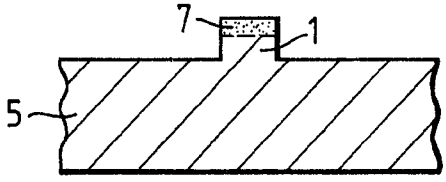


Fig.6.



SPECIFICATION

Silicon etch process

Technical Field

This invention concerns a silicon etch process, more particularly an etch process applied to silicon crystal material to produce non-planar structures — for example mesas or grooves. In this process, an area of the silicon crystal surface is protected and the crystal is exposed to an etchant; the etchant attacks the unprotected area of the silicon surface and removes silicon material to produce a non-planar structure.

Background Art

It is common practice to use an etch resistant mask — for example one of the photoresist material — to protect areas of the silicon surface during the etch process. Great care must be taken to ensure the proper definition, alignment, and registration of this mask. The finer the degree of tolerance on structure dimensions, the more critical is the accuracy of alignment and the more difficult this task.

Anisotropic or preferential etching of different crystal planes in silicon has been exploited widely for micro-engineering of mechanical and electronic structures. (See for example:— Proc IEEE *70*, 420 (1982); IEEE Trans on Electron Devices ED.25, 1185 (1978); and UK Patent Application No 8125375.) Conventional masking techniques employing etch resistant materials are used to define an etched surface with edges aligned to planes of lower etch rate. By suitable choice of crystal orientation and mask shape, fine geometries of grooves, holes and points can be obtained.

Etches have also been found that are selective to doping level, allowing highly doped layers to be used as etch stops to obtain depth discrimination. (See J Electrochem Soc *129*, 2051, 1982.)

Hitherto, the combination of surface masking and etch stop layers have been fundamental to technologies exploiting anisotropic etchants.

Disclosure of the Invention

For crystal specimen examination, it has been common practice to decorate the specimen surface using an etchant. Damage regions of the crystal lattice are in general vulnerable to etch attack, and when a crystal specimen is exposed to an isotropic etchant the damaged regions are etched away in preference to other regions. Damage is highlighted by etch pitting in the specimen surface. It is surprising, then, as has been found here, that quite the reverse effect is found when damaged silicon is exposed to an anisotropic etchant. Regions of crystal damage actually appear relatively resistant to anisotropic etch attack and crystal damage may thus be used to protect areas of a silicon crystal surface during etch process structure definition.

In accordance with this invention, there is provided a silicon etch process wherein an area of the plane surface of a silicon crystal is exposed to a flux of energetic particle radiation to thereby introduce crystal damage sufficient to passivate said exposed area, the edges of said area lying in planes of relatively low etch rate; and, thereafter, the silicon crystal is exposed to an anisotropic etchant to remove silicon material adjacent to the passivated area.

This process may thus be used for maskless etch, self-aligned, pattern definition. Alternatively, or in conjunction therewith, the damaged region of silicon crystal may be buried, for example by an intermediate step of epitaxial layer deposition, to serve then, as an etch stop during subsequent anisotropic etching. The invention thus facilitates a simple technology that is self-aligned and/or self limiting in the realisation of surface defined patterns as etch structures.

The radiation damage may be produced by means of an ion beam (I-Beam). For example, the said exposed area may be first delineated using a photolithographically patterned photoresist mask or other mask and exposing the crystal surface through this mask to a flux of energetic ions. These ions may be a dopant species — for example: arsenic (As^+); boron (B^+); or, phosphorus (P^+); or protons (H^+), or may be of silicon itself (Si^+).

Alternatively, the radiation damage may be produced by an energetic electron beam (e-Beam). The exposed area in this case could be defined by electron beam scan control, or again by mask definition.

Suitable anisotropic etchants are solutions of ethylenediamine pyrocatechol, and of potassium hydroxide.

The above process is applicable to VMOS device fabrication. Selecting the [100] plane as crystal surface, and 111 edge directions, the process may be applied to produce V-grooves and/or sloped side mesas.

The process is also applicable to UMOS device fabrication. Selecting the [110] plane as crystal surface, and 111 edge directions, the process may be applied to produce steep-walled grooves and/or vertical side mesas.

Brief Introduction of the Drawings

In the drawings accompanying this specification:—

Figure 1 is a schematic cross-section in the vertical plane of a vertical channel metal-oxide-semiconductor silicon transistor, illustrating a mesa structure produced using an anisotropic etchant;

Figure 2 is a perspective view of the mesa structure illustrated in the preceding figure; and,

Figures 3 to 6 are schematic cross-sections showing stages in the definition of this mesa structure.

Description of the Embodiments

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings.

There is shown in Figures 1 and 2 a steep-

walled mesa 1, a structure extending vertically from the [110] plane surface 3 of a single crystal silicon substrate 5. The upper surface of the mesa 1 has been implanted with arsenic dopant to produce the drain region 7 of the transistor. A dopant species has also been implanted in regions of the substrate 5 each side of the mesa, source implant regions 9. A gate electrode 11 is spaced from the side surfaces of the mesa 1 by a thin insulating layer 13 of oxide. Drain and source electrodes are also provided adjacent to the drain and source regions 7 and 9 (not shown). The sides of the mesa 1 are substantially vertical and the edges of the mesa 1 are aligned in the 111 crystal directions.

The initial steps in the process of fabricating this transistor are illustrated in Figures 3 to 6. In the course of this process a layer 15 of photoresist is spun on to the [110] plane surface of a prepared silicon crystal substrate 5 (Figure 3). The surface pattern of the mesa structure is then defined in the photoresist photographically and soluble photoresist removed, leaving a window 17 in the photoresist mask layer 15, a window having the pattern of the desired mesa surface. The silicon substrate 5 is then exposed to a flux of energetic ions from an arsenic source and the drain implant region 7 is formed (Figure 4). Ion radiation at 80 keV and dose producing a dopant ion density of 10^{15} ions cm^{-2} is found sufficient to produce adequate lattice damage to passivate the exposed surface of the silicon substrate 5. The remanent photoresist mask material 15 is then removed and the substrate exposed to an anisotropic etchant (Figure 5). The following etchants have each proved satisfactory:—

(i) Ethylenediamine pyrocatechol etchant:
500 ml Ethylenediamine
80 gm Pyrocatechol
67 ml water
3 gm pyrozine

(ii) Potassium hydroxide solution etchant:—
250 gm potassium hydroxide
800 ml water
250 ml propan-1-ol

After a period of time the etch process is halted. The mesa structure Figure 5 is thus obtained. Here the step height of the mesa 1 is determined by the etch time. However in preference to this, the etch may be halted by means of an etch stop incorporated at a predetermined depth beneath the silicon surface. For example, an epitaxial layer, produced by molecular beam epitaxy (MBE) or by chemical vapour deposition (CVD), of the required depth, may be grown on an implanted or ion cleaned surface. The latter treated surface serves as a buried etch stop.

The crystal damage produced during implantation is removed, and the dopant ion species are rendered electrically active, by thermal annealing following subsequent stages of the device fabrication.

Similar satisfactory results have also been obtained using boron, phosphorus, silicon and hydrogen ion sources. In these examples the ion density produced in the silicon was between 10^{14} and 10^{15} ions/cm^2. Penetration was to a depth of a few thousand Angstroms.

Maskless processing has also been performed employing electron beam lithography. It has been found at 25 keV and using beam currents in excess of 50 nA that patterns can be written directly on to the silicon surface, patterns that cause passivation to anisotropic etching.

CLAIM

A silicon etch process wherein an area of the plane surface of a silicon crystal is exposed to a flux of energetic particle radiation to thereby introduce crystal damage sufficient to passivate said exposed area, the edges of said area lying in planes of relatively low etch rate; and, thereafter, the silicon crystal is exposed to an anisotropic etchant to remove silicon material adjacent to the passivated area.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1984. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.