(12) UK Patent Application (19) GB (11) 2 137 806 A

(43) Application published 10 Oct 1984

(21) Application No 8309125

(22) Date of filing 5 Apr 1983

(51) INT CL[3]
H01L 21/425

(52) Domestic classification
H1K 1CB 2R3A 2S10 2S1D 2S20 2S2D 3E1M 3E5A 3E5CY 3F 9D1 9R2 LCA

(56) Documents cited
GB 1601070 GB 1401276
GB 1463121 GB 1294516

(58) Field of search
H1K

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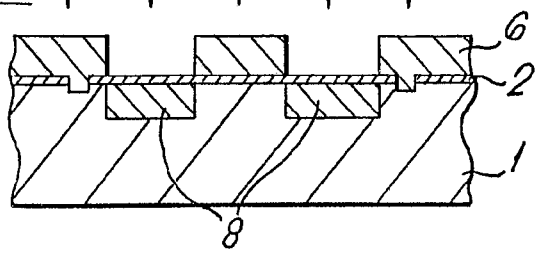
(54) Ion implantation in semiconductor bodies

(57) Ions are selectively implanted into layers (8) of a semiconductor substrate (1) of, for example, semi-insulating gallium arsenide via a photoresist implantation mask (6) and a metallic layer (2) of, for example, titanium disposed between the substrate surface and the photoresist mask (6). After implantation the mask (6) and metallic layer (2) are removed and the substrate heat treated for annealing purposes. The metallic layer (2) acts as a buffer layer and prevents possible contamination of the substrate surface, by photoresist residues, at the annealing stage. Such contamination would adversely affect the electrical properties of the substrate surface, particularly gallium arsenide substrates.

Fig.2.



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The drawing originally filed was informal and the print here reproduced is taken from a later filed formal copy.

Fig.1.

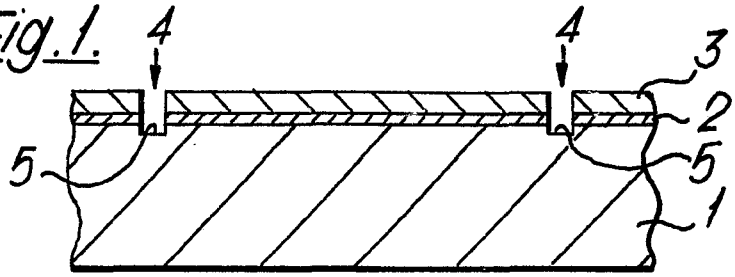


Fig.2.

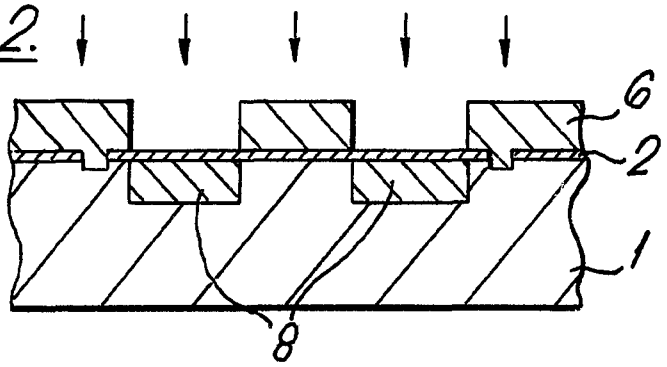


Fig.3.

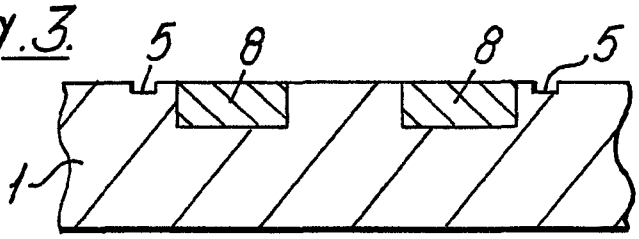


Fig.4.

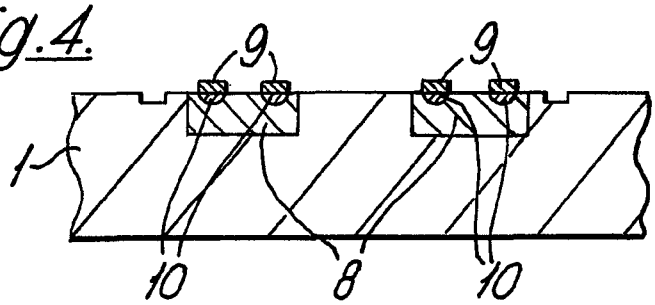
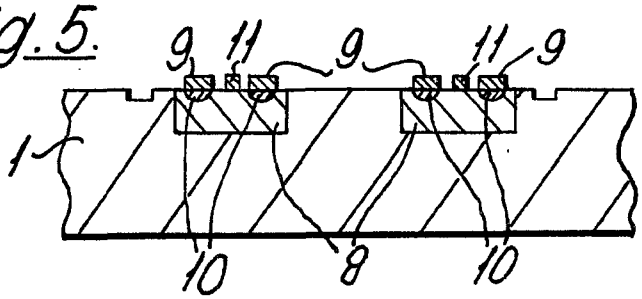


Fig.5.



SPECIFICATION

Semiconductor processing

This invention relates to semiconductor processing and in particular to ion implantation techniques.

According to the present invention there is provided a process for implanting ions into a semiconductor substrate comprising the steps of depositing a metallic layer on a surface of the substrate, providing a photoresist implantation mask on the metallic layer, and bombarding the substrate with ions whereby ions become selectively implanted into regions of the substrate via corresponding windows of the mask and the metallic layer.

Embodiments of the present invention will now be described with reference to the accompanying drawings, in which Figs. 1 to 5 show successive stages in the fabrication of discrete field effect transistors.

The drawings illustrate the fabrication of field effect transistors, i.e. a semi-insulating gallium arsenide substrate 1. The active regions required for the transistors are achieved by ion implantation. A thin titanium layer 2 (approximately 400Å thick) is evaporated onto a surface of the substrate (Fig. 1). A layer 3 of a positive photoresist is spun onto the titanium layer 2. Small windows 4 are opened in the photoresist layer 3 and through these windows 4 registration marks 5 are etched in the gallium arsenide surface. The layer 3 is removed and a fresh layer 6 (Fig. 2) of a positive photoresist applied. Large windows 7 are opened in the photoresist layer 6, thus defining a photoresist implantation mask.

The photoresist masked surface of the gallium arsenide substrate 1 is then subjected to bombardment with, for example, si^{29} ions, as indicated by the arrows, which are thus selectively implanted through the titanium layer 2 into regions of the substrate in order to provide conductive, in this case n-type, regions 8.

The photoresist layer 6 is removed by a suitable solvent and the titanium layer is removed by etching with HF thus achieving the selectively doped gallium arsenide structure shown in Fig. 3. In order to remove implantation induced damage of the structure it is subjected to a heat treatment at approximately 850°C by means, for example, of a capless annealing technique, that is a heat treatment without the provision of a layer on top of the GaAs substrate, thus the structure as shown in Fig. 3 is heat treated.

Source and drain electrodes 9 and regions 10 are then provided (Fig. 4). This may be achieved by means of metallisation lift-off process comprising applying a relatively thick photoresist layer to the annealed substrate; providing windows in the photoresist layer corresponding to the required source and drain electrodes and regions; metallising the photoresist layer and the regions 8 where exposed by the windows with an electrode/dopant metal such as a gold/germanium/nickel alloy, the photoresist is relatively thick in comparison with the alloy layer to ensure that the alloy layer breaks at the edges of the windows; stripping off the photoresist layer together with the surplus metal, leaving the metal electrodes 9 disposed on the regions 8; and heating the assembly to a sufficient temperature to diffuse the germanium from the metal electrodes 9 into the region 8, thus providing source and drain regions 10 with a high doping level, in this case n^+, in the regions 8.

Using a similar metallisation lift-off process, this time employing a Schottky metal, for example chromium/gold, a Schottky barrier gate electrode 11 is disposed between the source and drain electrodes 9 of each transistor. Finally the thus produced assembly is divided into individual devices or circuits which are then contacted or packaged.

The thin layer of titanium acts as a buffer layer between the photoresist and the gallium arsenide surface, and prevents any possible contamination of the gallium arsenide surface, which may result from photoresist residues when such a buffer layer is not used. Such residues are particularly undesirable when employing ion implantation techniques since the substrate must be subjected to heat treatment, the annealing process, after ion implantation and the surface of the substrate, if the photoresist is not fully cleaned off, will become contaminated and the electrical properties of the wafer will be adversely affected. These residues are particularly encountered with gallium arsenide substrates since it is not possible to clean photoresist from a surface thereof particularly rigorously without adversely affecting the surface.

Whereas the invention has basically been described with respect to discrete devices it is also applicable to the fabrication of integrated circuits on gallium arsenide substrates. Whereas only a titanium buffer layer has been described above other metallic layers of, for example, tin, chromium, aluminium, manganese magnesium or indium, may be similarly employed. Such metallic layers, and any photoresist residues therein, can be simply and effectively removed by HF or HCL etching, for example, without damaging the substrate surface. Whereas the semiconductor body into which ions are implanted has been specifically described as gallium arsenide, other semiconductors for example other compound semiconductors or silicon may be similarly processed. It is possible to merely use a patterned photoresist layer for the selective ion implantation of silicon, since the latter can be subjected to a very rigorous cleaning process, to ensure that no photoresist residues remain before annealing, without adversely affecting the surface of the silicon. However in certain instances it may be preferable to use the metallic buffer layer described above.

CLAIMS

1. A process for implanting ions into a semiconductor substrate comprising the steps of

depositing a metallic layer on a surface of the substrate, providing a photoresist implantation mask on the metallic layer, and bombarding the substrate with ions whereby ions become selectively implanted into regions of the substrate via corresponding windows of the mask and the metallic layer.

2. A process as claimed in claim 1, further including the steps of removing the photoresist mask and the metallic layer and heat treating the ion-implanted substrate whereby to remove implantation induced damage.

3. A process as claimed in claim 1 or claim 2, wherein the substrate is of gallium arsenide.

4. A process as claimed in any one of the preceding claims wherein the metallic layer is of titanium.

5. A method of manufacturing a field-effect transistor including the steps of selectively implanting ions into a region of a semi-insulating gallium arsenide substrate by a process as claimed in claim 1 whereby to cause the region to have one conductivity type, forming spaced apart source and drain electrodes of an electrode/dopant metal on the surface of the region, alloying the electrodes whereby to diffuse the dopant into the region to provide source and drain regions of the one conductivity type, but with a higher doping level, and forming a gate electrode on the surface of the region between the source and drain electrodes.

6. A method as claimed in claim 5, wherein the electrode/dopant metal comprises a gold/germanium/nickel alloy.

7. A method as claimed in claim 5 or claim 6, wherein the gate electrode is formed of a Schottky metal.

8. A method as claimed in claim 7, wherein the Schottky metal electrode comprises chromium/gold.

9. A selective ion implantation process substantially as herein described with reference to the accompanying drawings.

10. A semiconductor device made by a process or method according to any one of the preceding claims.

Printed in the United Kingdom for Her Majesty's Stationery Office, Demand No. 8818935, 10/1984. Contractor's Code No. 6378.
Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.