

30  
1-71-85 JS (1)

**NOTICE**  
**PORTIONS OF THIS REPORT ARE ILLUSTRATIVE.**  
It has been reproduced from the best available copy to permit the broadest possible availability.

### THE VERNIER DELAY UNIT

W. B. Pierce  
Stanford Linear Accelerator Center  
Stanford University  
Stanford, California 94305

DE85 004678

CONF-84/007--43

MASTER

#### Abstract

This module will accept differential ECL pulses from the auxiliary rear panel or NIM level pulses from the front panel. The pulses are produced at the output with a fixed delay that is software programmable in steps of 0.1 ns over the range of 0.1 to 10.5 ns. Multiple outputs are available at the front panel. Minimum delay through the module is 0 ns.

#### Introduction

One of the most critical timing specifications for the SLC machine occurs at the injector and ejector magnets for the Damping Ring. It has been determined that the trigger pulses to the magnets must be controlled to 0.1 ns. The primary source for all trigger pulses for the SLC machine is the Programmable Delay Unit (PDU). The PDU generates a 67.2 ns wide pulse with delay increments of 8.7 ns. The gap between the required accuracy and that available from the PDU requires the design of a new module that is called the Vernier Delay Unit (VDU). This module accepts the 67.2 ns pulse from the PDU and is capable of increasing the delay in steps of 0.1 ns from 0 to 10.7 ns plus the minimum 9 ns delay.

The module has two totally independent channels. The pulse input to the module is software selectable from either the auxiliary backplane or a front panel Lemo connector. The auxiliary backplane pulses are to be the 67 ns differential ECL pulses from the PDU. The front panel input is to be a NIM level (-0.7 V 50  $\Omega$  termination).

With the exception of the Pos 5 V signal, all output pulse widths will track the input pulse widths. The following outputs are available on the front panel:

- 1. Differential ECL
- 2. NIM level
- 3. Pos 5 V, 500 ns wide pulse

The delays for the two channels are independently software programmable over the range of 0 to 10.7 ns. The delay is achieved by utilizing the PECLDL Programmable Delay Lines that are available from Engineered Components Company of San Luis Obispo, California. Two units were used per channel: the PECLDL 2.8-0.1 and the PECLDL 2.8-0.6.

These delay lines are connected in series, and both are 4 bit programmable. The 2.8-0.6 model produces stepped delays in increments of 0.6 ns from 0 to 9.0 ns. The model 2.8-0.1 has increments of 0.1 ns and is programmable from 0 to 1.5 ns. Each unit presents a minimum of 2.8 ns delay. Added to this 5.6 ns delay is the VDU internal delay of approximately 3 ns, giving a minimum delay of approximately 9 ns. For all of the testing and calibration, this fixed delay is measured by programming 0 delay to the module and measuring the delay between input and output pulse. All subsequent delay measurements made during calibration and testing were corrected to present incremental delays that do not include this fixed value.

The two programmable delays in series [0.6 ns and 0.1 ns] will have the condition that some delays which are to be requested could be requested by several different programs. For example: If we wish to request a delay of 1.5 ns, there are three possible choices:

0.6 Program	0.1 Program	Total Delay
1. 2 = 12	3 = 03	= 1.5 ns
2. 1 = 06	9 = 09	= 1.5 ns
3. 0 = 0	15 = 15	= 1.5 ns

Output 11 from Channel 1	Delay (ns)	Output 12 from Channel 2	Delay (ns)
00000	0.000	00000	0.000
00001	0.030	00001	0.030
00002	0.060	00002	0.060
00003	0.090	00003	0.090
00004	0.120	00004	0.120
00005	0.150	00005	0.150
00006	0.180	00006	0.180
00007	0.210	00007	0.210
00008	0.240	00008	0.240
00009	0.270	00009	0.270
00010	0.300	00010	0.300
00011	0.330	00011	0.330
00012	0.360	00012	0.360
00013	0.390	00013	0.390
00014	0.420	00014	0.420
00015	0.450	00015	0.450
00016	0.480	00016	0.480
00017	0.510	00017	0.510
00018	0.540	00018	0.540
00019	0.570	00019	0.570
00020	0.600	00020	0.600
00021	0.630	00021	0.630
00022	0.660	00022	0.660
00023	0.690	00023	0.690
00024	0.720	00024	0.720
00025	0.750	00025	0.750
00026	0.780	00026	0.780
00027	0.810	00027	0.810
00028	0.840	00028	0.840
00029	0.870	00029	0.870
00030	0.900	00030	0.900
00031	0.930	00031	0.930
00032	0.960	00032	0.960
00033	0.990	00033	0.990
00034	1.020	00034	1.020
00035	1.050	00035	1.050
00036	1.080	00036	1.080
00037	1.110	00037	1.110
00038	1.140	00038	1.140
00039	1.170	00039	1.170
00040	1.200	00040	1.200
00041	1.230	00041	1.230
00042	1.260	00042	1.260
00043	1.290	00043	1.290
00044	1.320	00044	1.320
00045	1.350	00045	1.350
00046	1.380	00046	1.380
00047	1.410	00047	1.410
00048	1.440	00048	1.440
00049	1.470	00049	1.470
00050	1.500	00050	1.500
00051	1.530	00051	1.530
00052	1.560	00052	1.560
00053	1.590	00053	1.590
00054	1.620	00054	1.620
00055	1.650	00055	1.650
00056	1.680	00056	1.680
00057	1.710	00057	1.710
00058	1.740	00058	1.740
00059	1.770	00059	1.770
00060	1.800	00060	1.800
00061	1.830	00061	1.830
00062	1.860	00062	1.860
00063	1.890	00063	1.890
00064	1.920	00064	1.920
00065	1.950	00065	1.950
00066	1.980	00066	1.980
00067	2.010	00067	2.010
00068	2.040	00068	2.040
00069	2.070	00069	2.070
00070	2.100	00070	2.100
00071	2.130	00071	2.130
00072	2.160	00072	2.160
00073	2.190	00073	2.190
00074	2.220	00074	2.220
00075	2.250	00075	2.250
00076	2.280	00076	2.280
00077	2.310	00077	2.310
00078	2.340	00078	2.340
00079	2.370	00079	2.370
00080	2.400	00080	2.400
00081	2.430	00081	2.430
00082	2.460	00082	2.460
00083	2.490	00083	2.490
00084	2.520	00084	2.520
00085	2.550	00085	2.550
00086	2.580	00086	2.580
00087	2.610	00087	2.610
00088	2.640	00088	2.640
00089	2.670	00089	2.670
00090	2.700	00090	2.700
00091	2.730	00091	2.730
00092	2.760	00092	2.760
00093	2.790	00093	2.790
00094	2.820	00094	2.820
00095	2.850	00095	2.850
00096	2.880	00096	2.880
00097	2.910	00097	2.910
00098	2.940	00098	2.940
00099	2.970	00099	2.970
00100	3.000	00100	3.000
00101	3.030	00101	3.030
00102	3.060	00102	3.060
00103	3.090	00103	3.090
00104	3.120	00104	3.120
00105	3.150	00105	3.150
00106	3.180	00106	3.180
00107	3.210	00107	3.210
00108	3.240	00108	3.240
00109	3.270	00109	3.270
00110	3.300	00110	3.300
00111	3.330	00111	3.330
00112	3.360	00112	3.360
00113	3.390	00113	3.390
00114	3.420	00114	3.420
00115	3.450	00115	3.450
00116	3.480	00116	3.480
00117	3.510	00117	3.510
00118	3.540	00118	3.540
00119	3.570	00119	3.570
00120	3.600	00120	3.600
00121	3.630	00121	3.630
00122	3.660	00122	3.660
00123	3.690	00123	3.690
00124	3.720	00124	3.720
00125	3.750	00125	3.750
00126	3.780	00126	3.780
00127	3.810	00127	3.810
00128	3.840	00128	3.840
00129	3.870	00129	3.870
00130	3.900	00130	3.900
00131	3.930	00131	3.930
00132	3.960	00132	3.960
00133	3.990	00133	3.990
00134	4.020	00134	4.020
00135	4.050	00135	4.050
00136	4.080	00136	4.080
00137	4.110	00137	4.110
00138	4.140	00138	4.140
00139	4.170	00139	4.170
00140	4.200	00140	4.200
00141	4.230	00141	4.230
00142	4.260	00142	4.260
00143	4.290	00143	4.290
00144	4.320	00144	4.320
00145	4.350	00145	4.350
00146	4.380	00146	4.380
00147	4.410	00147	4.410
00148	4.440	00148	4.440
00149	4.470	00149	4.470
00150	4.500	00150	4.500
00151	4.530	00151	4.530
00152	4.560	00152	4.560
00153	4.590	00153	4.590
00154	4.620	00154	4.620
00155	4.650	00155	4.650
00156	4.680	00156	4.680
00157	4.710	00157	4.710
00158	4.740	00158	4.740
00159	4.770	00159	4.770
00160	4.800	00160	4.800
00161	4.830	00161	4.830
00162	4.860	00162	4.860
00163	4.890	00163	4.890
00164	4.920	00164	4.920
00165	4.950	00165	4.950
00166	4.980	00166	4.980
00167	5.010	00167	5.010
00168	5.040	00168	5.040
00169	5.070	00169	5.070
00170	5.100	00170	5.100
00171	5.130	00171	5.130
00172	5.160	00172	5.160
00173	5.190	00173	5.190
00174	5.220	00174	5.220
00175	5.250	00175	5.250
00176	5.280	00176	5.280
00177	5.310	00177	5.310
00178	5.340	00178	5.340
00179	5.370	00179	5.370
00180	5.400	00180	5.400
00181	5.430	00181	5.430
00182	5.460	00182	5.460
00183	5.490	00183	5.490
00184	5.520	00184	5.520
00185	5.550	00185	5.550
00186	5.580	00186	5.580
00187	5.610	00187	5.610
00188	5.640	00188	5.640
00189	5.670	00189	5.670
00190	5.700	00190	5.700
00191	5.730	00191	5.730
00192	5.760	00192	5.760
00193	5.790	00193	5.790
00194	5.820	00194	5.820
00195	5.850	00195	5.850
00196	5.880	00196	5.880
00197	5.910	00197	5.910
00198	5.940	00198	5.940
00199	5.970	00199	5.970
00200	6.000	00200	6.000
00201	6.030	00201	6.030
00202	6.060	00202	6.060
00203	6.090	00203	6.090
00204	6.120	00204	6.120
00205	6.150	00205	6.150
00206	6.180	00206	6.180
00207	6.210	00207	6.210
00208	6.240	00208	6.240
00209	6.270	00209	6.270
00210	6.300	00210	6.300
00211	6.330	00211	6.330
00212	6.360	00212	6.360
00213	6.390	00213	6.390
00214	6.420	00214	6.420
00215	6.450	00215	6.450
00216	6.480	00216	6.480
00217	6.510	00217	6.510
00218	6.540	00218	6.540
00219	6.570	00219	6.570
00220	6.600	00220	6.600
00221	6.630	00221	6.630
00222	6.660	00222	6.660
00223	6.690	00223	6.690
00224	6.720	00224	6.720
00225	6.750	00225	6.750
00226	6.780	00226	6.780
00227	6.810	00227	6.810
00228	6.840	00228	6.840
00229	6.870	00229	6.870
00230	6.900	00230	6.900
00231	6.930	00231	6.930
00232	6.960	00232	6.960
00233	6.990	00233	6.990
00234	7.020	00234	7.020
00235	7.050	00235	7.050
00236	7.080	00236	7.080
00237	7.110	00237	7.110
00238	7.140	00238	7.140
00239	7.170	00239	7.170
00240	7.200	00240	7.200
00241	7.230		

In theory any of these programs should produce the requested delay. In practice we are looking for the best fit to the ideal requested value. In the example, that value would be 1.500 ns. Another requirement is that the value of the incremental delay increase monotonically as the requested delay is increased. To obtain the addresses for a best fit, a computer program was written that cycles through all possible delay address combinations, measures and records the delay, and address, and stores these values in RAM. The computer then looks for the best fit to the ideal curve. When it finds this best fit, it prints out the ideal value, address of the closest available delay, and does a second measurement of the delay and prints this value.

At the completion of this program, the printout will contain the delay addresses that will produce the most linear monotonically increasing delay. These delay addresses are stored in a PROM that is addressed by the software requested delay. The PROM is acting as a program director, insuring best fit of the requested delay.

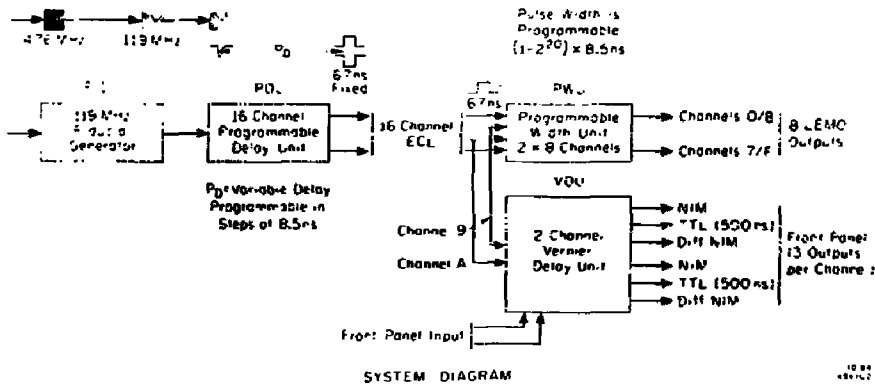
The computer printout is shown in Fig. 1 for the programming of a specific PROM. Each of the units will have a unique PROM program. The upper portion of the printout lists the delay at each address. The lower portion shows how to program the PROM to get the best fit available.

The result of a final test of the module is shown in Fig. 2. The PROM has been programmed and the module is functional and ready for delivery. Fig. 3 is a system diagram, Fig. 4 is a VDU-1 channel block diagram and Fig. 5 is a schematic of the module.

Module: 1700-1000-0  
 Module: 1700-1000-0  
 Module: 1700-1000-0

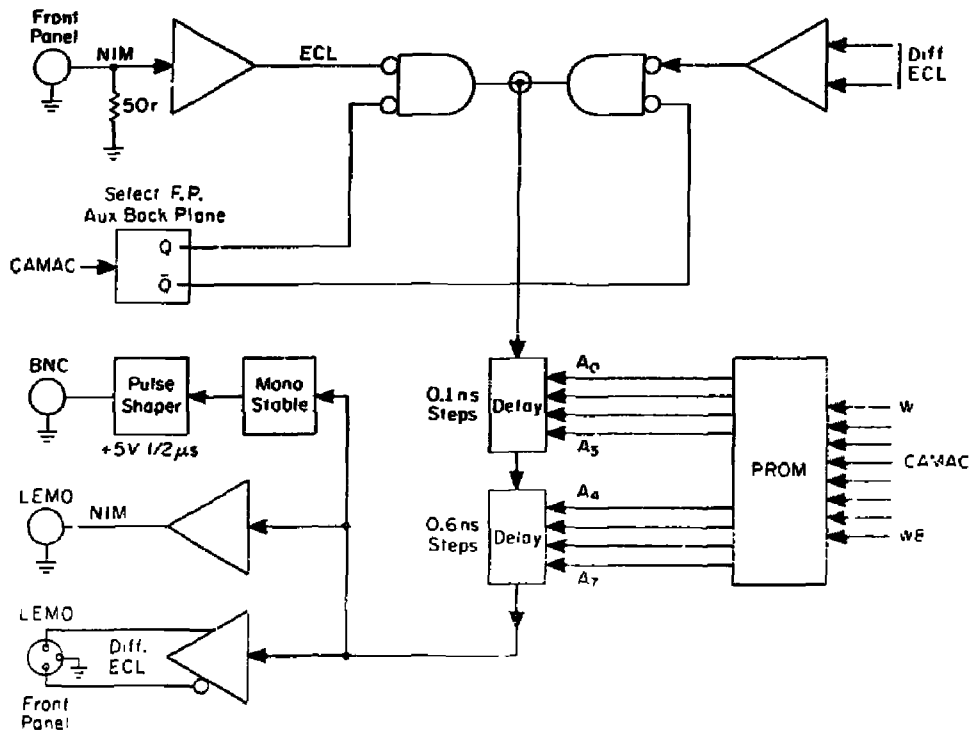
Address	Requested Delay (ns)	Actual Delay (ns)
0	0.000	0.000
1	0.100	0.100
2	0.200	0.200
3	0.300	0.300
4	0.400	0.400
5	0.500	0.500
6	0.600	0.600
7	0.700	0.700
8	0.800	0.800
9	0.900	0.900
10	1.000	1.000
11	1.100	1.100
12	1.200	1.200
13	1.300	1.300
14	1.400	1.400
15	1.500	1.500
16	1.600	1.600
17	1.700	1.700
18	1.800	1.800
19	1.900	1.900
20	2.000	2.000
21	2.100	2.100
22	2.200	2.200
23	2.300	2.300
24	2.400	2.400
25	2.500	2.500
26	2.600	2.600
27	2.700	2.700
28	2.800	2.800
29	2.900	2.900
30	3.000	3.000
31	3.100	3.100
32	3.200	3.200
33	3.300	3.300
34	3.400	3.400
35	3.500	3.500
36	3.600	3.600
37	3.700	3.700
38	3.800	3.800
39	3.900	3.900
40	4.000	4.000
41	4.100	4.100
42	4.200	4.200
43	4.300	4.300
44	4.400	4.400
45	4.500	4.500
46	4.600	4.600
47	4.700	4.700
48	4.800	4.800
49	4.900	4.900
50	5.000	5.000
51	5.100	5.100
52	5.200	5.200
53	5.300	5.300
54	5.400	5.400
55	5.500	5.500
56	5.600	5.600
57	5.700	5.700
58	5.800	5.800
59	5.900	5.900
60	6.000	6.000
61	6.100	6.100
62	6.200	6.200
63	6.300	6.300
64	6.400	6.400
65	6.500	6.500
66	6.600	6.600
67	6.700	6.700
68	6.800	6.800
69	6.900	6.900
70	7.000	7.000
71	7.100	7.100
72	7.200	7.200
73	7.300	7.300
74	7.400	7.400
75	7.500	7.500
76	7.600	7.600
77	7.700	7.700
78	7.800	7.800
79	7.900	7.900
80	8.000	8.000
81	8.100	8.100
82	8.200	8.200
83	8.300	8.300
84	8.400	8.400
85	8.500	8.500
86	8.600	8.600
87	8.700	8.700
88	8.800	8.800
89	8.900	8.900
90	9.000	9.000
91	9.100	9.100
92	9.200	9.200
93	9.300	9.300
94	9.400	9.400
95	9.500	9.500
96	9.600	9.600
97	9.700	9.700
98	9.800	9.800
99	9.900	9.900
100	10.000	10.000

Fig. 2. Final Test Printout



SYSTEM DIAGRAM

Fig. 3. System Diagram



15 64

VDU-1 CHANNEL BLOCK DIAGRAM

44415

Fig. 4. VDU-1 Channel Block Diagram

The following discussion refers to Fig. 5 [Schematic Drawing DS-135-756-01-R2], and is an effort to describe the circuit function of the chips utilized. U14, U17 are ECL line receivers that present proper terminations to the driving circuits. U16 and U15 are ECL gates that ultimately determine which condition is selected, i.e., rear panel, front panel or channel disabled. U11 and U12 are the programmable TTL registers that dictate which condition the gates will be in. (Again: front/rear panel select or disable) U18, 19, 20, 21 are the ECL programmable delays. U19, 21 are programmable delays of 15 steps of 0.1 ns per step. U18, 20 are programmable in 15 steps of 0.6 ns per step.)

U22, 24 are ECL line drivers that condition the output signal to the desired levels. U23 and U25 are ECL monostables that generate the fixed 500 ns output pulse width and Q4, Q5 and Q6, Q7 are discrete transistors that generate the +5 V amplitude of this 500 ns pulse. U1, U2 are latches that hold the requested delay that is on the CAMAC write lines. U7, U8 are PROMs that are programmed to get the optimum incremental delay response. U3, U4, U5 are TTL circuits used to read back the information as to what delay has been programmed into the circuit. U3 and U4 act as a multiplexer selecting between Ch1 and 0. U5 is the CAMAC READ line driver. U13 is the "n" light driver.

#### DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

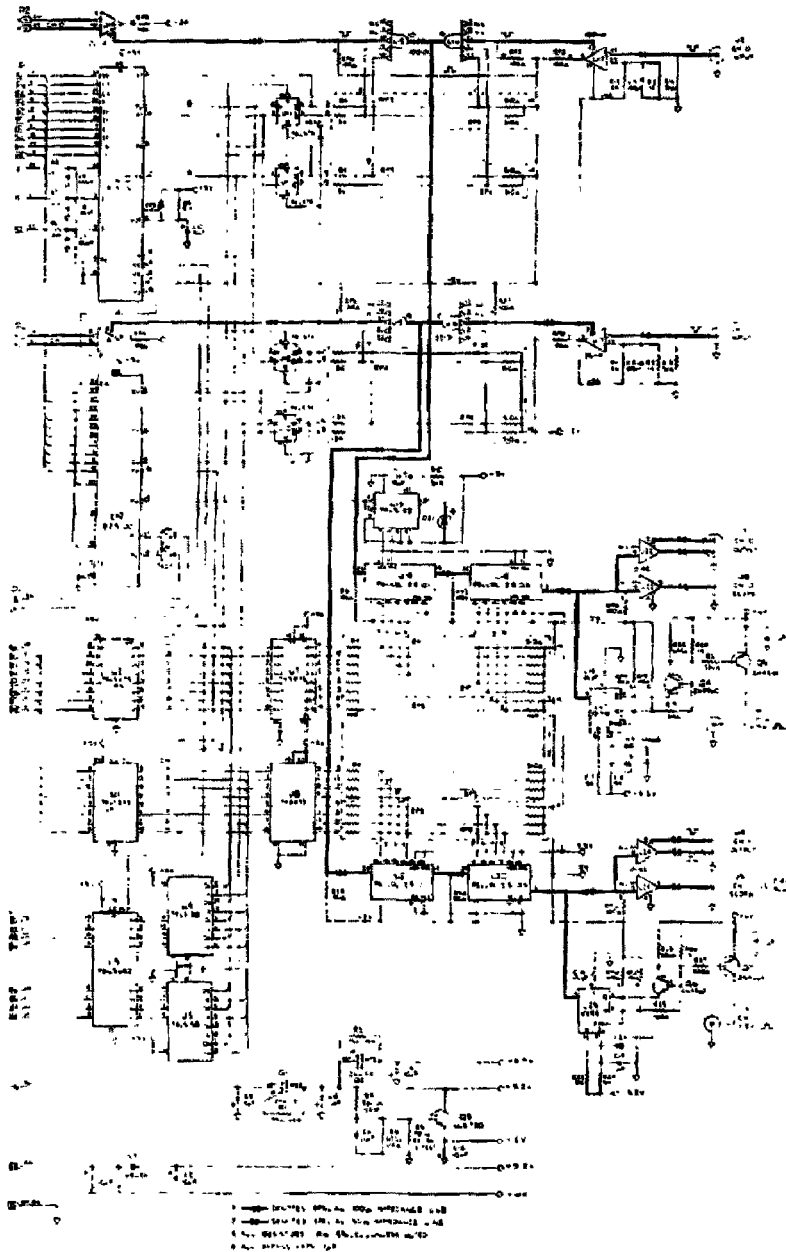


Fig. 5. Module Schematic

The VDU module is a single width CAMAC module. Figure 6 is a photo of the module.

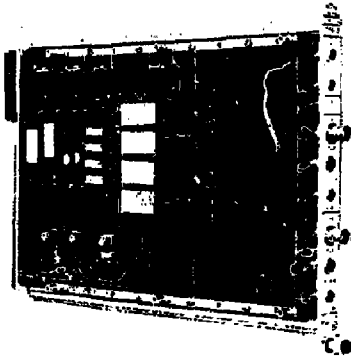


Fig. 6. VDU Module

The CAMAC commands utilized for this module are as follows:

#### CAMAC CODES

- Power On, F9=AX=82, I=82 will disable all outputs and clear all channels.
- F0 A0/A1 : Read the contents of the delay register. Q=1 implies that the auxiliary backplane is selected AND channel (0/1) is enabled.
- F1 A0/A1 : Read the contents of the delay register. Q=1 implies that the front panel is selected AND channel (0-1) is enabled.
- F10 A0/A1 : Disable channel (0/1).
- F16 A0/A1 : WRITE W1-W7 into channel 0 or 1, in straight binary. This command also selects the auxiliary backplane, and enables the output.
- F17 A0/A1 : Same as F16 A(0/1) except that the inputs are selected from the front panel.
- F25 A0/A1 : Enable channel (0/1). Enable rear panel input.
- F26 A0/A1 : Enable channel (0/1). Enable front panel input.
- F27 A0/A1 : Q=1 implies that channel (0/1) is enabled.