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HIGH SENSITIVITY AMPLIFIER/DISCRIMINATOR FOR PWC'S

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I. Introduction

The facility support group at Fermilab is designing and building a general purpose beam chamber for use in several locations at the laboratory. This pwc has 128 wires per plane spaced 1 mm apart. An initial production of 25 signal planes is anticipated.

In proportional chambers, the size of the signal depends exponentially on the charge stored per unit of length along the anode wire. As the wire spacing decreases, the capacitance per unit length decreases, thereby requiring increased applied voltage to restore the necessary charge per unit length[1]. In practical terms, this phenomenon is responsible for difficulties in constructing chambers with less than 2mm wire spacing. 1mm chambers therefore, are frequently operated very near to their breakdown point and/or a high gain gas containing organic compounds such as "magic gas" is used. This argon/iso-butane mixture has three drawbacks: it is explosive when exposed to the air, it leaves a residue on the wires after extended use and is costly. An amplifier with higher sensitivity would reduce the problems associated with operating chambers with small wire spacings and allow them to be run a safe margin below their breakdown voltage even with an inorganic gas mixture such as argon/CO2, thus eliminating the need to use "magic gas". Described here is a low cost amplifier with a usable threshold of less than 0.5 uA. Data on the performance of this amplifier/discriminator in operation on a prototype beam chamber are given. This data shows the advantages of the high sensitivity of this design.

II. Design Considerations

For a pwc amplifier/discriminator, five attributes are desirable: high sensitivity with low inherent noise, high reliability, small physical size, low power consumption and low cost.

The amplifier/discriminator can be divided into three sections: front end amplifier, discriminator, and line driver. The front end determines the sensitivity and noise performance of the whole system. It should have a good impedance match to a wire chamber, and produce a large enough signal for the discriminator. The only off-the-shelf amplifier chips with sufficient gain and frequency response presently available are the ECL logic gates run as amplifiers or video amplifier integrated circuits. The ECL chips use a large amount of power, have a relatively low density, and have a bandwidth approaching 200 Mhz which is much more than required making circuit design unnecessarily difficult. The video

amplifiers offer advantages in packaging density, power consumption, and have less bandwidth (of order 100Mhz). This is quite adequate for wire chamber signals and makes layout considerations somewhat easier. The third alternative for the front end is a custom designed amplifier realized with discrete components. The only drawback to this approach is the low packaging density and the large number of associated components such as resistors and capacitors.

There are three basic discriminator elements available: TTL output comparators, ECL output comparators, and a tunnel diode used in conjunction with a high bandwidth amplifier, usually an ECL gate amplifier. The TTL comparators have good performance, reasonable power consumption, low price, and good packaging density. These IC's have one major drawback. TTL outputs cause large switching transients on the power lines. These will feedback to the front end section unless the supply lines are decoupled with great care. The ECL output comparators are ideally suited for pwc readout systems having excellent performance and inherent line drive capability but are very costly. The tunnel diode/amplifier scheme performs well but is also expensive.

ECL level differential line drivers are the most commonly used for outputs of amplifier/discriminators and are easily implemented with available driver gates.

III. Amplifier Description

For the amplifier section used here a 733 video amplifier was chosen for the the principal gain block. It does not have by itself sufficient sensitivity to operate at the very low thresholds sought for our application. A discrete two transistor stage was added (Fig 1). The first transistor is a common base impedance matching stage which has an intrinsic input impedance of about 100 ohms. If a larger input impedance is desired an appropriate series termination resistor can be added .The second transistor, a common emitter stage can be analyzed approximately as a transresistance amplifier with a feedback resistor of 5600 ohms. This would give a 5.6 Mv output voltage change for each uA of input current. The 733 has a fixed voltage gain of 100. The amplifier section should then produce about 560 mV per μA of input current. In practice, because of the finite gain of the second transistor, the amplifier delivers about 480 mV/uA.

A TTL discriminator was chosen for reasons of economy. The problem of power line transients can be largely eliminated through the use of distributed capacitance power busing. Care has been exercised in signal path layout and as much ground plane as possible was used on the circuit board. The outputs of the 733 are capacitively coupled to the inputs of the discriminator which are terminated with 1000 ohms. A 100K ohm resistor is connected from one input of the discrinator to the threshold bus. With the 1K terminating resistor a resistive divider is formed which results in 10 mV of input offset for each volt of threshold voltage.

Most chamber readout systems have 100 ohm ECL level balanced inputs. If a TTL output discriminator is used, there must be a level shift to ECL as well as a driver stage. A 10124 ECL chip

performs both functions.

IV. Amplifier Performance

A prototype 16 channel amplifier/discriminator card using these design features has been made. The ratio of external threshold voltage to minimum input current sufficient to produce an output pulse was measured to be 24 volts per μA. The minimum usable threshold on a bench test was 0.25 μA. The card was operationally tested on a prototype beam chamber with 1 mm wire spacing and an anode to cathode gap of 3.2 mm. For this test,a Ruthenium beta source was placed on one side of the chamber and two thin scintillator counters were placed opposite the source on the other side. Efficiency was defined to be the ratio of three-fold coincidences between the counters and chamber and two-fold coincidences between the counters. The minimum attainable threshold was 0.3 μA. Under the same conditions, the minimum threshold for the LeCroy PCOS III amplifier card was 0.8 μA.

Plateau curves for different threshold settings and gas mixtures for the two cards are shown in figures 2A and 2B. The difference in operating sensitivities clearly manifests itself in a lower plateau voltage using our card. A difference in threshold of a factor of two results in a change in voltage at plateau of about 100 volts. Changing gas from Ar/CO2 to "magic gas" reduces the voltage at plateau about 75 volts.

The card draws 750 mA of -5V and 400 mA of +5V. The estimated cost of fabrication by an outside vendoris of order $6.00 per wire and the card has overall dimensions of 5"x6". It is a plug in alternative for the the LeCroy PCOS III card. Time slew measurements show a change in transit time through the amplifier of 7 nsec for an input signal change in magnitude fron 2X threshold to 20X threshold (Fig.2). This time slew results from the relatively slow rise time of the preamplifier stage. For drift chambers where time slew is critical but wire signals are large, the amplifier could be used without the discrete transisitor section. Such a card could be expected to have a minimum usable threshold of order 1 μA and a 2X to 20X threshold time slew of 2-3 nsec.

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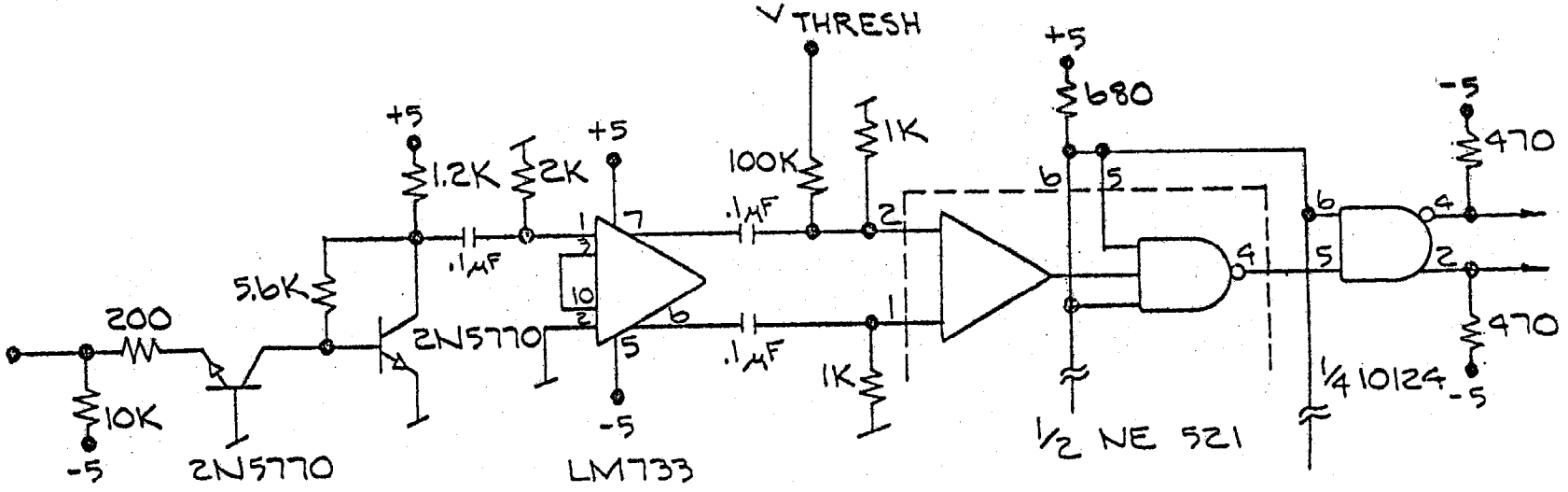
SCHEMATIC

FIG. 1



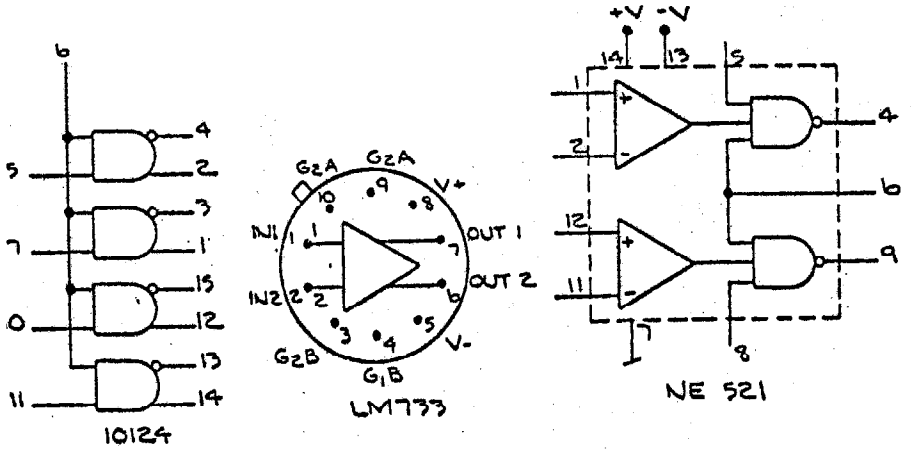


FIG. 2 TIME SLEW

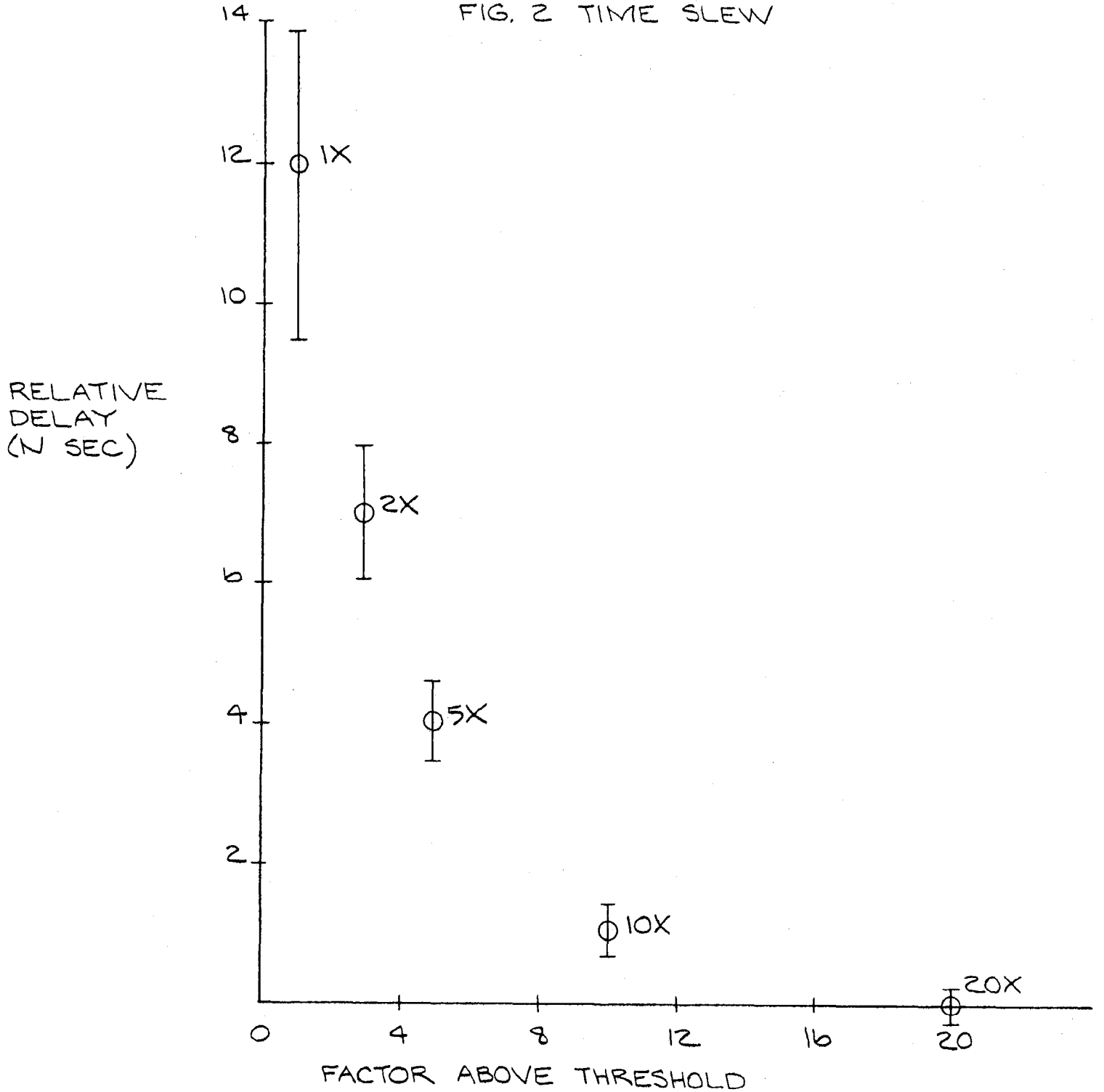
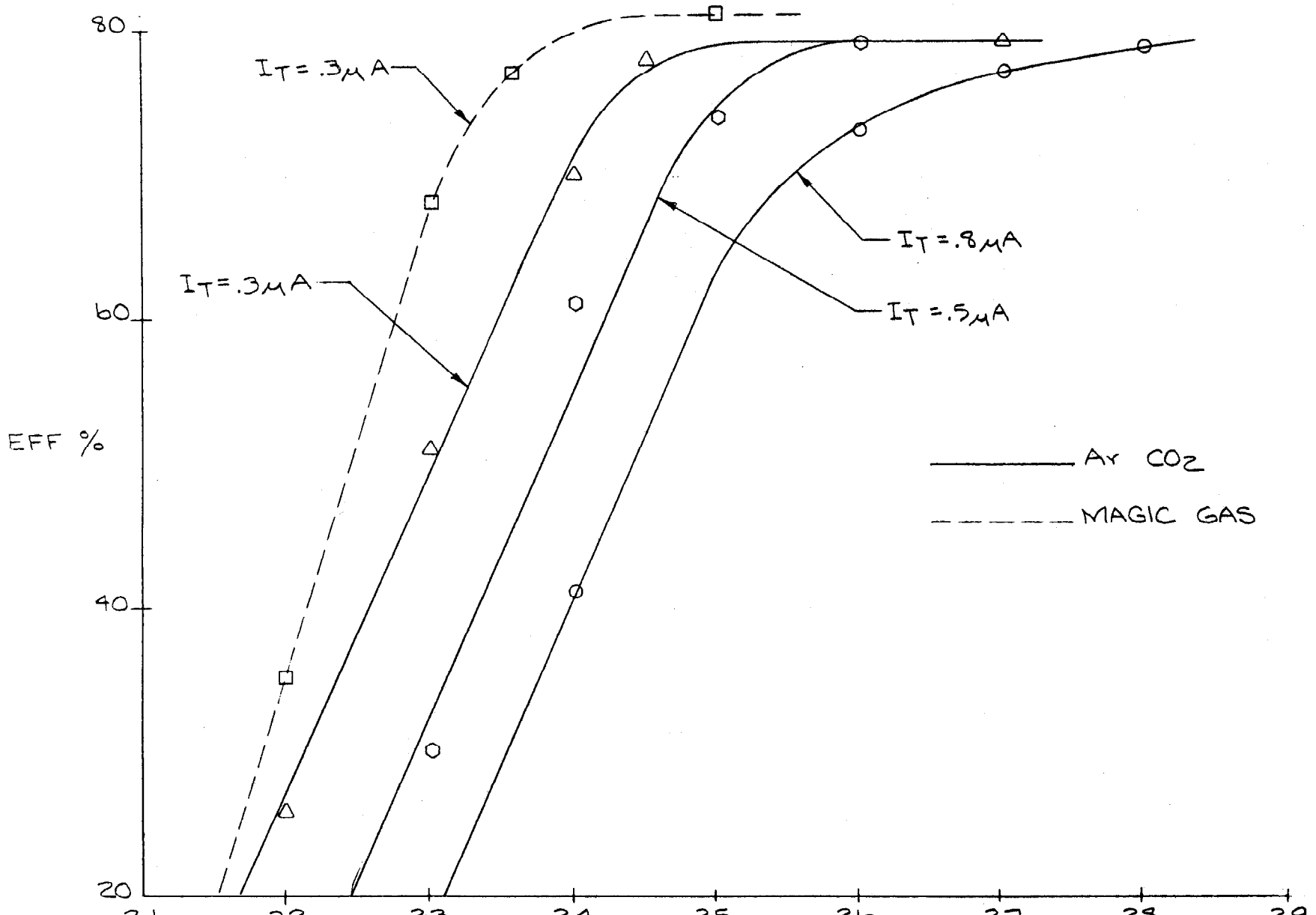
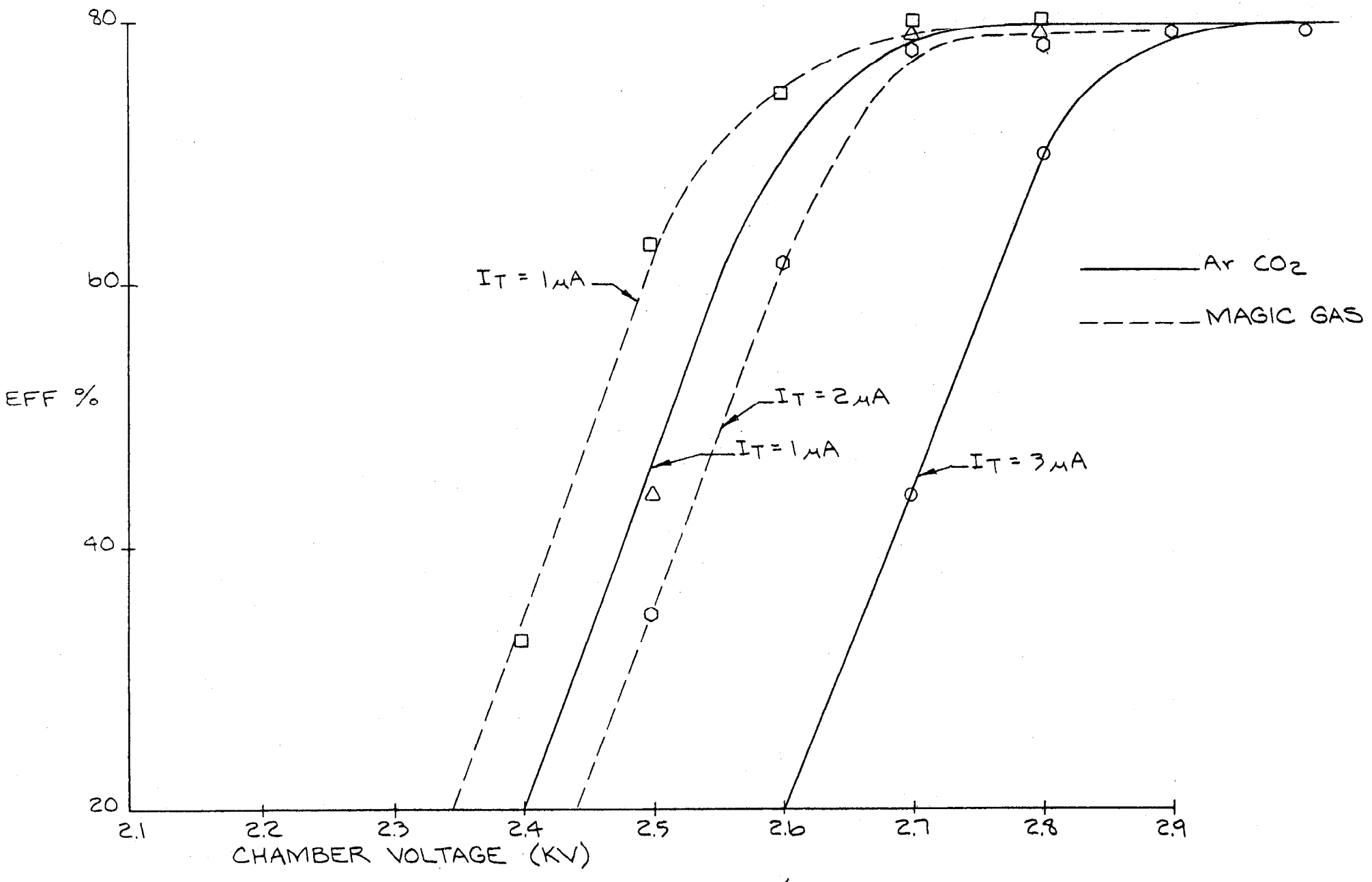


FIG. 3A



PLATEU CURVES FOR FSG AMP/DISC
ON 1mm CHAMBER

FIG. 3B



PLATEAU CURVES FOR PCOS III AMP/DISC
ON 1mm CHAMBER