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MAGNET POWER SUPPLY CONTROL, OF THE NSLS VUV AND X-RAY STORAGE RINGS, TRANSFER LINES

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Abstract

The transfer lines for NSLS VUV and X-ray storage rings have been split. New power supplies have been incorporated with existing ones. The existing microprocessor system has been upgraded in order to control the additional functions. This system expands the input/output port of the microprocessor to an addressable serial/parallel link to each magnet power supply. The implementation of this system will be discussed.

Introduction

In the past at the NSLS the beam transfer lines from the booster ring to the VUV and X-ray ring shared common power supplies and control. They have been converted to separate systems and each transfer line has its own power supplies and controls. The controls were developed so that the existing microprocessor systems could do more tasks and thus minimize the demand for additional communication lines to the central computer system. The control bus to perform the function is a parallel multi-drop system. This bus is an extension of the input/output ports of the microprocessor board. The bus was implemented in two different ways, one to control purchased power supplies and the second for NSLS developed power supplies.

The bus is addressable and interactive so that when data and commands are sent out, a reply is sent back to the microprocessor. The bus is called P-BUS.

Design Goals

The purpose of a parallel bus (PBUS) is to link microprocessors to devices or other microprocessors. It allows placing device hardware external to the microprocessors. Signal processing modules such as A/D converters can be placed near the control equipment and minimizes the distance over which analog signals must be run. In some cases the number of devices per micro is limited by the number of cards that may be put in a crate or the number of connectors that can be placed on the rear of a micro crate. Placing device hardware outside the micro overcomes these limitations. It also allows some standardization of hardware.

The following definition was proposed as a standard so that all implementations of a bus would be the same. Many different devices may reside on the bus. The only requirement is that each device should have its own address or range of addresses.

The design requirements were:

1. It should be very easy to implement for simple devices.

2. It should allow for communications with a smart device such as another micro. It is supposed that some device would contain a micro and have some response time limitations such that a handshake would be required.

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Parallel Port Bus

The parallel port bus is based on the standard Intel single board computer 24-bit parallel port. Intel uses the 8255 parallel port chip on many of their computer and peripheral boards. This chip has three 8-bit parallel ports which may be operated in several modes. The parallel port bus uses port A as an 8-bit bidirectional data bus. The 80/24 computer board used at the NSLS comes with bidirectional driver on port A and it is used for inputting or outputting data to a device. Port B is used as an output port for the address of the selected device. The 8255 allows the third port (C) to be split, where 4 upper bits are used for output and 4 lower bits for input. In addition, the port C bits can be individually set. Two input and two output bits are used to control the transfer of data between external devices and the computer.

The other two input bits and two output bits have been defined for special functions. One output bit is available for use in a heartbeat circuit. The micro will set this bit periodically, probably once a second or sooner, where it is necessary for the external device to be aware when the micro is not running. Presently, each time this bit is triggered a one-second timer is started in the interface. If the micro fails, and the timer is not reset in a second, an indication is given to the external device.

An output bit is reserved to allow resetting an external device which is an addressable command.

An input status bit can be set by external equipment and the micro polls each address for data available bit.

One input bit is special in that it is non-addressable or active input that may be pulled down by external devices to request attention. For the cases where it is inefficient to poll devices, this will allow the generation of an interrupt by external devices. After an interrupt, the micro will poll to determine which device has data available bit.

General Hardware Interface to Parallel Bus

This section describes the interface when devices are controlled with the standard PBUS hardware.

The standard PBUS interface is a printed circuit board which has an address and appears to the micro as four 8-bit output registers and four 8-bit input registers which can be used for setting magnitude for the devices or for ON/OFF control or for inputting device magnitude and status.

P-Bus Hardware Description

P-Bus for the NSLS developed power supplies was developed using differential twisted pair. The line drivers and receivers are RS-485 type which can handle 64 nodes at a distance of 4,000 ft. and a data rate of 10,000 K bits per second. The cable selected was an overall shielded 25 twisted pair, UL style 2464. The connectors for the cable is a "AMP" champ (TM) which is the same type as used in telephone installations. The connectors are inexpensive and easily terminated. The connector is an insulation displacement type and tooling is straight forward. The other advantage of

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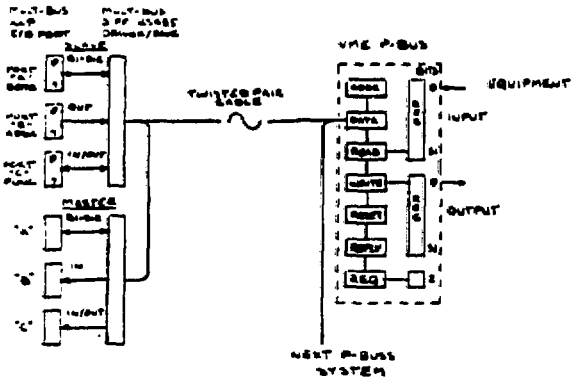
these terminations is that they mix well with ribbon and other connector families.

The printed circuit boards developed for the system was a multi-bus driver receiver board. The board takes the single-ended signals from I/O port of microprocessor board and converts them into RS-485 differential signals. This board goes to the outside world and connects to the remote equipment interface board.

The equipment interface board has RS-485 drivers and receivers and makes the transition back to the single-ended. The equipment board is packaged on a VME format. The post header connector configuration allows for direct connection to devices such as relays, optical isolators, or an inversion in the logic and are high current open collectors. The signals on the VME connector are the input and output registers. The input and output registers interface with the equipment. The equipment requirements are ON/OFF control, status bits and interlocks, digital to analog converters and analog to digital converters. The system configuration is shown below. Some other subset function boards that have been developed and which interface with the P-Bus equipment board are optical isolators, D/A, A/D and ON/OFF control. The other boards use the P-Bus equipment board as a front end and data is sent and collected as standard 64 bit I/O. The other boards are packaged on the same format and have the same pin numbers, which enable them to be bussed at the I/O bit level.



P-Bus System

Transfer Line Description

Quadrupole Power Supply System

1. Power Supply Set Point Control

The quadrupole power supply system controls all transfer line quadrupole magnet currents. There are two such system, one for each transfer line. Each transfer line consists of 11 quadrupoles with their nominal values as following for 750 MeV injection:

Quads	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11
Volts	7	59	64	65	28	31	67	55	48	63	43
Amp	140	4.2	4.5	3.2	5.5	3.8	4.8	6.7	3.4	4.5	3.0

As shown in Fig. A, the parallel port interface sends 12 bit set point to the power supply interface logic. The 12 bit DAC provides the reference voltage to the self-regulated power supply. The power supply output is connected to the magnet along with a shunt

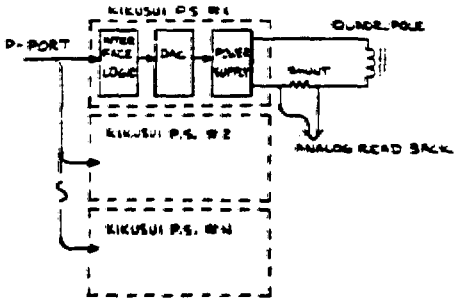


Fig. A. P-Port System

in series. The block diagram of the system is shown in Fig. A and following is given the description of each functional block.

2. Interface Logic

The interface logic block diagram is shown in Fig. B. The parallel port interface carries the address and the data on the same bus and the strobe is sequenced with the data. When the address is on the bus, the address strobe is generated and the address is latched into the address latch. The output of the latch goes to the one side of the comparator; the local address selected by a switch goes to the other side of the comparator as shown in Fig. B. Next, data is placed on to the bus with a data strobe. Data is latched into the data latches only if the computer address matches the local address, set by local switches, because, only then, the enable sign will be high. The 12-bit data is optically isolated before it goes to the DAC.

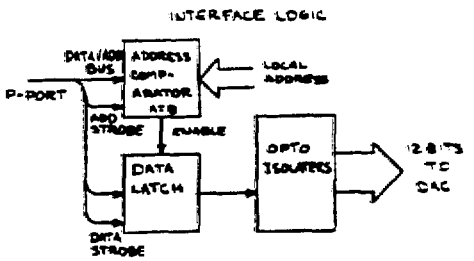


Fig. B. P-Port Interface

3. Digital to Analog Converter

A 12-bit digital to analog converter converts optically isolated digital signal to the analog voltage. The range of this voltage is from 0 to 1 volt. The output of this converter is used as a reference to the power supply input.

4. Regulated Power Supply

The regulated power supplies are stand alone and are manufactured by Kikusui International. Most of the power supplies have regulation of better than 1 part in 4000. The power supply output is directly connected to the quadrupole magnet with a calibrated shunt in series. The shunt output signal is used for reading the current into the computer.

5. Power Supply Read Back

The power supply read back system consists of a slave microprocessor system. This system contains a CPU card and a 12 bit analog to digital converter card. Sixteen analog signals are multiplexed to this analog to digital converter. All the shunts signals are routed to this card and these shunt signals are read by the microprocessor. The slave microprocessor communicates with the master on a regular basis via a second parallel port interface bus as shown in Fig. C.

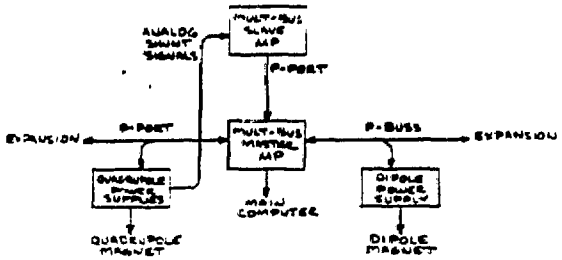


Fig. C. Microprocessor System

Dipole Power Supply System

The dipole power supply system provides the current for the transfer line bending magnets. There are two such systems, one for the booster to UV transfer line and the other for the booster to X-ray transfer line. The block diagram of this system is shown in Fig. D. The dipole power supply system is connected to the master microprocessor system via a parallel port bus, which is bi-directional and uses a protocol to establish communication.

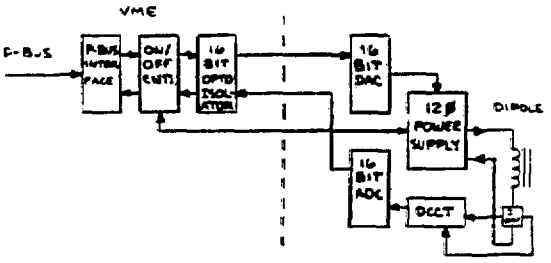


Fig. D. Dipole Power Supply

The P-Bus interface provide the input and output latches and the read and write strobes for the data. The 16-bit data output is optically coupled to the high precision 16-bit digital to analog converter. The output of the converter is used as a computer reference voltage to the 12-phase regulated power supply.

The transfer line bending magnet is connected to this power supply. A DCCT (high precison current transformer measuring system) is used to provide the feedback reference to the regulator system. This signal is also used as a readback signal for the computer and a 16-bit analog to digital converter is used.

An ON/OFF card provides the on, off and interlock for the power supply from the computer.

Software

The software controlling the power supplies runs on the single board computer Intel 80/24. The control monitor receives the various commands such as set magnitude, ON/OFF and Reset commands, read magnitude etc. from the operators and issues them to the devices through the P-Bus. The microcode has been made more generalized by defining a device type which could encompass the various types of devices (whether read or write only or both or ON/OFF type or a combination of all). As already described earlier, the hardware interface between the P-Bus and the devices have been standardized and library driver routines for P-Bus interface have been provided. This allows the microcode implementation easy and fast.

Conclusion

This system has enabled us to expand our existing systems without adding more central computer lines or microprocessor systems. We have been able to define and build standard hardware interfaces, and associated software. When building new equipment there is more thought given to the possibility of using the existing equipment as when building new equipment, and designing it such that it can be used elsewhere. The micros are stationary and new equipment is installed at some distance from the equipment interface. This enables us to process data locally (analog) and transmit back digitally. The noise is reduced, therefore, the greater the precision. The hardware and software package go together quickly and a system can be added in short machine maintenance periods. This system is also used in the control of the X-ray RF power amplifier system and is planned to be used elsewhere in the machine control functions.

References

1. K. Batchelor, B.B. Culwick, J. Goldstick, J. Sheehan, J. Smith, Distributed control system for the National Synchrotron Light Source, Proc. of the 1979 Part. Accel. Conf. IEEE Trans. Nucl. Sci. NS-26 No. 3, p 3387.

2. E. Bozoki, B.B. Culwick and J.D. Smith, Status of the National Synchrotron Light Source Control System, Proc. of the 1981 Part. Accel. Conf. IEEE Trans. Nucl. Sci. NS-28, No. 3, part 1, p 2183.

3. J.D. Klein, J.F. Sheehan, Microprocessor techniques and construction at the NSLS, Proc. of the 1983 Part. Accel. Conf. IEEE Trans. Nucl. Sci. NS-30, No. 4, part 1, p 2222.

4. D. Pipinger, J. Miller, Driver/receiver family extends data-link performance, Electronic Products, January 15, 1985, p 97.