CONF-851071--1

CONF-851071--1

DE85 013874

DETAILED DESIGN OF A 13 KA 13 kV DC SOLID-STATE TURN-OFF SWITCH*

W. F. Praeg

Argonne National Laboratory
9700 South Cass Avenue
Argonne, Illinois 60439

To be presented at the
1985 Annual Meeting of the
IEEE-Industry Application Society

Royal York Hotel
Toronto, Canada

October 6-11, 1985

*Work supported by the U.S. Department of Energy.

DETAILED DESIGN OF A 13 kA 13 kV DC
SOLID-STATE TURN-OFF SWITCH*

W. F. Praeg
Argonne National Laboratory
9700 S. Cass Avenue
Argonne, IL 60439

Abstract: An experimental facility for the study of electromagnetic effects in the First Wall-Blanket-Shield (FWBS) systems of fusion reactors has been constructed at Argonne National Laboratory (ANL). In a test volume of 0.76 m^3, a vertical, pulsed 5 kG dipole field ($\dot{B}$ < 320 kGs^{-1}) is perpendicular to a 10 kG solenoid field. Power supplies of 2.75 MW at 550 V dc and 5.5 MW at 550 V dc and a solid-state switch rated at 13 kA and 13 kV (169 MW) control the pulsed magnetic fields. The total stored energy in the coils is 2.6 MJ. This paper describes the design and construction features of the solid-state switching circuit which turns off a dc current of 13 kA in approximately 82 μs and holds off voltages of < 13 kV.

Introduction

The FWBS system of a fusion reactor generally lies between the plasma and the magnets that provide confinement, equilibrium, shape, and position control. In that location, the system is subject to electromagnetic effects both from plasma displacement or disruption and from normal or abnormal magnetic field changes from the magnets. In these cases, eddy currents are created which generate large forces, torques, and stresses. They can also produce resistive heating, breakdown of insulation, and spurious signals in FWBS instrumentation. The importance of these electromagnetic effects and the uncertainty in the ability to estimate them with sufficient accuracy, led to the selection of electromagnetic effects as one of the areas for study under the FWBS Engineering Test Program of the Department of Energy. To carry out the necessary experiments, the facility shown in Figs. 1 and 2 was built at ANL, and given the name FELIX [1] (Fusion ELectromagnetic Induction eXperiment). In a useful volume of 0.76 m^3, the constant field of a fusion reactor is modeled by a slowly pulsed solenoid field that has a rise and fall time of 3 s and a flattop of 7 s. The pulsed field is modeled by a pulsed dipole field that has a rise time of 0.42 s, a flattop of 3.5 s, and a variable decay time of 16 ms or more which simulates a plasma disruption. The repetition rate is 1 ppm. This paper describes the switching circuit that disconnects the

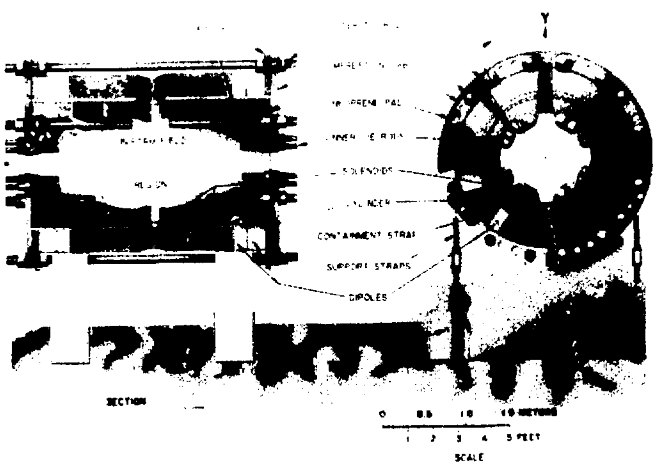

Fig. 1. FELIX Components and Experimental Volume

*This work supported by the U.S. Department of Energy.

5.5 MW dc power supply of the dipole coils in approximately 82 μs, and forces a discharge of the dipole fields with L/R time constants between 0.016 < τ < 0.128 s. The switch holds off voltages < 13 kV.

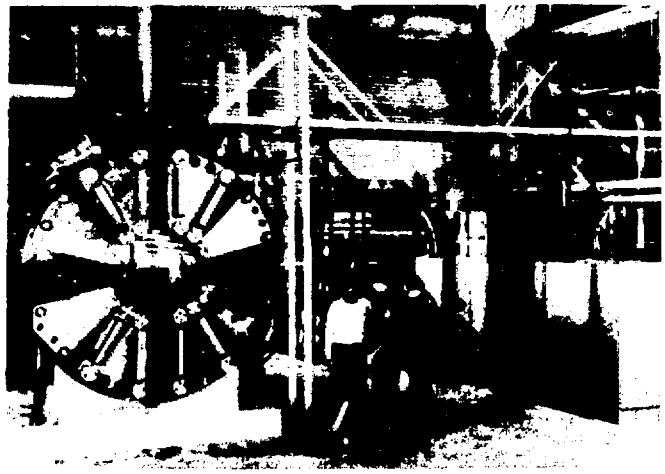

Fig. 2. FELIX Facility with Disk Experiment

Pulsed Power Supply

A block diagram of the dipole power supply is shown in Fig. 3. The dc power supply for the solenoid

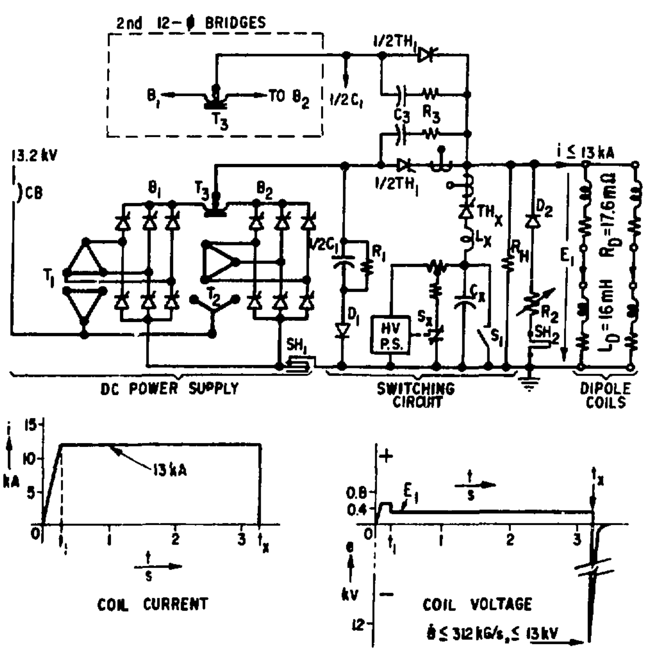

Fig. 3. Block Diagram of Dipole Power Supply

coil is identical, but without the solid-state switching circuit and discharge resistors. Both power supplies have an output voltage of 550 V dc; the solenoid supply drives the current up to 12.4 kA in 3 s, holds it at that value for 7 s, and thereafter drops it to zero in another 3 s. In the middle of this 7 s flattop, the dipole field is discharged with a time constant determined by resistor R_2. The above cycle can be repeated every 60 s. Each of the two power supplies has two identical 12-phase rectifier circuits operating in parallel. Each 12-phase rectifier comprises two 3-phase full wave bridges (B_1 and B_2) connected in parallel through an interphase transformer (T_3); the diagram of Fig. 3 shows details of one of the two 12-phase rectifier circuits.

The dipole power supply is connected to a 5.3 MVA rectifier transformer, which can withstand the pulsed magnetic forces associated with sudden current interruption from 30% overload. One 13.2 kV circuit breaker feeds both transformer primaries from a nearby substation. The rectifier thyristor phase control uses a current regulator with a feedback from a 175-μΩ coaxial shunt, SH_1, that monitors the dc output. The regulator controls the gate drive circuits for all thyristors in the 12-phase systems covering the range from full rectification to power inversion. Any current level may be selected on a 12-bit D/A converter which is set by a binary up-down counter either at the power supply or remotely by the computer.

Switching Circuit

Circuit Operation

One of the many logic circuits controlling the power supply ensures that power can only be turned on when the 500 μF capacitor bank C_x in Fig. 3 is charged to ≤ 13 kV. At time t_o, the output voltage of the dc power supply is gradually increased by rectifier phase control to limit the inrush current into capacitor C_1. Shortly before the 6000 μF capacitor bank C_1 is charged to 510 V, thyristor assembly TH_1 is gated on causing the dipole current to rise at a rate of $di/dt = E_1/L_D = 510$ V/16 mH = 32 kA/s. This corresponds to a di/dt value of 0.0032 A/μs for each of the ten parallel connected thyristor modules that make up TH_1, which is too small to turn them on. In order for the thyristors to reach a "latching" current of about 2.2 A per module, a 25 Ω resistor, R_H, rated 9 kW pulls 22 A. After ~ 0.42 s, the dipole current has reached 13 kA, generating a field of 5 kG. At that time, t_1, the regulator reduces the power supply output voltage to ~ 245 V to maintain this current within ±0.1%. During the flattop time (t_1 to t_x), the dipole field penetrates the experimental test piece, and eddy currents in the test piece, generated during the current rise, decay to insignificant values. The actual test starts at time t_x when the power supply is disconnected from the dipole coils. At this time, thyristor TH_x is turned on applying the ≤ 13 kV charge on capacitor C_x to the circuit. Capacitor C_x has three discharge paths through L_x and TH_x. One is via TH_1, C_1, and D_1; a second through R_H, and a third via the dipole coils. There are four distinct circuit conditions. The first is when thyristor TH_x has turned on; a second, when thyristor TH_1 has turned off. The third condition exists when capacitor C_x has discharged and no longer back biases diode D_2, and the fourth condition, when capacitor C_x is charged to its negative peak voltage. After that, the dipole coil current flows only through R_2, D_2, and R_H.

When, at time t_x thyristor TH_x has turned on, capacitor C_x oscillates with inductor L_x through capacitor C_1 at a frequency of $f_1 = 828$ Hz (T/4 = 302 μs), and with the dipole L_D at a frequency of $f_2 = 56.3$ Hz (T/4 = 4.44 ms). The capacitor discharge current is:

$$i_{C_x} = i_{TH_1} + i_{L_D} + i_{R_H} \qquad (1)$$

$$i_{C_x} = \frac{e_{C_x}}{\omega_1 L_x}\,\epsilon^{-\alpha_1 t}\sin\omega_1 t + \frac{e_{C_x}}{\omega_2 L_D}\,\epsilon^{-\alpha_2 t}\sin\omega_2 t + \frac{e_{C_x}}{R_H} \qquad (1')$$

where

$$\alpha_1 = \frac{R_x}{2L_x}, \qquad \alpha_2 = \frac{R_D}{2L_D}$$

$$\omega_1 = \left(\frac{1}{L_x C_x} - \frac{R_x^2}{4L_x^2}\right)^{1/2}; \qquad \omega_2 = \left(\frac{1}{L_D C_x} - \frac{R_D^2}{4L_D^2}\right)^{1/2}$$

With C_x charged to 13 kV at time t_x and 13 kA flowing in the dipole coils, it takes 82.3 μs for the current through TH_1 to go to zero at time t_1 as shown in Fig. 4a. During this time, the current through capacitor C_x, inductor L_x, and the dipole coil has risen to 13064 A and the capacitor voltage has decayed to 11.82 kV as shown in Fig. 4. With TH_1 turned off, capacitor C_x keeps oscillating with the dipole inductance L_D at 56.3 Hz, driving the current up to 13.23 kA between times t_1 and t_2 as shown in Fig. 4a.

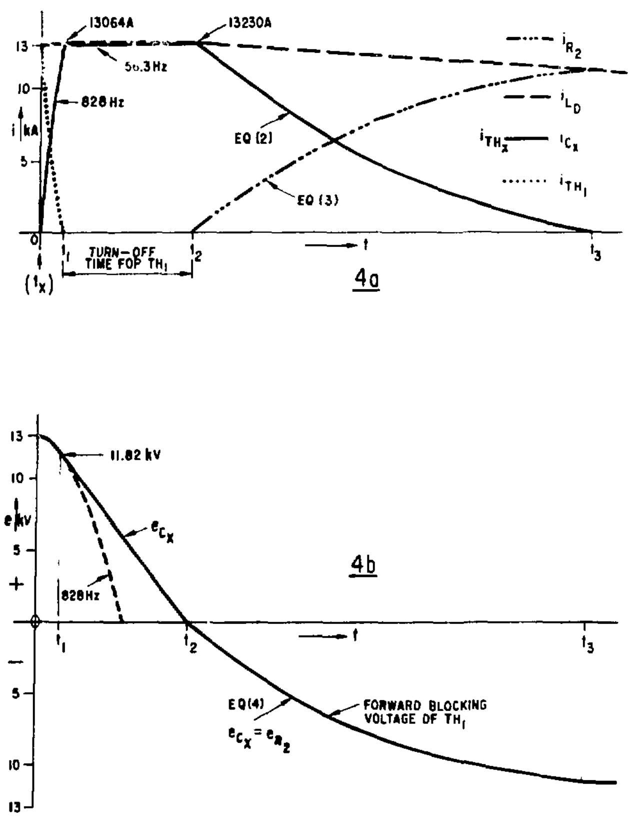

Fig. 4. Current and Voltage Waveshapes of the Switching Circuit

During this time interval, the average dipole current of $i_{C_X} = (13064 + 13230)/2 = 13.15$ kA discharges capacitor C_x in:

$\Delta t = e_{C_x} C_x / i_{C_x} = 11.82$ kV x 500 μF/13.15 kA = 449 μs;

thyristor TH_1 regains its forward blocking ability during this time. With capacitor C_x discharged, diode D_2 is no longer back biased and resistor R_2 becomes part of the circuit. Resistor R_2 overdamps the oscillatory circuit comprised of the dipole coils and capacitor C_x. The dipole coil current transfers from the capacitor to the resistor during the time it takes to charge C_x to its negative peak voltage; as illustrated in Fig. 4 between times t_2 and t_3. Neglecting the effect of L_x = 80 μH vs the dipole inductance L_D = 16 mH, the current and voltage shapes during transfer are:

$$i_{C_x} = I\varepsilon^{-\alpha_3 t}(\cosh \omega_3 t - \frac{\alpha_3}{\omega_3} \sinh \omega_3 t) \quad (2)$$

$$i_{R_2} = \frac{I}{\omega_3 R_2 C_x} \varepsilon^{-\alpha_3 t} \sinh \omega_3 t \quad (3)$$

$$e_{C_x} = e_{R_2} = \frac{I}{\omega_3 C_x} \varepsilon^{-\alpha_3 t} \sinh \omega_3 t \quad (4)$$

where

$$\alpha_3 = \frac{R_2 R_D C_x + L_D}{2 R_2 C_x L_D}$$

$$\omega_3 = \left(\alpha_3^2 - \frac{R_2 + R_D}{R_2 C_x L_D}\right)^{1/2}$$

I = dipole current at time capacitor voltage is zero

t = time after capacitor voltage is zero.

Figure 5 shows current and voltage shapes during the transfer time (t_2 to t_3 in Fig. 4) for various values of R_2. When capacitor C_x has reached its negative peak voltage, current stops flowing through it and thyristor TH_x turns off. The dipole current discharges through resistor R_2 and diode D_2 exponentially. Resistor R_2 forces a rapid magnetic field decay; it is adjustable in steps to have values of 1, 0.5, 0.25, and 0.125 Ω to produce L/R time constants of 0.016, 0.032, 0.064, and 0.128 s respectively.

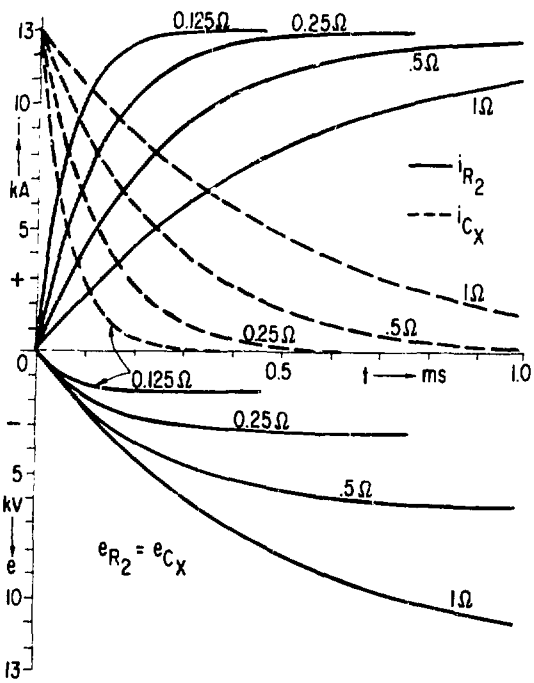

Fig. 5. Current and Voltage During Transfer of Current From Capacitor C_x Into Crowbar Resistor R_2 for Various Values of R_2.

<u>Thyristor Assemblies</u>

The heart of the 169 MW switching circuit is the thyristor assemblies TH_1 and TH_X, each comprising 90 silicon controlled rectifiers rated 800 A_{ave}, 1260 A_{rms}, 3100 V. These thyristors are arranged in 10 parallel modules, each having nine thyristors in series. The thyristors of each module have been selected to have only a small difference in recovery charge when they turn off. Figure 6 is a picture of one assembly.

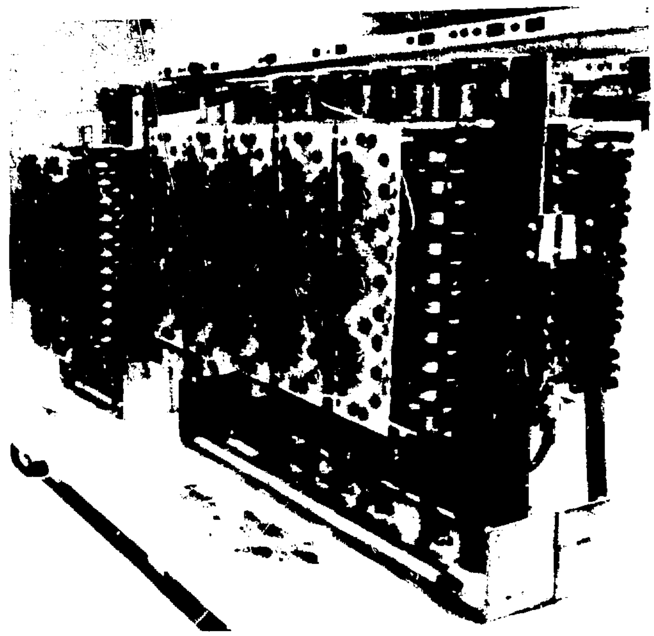

Fig. 6. Thyristor and Diode Assembly

One "C" core assembly located at the bottom of each module, and wired as shown in Fig. 7, assists in forcing equal current sharing among the ten modules.

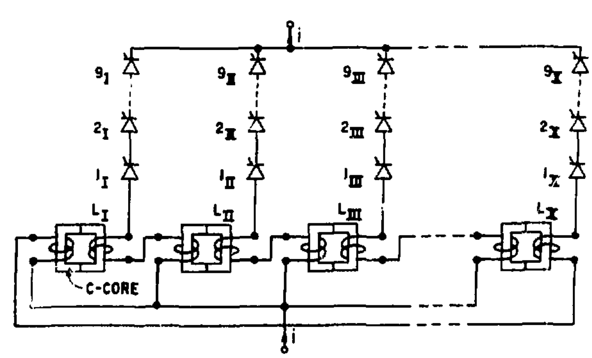

Fig. 7. Wiring of C-Cores

Also shown in Fig. 6 are the voltage-grading circuits in parallel with each thyristor, the water-cooled heat sinks, and the water header. In the rear of the picture is shown the diode assembly D_2 comprising 44 diodes, each rated 1600 A_{ave}, 2400 V. They are arranged in four parallel modules of 11 diodes in series. Each diode has connected in parallel dc and ac voltage-grading circuits, comprising a 50 kΩ 120 W resistor for dc, and a 75 Ω 15 W resistor in series with a 0.15 μF 1760 V capacitor for ac.

In order to limit the total number of thyristors (and thyristor trigger circuits) to 180 and to minimize the cost of the assemblies, high power 60 Hz thyristors were selected. The high current and high voltage rating of these relatively low-cost devices comes at the expense of slow turn off times (typically 250 μs vs 25 μs for more expensive inverter type thyristors). This requires a powerful turn-off circuit which is provided by the 500 μF capacitor bank C_x charged to < 13 kV (< 42 kJ) in conjunction with inductor L_x = 80 μH.

Thyristor Firing Circuits

Because nonsimultaneous firing of the thyristors might produce dangerous turn-on overvoltages, the firing system for the 13 kV thyristor assembly TH_x must satisfy the following requirements:

- The gate signal must be at least equal to four times the minimum gate turn-on current (> 4 x 0.15 A > 0.6 A).
- The rise time of the gate current must be less than 0.4 μs.
- The time difference (jitter) among the gate-current pulses must be less than 0.2 μs to minimize the delay between the first and the last thyristor turned on in a string of nine.
- The gate-current pulse must last for at least 50 μs and must not exceed the power rating of the thyristor gate.
- The firing circuit must be fail-safe.

The above requirements are met by furnishing gate signals by means of a primary cable threaded through torroidal tape-wound cores on which are placed secondary windings supplying the gates of each of the ninety thyristors of an assembly. As illustrated by Fig. 8, the secondaries of one core provide signals to one thyristor in each of the ten parallel connected thyristor modules. In this way, all the secondaries of a core are nominally at the same potential to ground; this potential varies from 1.44 to 13 kV in nine steps of 1.44 kV. The pulse shaping network of Fig. 9 gives a rise time of 200 μs without requiring good high frequency characteristics from the transformer circuit. These networks are mounted close to each thyristor, as shown in Fig. 10. By adjusting resistor R_1, the time constant $R_1 C_1$ can be varied, and with it the time when capacitor C_1 reaches the zener voltage of D_2 which initiates a gate pulse by triggering SCR_1. Resistor R_1 also helps to force current sharing between the secondary windings. Resistor R_1 and capacitor C_1 act not only as a delay circuit to time and to sharpen the gate pulse, but also as a noise suppressor to the gates that are connected in parallel through the common transformer core. The parallel connection of C_2 and R_2 forces a high initial peak current (via C_2) followed by a lower gate current (determined mainly by R_2). Resistor R_3 connects the cathode to the gate and resistor R_4 is the means for measuring the gate current. Diode D_3 assures that the gate will not get biased negatively and diode D_1 provides a path for a sinusoidal relatively low frequency core reset current pulse. The toroidal transformer cores use 2-mil grain oriented silicon steel. They are Arnold Engr. type T5581. Each secondary has three turns. For fail-safe operation, two

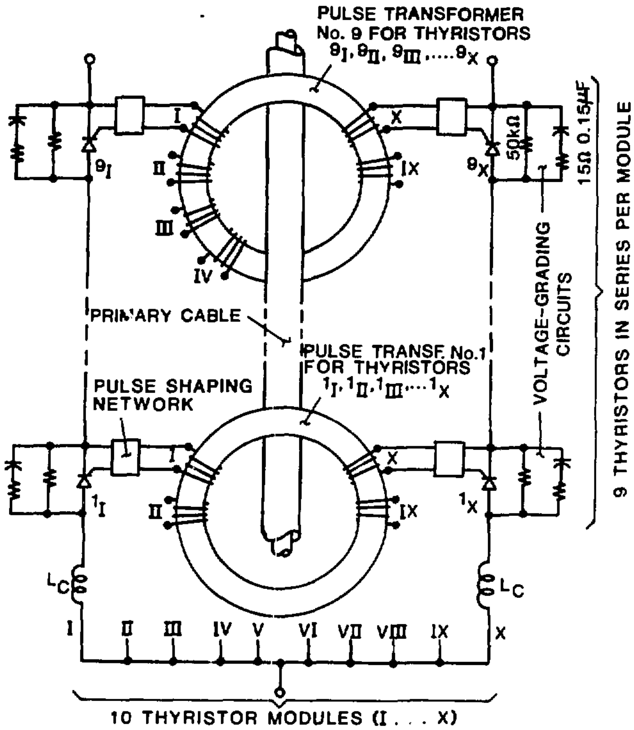

Fig. 8. Diagram of Thyristor Pulse Transformer Operation

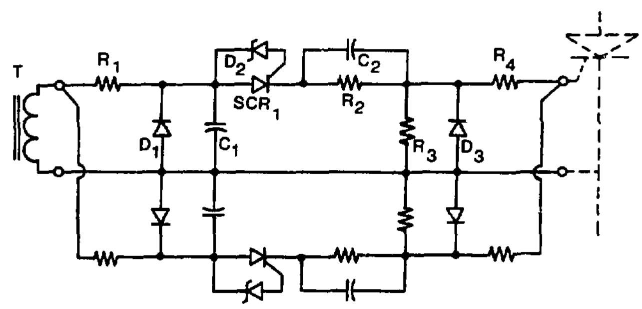

Fig. 9. Thyristor Pulse Shaping Network

identical pulse shaping networks have been provided for each thyristor gate. They operate in parallel and the leading edge of their gate pulses have been adjusted, by adjusting R_1, to be within < 100 ns.

As shown in Fig. 8, each thyristor is shunted by a voltage-grading circuit that equalizes the voltage across the nine thyristors caused by nonsimultaneous firing or different leakage currents. The dc grading resistor is 50 kΩ. The transient grading circuit consists of a 15 Ω resistor connected in series with 0.15 μF (τ = 2.25 μs); the 0.16 J charge stored at 1.4 kV on the 0.15 μF capacitor aids in keeping the fastest thyristor turned on while the slower ones are turning on.

The primary cable pulse is generated by discharging an extended-foil capacitor bank of C_1 = 80 μF from 350 V when thyristor S_2 in Fig. 11 is turned on. Time delay reactor L_2 limits the discharge current for 2 μs. The pulse transformer cores and reactor L_2 are reset when capacitor C_1 is recharged via the primary cable by a sinusoidal current pulse of opposite direction when thyristor S_1 is turned on.

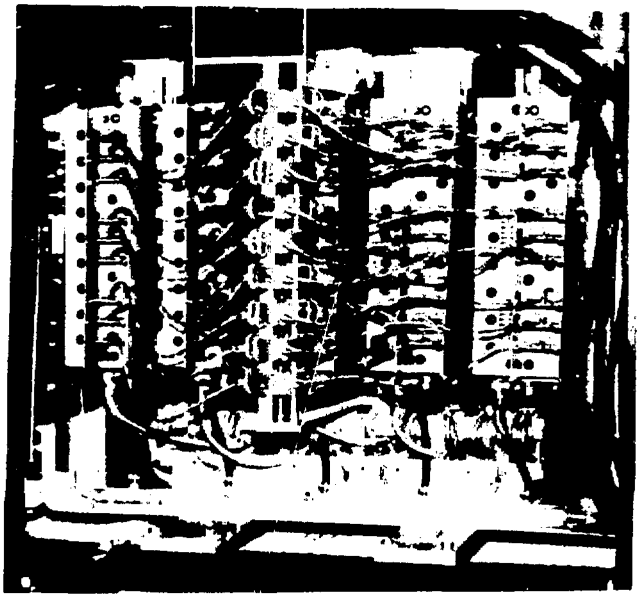

Fig. 10. Thyristor and Pulse Transformer Assembly

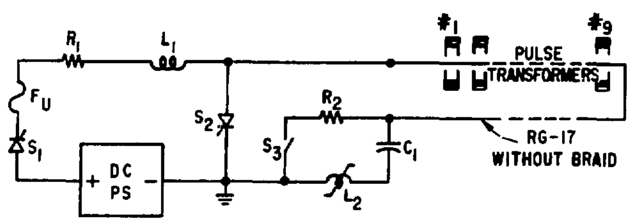

Fig. 11. Thyristor Firing Circuit

Thyristor Protection

It is essential that all ten parallel connected thyristor modules of TH_1 turn on and stay on when they are gated on in the presence of a forward voltage of only ~ 500 V dc. Turn on of each module is monitored by threading the cable of its C-core winding through the center of a torroidal ferrite core. The core has a cross section 1/4" x 1/2" with an I.D. of 2". It is glued to a 3 1/2" long nylon tube of 1 15/16" OD, and 1" ID, which gives HV insulation. The ferrite core has one radial slit 1/16" wide to accomodate a Linear Output Hall-effect transducer type 91SS12-2 of Micro Switch. This inexpensive transducer has a span -400 G to +400 G, a null offset at 0 G of 6 V, a sensitivity of 7.5 mV/G and ±1.5% linearity. The output of the transducer is compared to a reference voltage at a fixed point during the current rise. If all transducer outputs are above the reference level, operation continues. If a module has not turned on, its transducer level is below its reference, this fact, via logic circuits, initiates a power supply shutdown. A similar circuit is employed for TH_x. During low level operation (≤ 500 G, ≤ 1300 A, ≤ 130A/module) occasionally one module of TH_1 fails to turn on, however, in this case it can be tolerated because two modules out of the ten could handle such relatively small currents.

Inductor L_x

For turn-off inductor L_x = 80 µH, a foil-wound construction with an air core was chosen as shown in Fig. 12. This design has the advantages of:

- *being extremely rugged;*
- being easy to wind; and
- having a constant turn-to-turn voltage gradient.

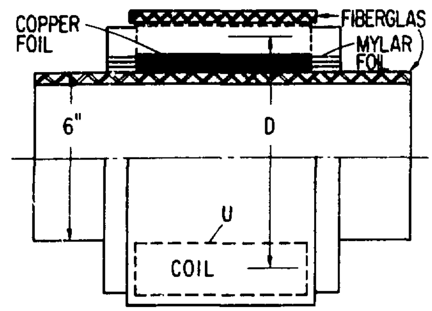

Fig. 12. Foil-Wound 80 µH Turn-Off Inductor

The inductor was wound on a fiberglass cylinder of 6" OD using 6" wide copper foil 0.020" thick with rounded foil edges. For turn insulation, two layers of mylar foil 0.014" x 8" was employed. The coil terminals are copper pieces 1/4" x 2" x 12" long with rounded corners. For a cylindrical coil, the inductance in µH is:

$$L = 1.05\ D\ n^2 \left(\frac{D}{U}\right)^{3/4} \qquad (5)$$

for D/U < 1, and

$$L = 1.05\ D\ n^2 \left(\frac{D}{U}\right)^{1/2} \qquad (6)$$

for 1 < D < 2.5,

where

n = number of turns

D = (ID + OD)/2 (mean diameter) in meters

U = circumference of coil in meters.

With n = 27 turns, we have D = 0.177 m, D/U = 0.5 resulting in an inductance of 80.9 µH. The turn insulation is exposed to 13 kV/27 turns = 481 V/turn. A fiberglass jacket 1/4" thick contains the magnetic forces. The coil assembly was vacuum impregnated with epoxy resin.

Capacitor Bank C_1

The 6000 µF, 930 V, capacitor bank serves two purposes. First, it provides a low impedance path for the turn-off current for thyristor assembly TH_1. Secondly, it absorbs the energy stored in the wiring inductance of the dc power supply when its current of 13 kA decays to zero in approximately 82 µs at a rate of ≤ 162 A/µs. Capacitor C_1 and the dipole coils would resonate at 16 Hz; diode D_1 prevents this. Resistor R_1, rated 150 Ω, 2 kW, discharges C_1 with a time constant of 0.9 s between pulses.

Discharge Resistor R_2 for Dipole Coils

The energy of 1.35 MJ stored in the dipole coils is discharged into a water-cooled high voltage (HV) resistor bank that can be adjusted in steps to have values of 1, 0.5, 0.25, and 0.125 Ω. To keep the cost and circuit inductance relatively low, the resistors were made up from 0.85 Ω modules as shown in Fig. 13.

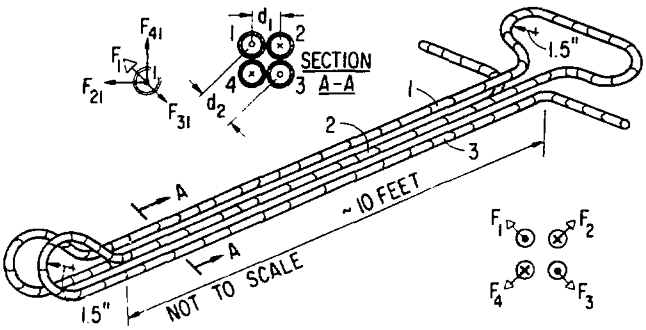

Fig. 13. Low Inductance HV Water Cooled Resistor Module

Each module is built from four commercially available 12-ft-long stainless steel tubes of 3/8" OD and 0.020" wall thickness. The four tubes are arranged side-by-side and connected in series as shown in Fig. 13. By having the current flowing in opposite directions in adjacent tubes, the magnetic forces partially cancel and the net force on each tube is outward. These forces can be estimated from:

$$F = \frac{\mu}{2\pi} \frac{l}{d} I^2 \qquad (7)$$

where

$\mu = 0.126 \times 10^{-6}$ kg/A^2

l = length of tube

d = separation of tubes

I = current A

For example in Fig. 13 are illustrated the forces exerted on tube 1 by the currents flowing in tubes 2, 3, and 4. The modules of 0.85 Ω which make up the resistance networks carry a peak current of 3.25 kA when they are connected for 1 Ω. This results in a net force of 0.14 kg/cm = 0.78 lbs/in. for each tube, directed outward as shown in Fig. 13. By insulating the tubes with sheets of mylar for ~ 30 kV, the tube separation is small and with it the inductance of the module. The L/R time constant of a resistor module is a few μs. Fig. 14 is a picture of the resistor bank which is located in a tunnel below the switching circuit cubicle.

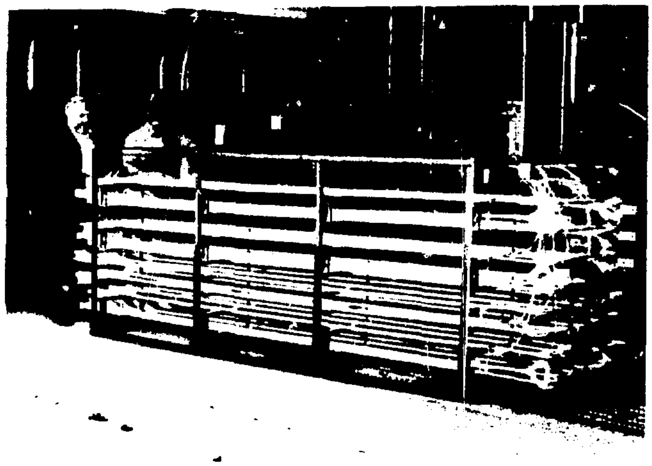

Fig. 14 Dipole Discharge Resistor Bank

Acknowledgment

I am grateful to Don McGhee for assemblying and testing the switching circuit. He also designed and constructed the 2.75 MW and 5.5 MW dc power supplies including their monitoring and control circuits. The thyristor and diode assemblies were built by International Rectifier to ANL specifications.

References

[1] W. Praeg, et al, "FELIX: Construction and Testing of a Facility to Study Electromagnetic Effects for First Wall, Blanket and Shield Systems," Proceedings of the 10th Symposium on Fusion Engineering, Philadelphia, PA, Dec. 1983.