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AN ISOLATED DATA ACQUISITION SYSTEM FOR HIGH VOLTAGE APPLICATIONS*

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AN ISOLATED DATA ACQUISITION SYSTEM FOR HIGH VOLTAGE APPLICATIONS

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Abstract: This report describes the design and operation of a microcomputer controlled system for acquisition of both analog and binary data within the high voltage stages of a linac modulator. The system is comprised of a microprocessor Controller which communicates with the remote data Acquisition circuits via an optical bus. The bus, which uses a 1 MHz Manchester II format, is configured as a loop, starting at the Controller, daisy-chaining the remote cards and terminating back at the Controller. Upon receiving a linac timing pulse, the Controller sends addressed commands to the individual remote cards and receives data back. It then passes this data to the linac control system through a Multibus connection. Each remote circuit can return 16 binary sense and 7 (12 bit) analog parameters within 270 us. This speed is possible because of a pipelined design where one word is transmitted while another is being converted. A data conversion cycle is initiated when a remote data acquisition card receives the proper command and address from the controller.

Introduction

Before the advent of low cost high precision fiber optics, the only practical way of taking measurements of transient signals from inside of Fermilab's multi-deck linac modulators was to use transformer coupling. Aside from the disadvantages of cost and size of transformers there is always the danger of a tube generated spark jumping across and destroying measurement equipment.

The system that we are describing circumvents these problems by employing fiber optic links to transmit data from high voltage modulator decks to the linac control system at ground potential. The system is capable of making both analog and binary (e.g. fuse intact or blown) measurements for diagnostic purposes. The measurements are of the following parameters; grid voltage, anode voltage, filament voltages, grid current, circuit breakers and fuses (binary sense).

Overview of System

The structure of the system is shown in fig. 1. The system is comprised of a microprocessor based Controller that gathers data from a number of remote data Acquisition circuits via light links. After the Controller has gathered its data, it transfers it to the Multibus based linac control system through a parallel connection to an I/O Multibus board. The Controller also outputs the systems status and a portion of the data to its front panel so the system can be monitored directly. In addition to these ports, the Controller board has a serial port for communication via video terminal. This feature will be used for setup and adjustment of the system.

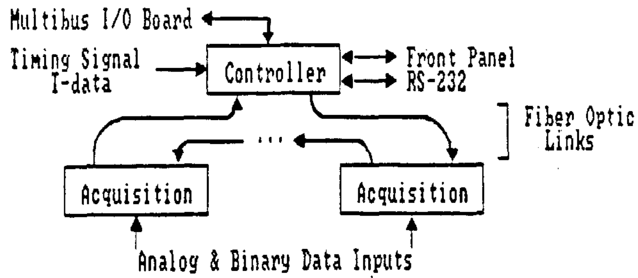

Fig.1 Isolated Data Acquisition System

The light link daisy-chains from the Controller through all the remote data Acquisition circuits and back to the Controller. The 16 bit Manchester II serial word format used on the light link is adapted from the MIL-1553 bus standard. Words originating from the Controller are command words while those originating at the Acquisition circuits are data words. The difference between these two word types can be seen in fig. 2. The system can have up to seven Acquisition circuits, each with the capability of gathering one 16 bit binary status, and seven 12 bit analog parameters.

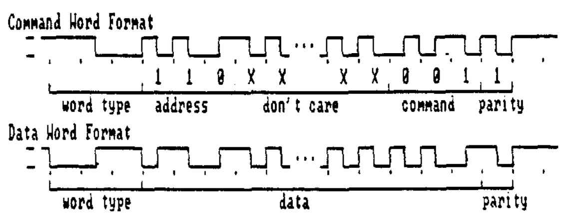

Fig. 2 Example Command and Data Words

The entire system operates at a 15 Hz cycle rate. The cycle is initiated when the Controller receives a linac timing pulse, T_data. This is sent through the light link to latch all the analog sample and holds and the binary latches in the Acquisition circuits. This pulse also interrupts the processor in the Controller circuit which then sends out addressed commands for each Acquisition circuit to convert and transmit its data. Each Acquisition circuit responds to its addressed commands by sequentially converting (for analog data) and transmitting data down to the Controller. Once the Controller has received and stored the data, it rests all the Acquisition circuit's latches, and sample and holds by sending a globally addressed reset command. The Controller next waits for requests for data from the Multibus I/O connection. After the Controller has transferred its data to the linac control system, it outputs the specified data to the front panel and updates the status indicators. After this the Controller services any requests from the serial port, otherwise it waits for the beginning of the next cycle.

Description of Controller

A block diagram of the Controller is shown in fig. 3. The heart of the Controller is its microcontroller, the Hitachi HD63P01, (similar to the Motorola 68Ø1). There are three functional areas that make up the Controller board; the fiber optic, multibus and diagnostic/setup interfaces.

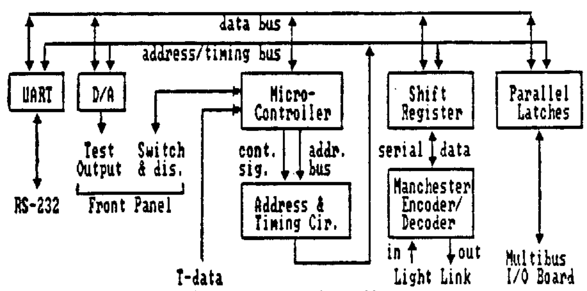

Fig. 3 Block Diagram of Controller

The fiber optic interface consists of the shift register, and the Manchester encoder/decoder. The microcontroller transmitts a command to the Acquisition circuits by writing the command word to the shift register. This automatically initiates the encoding and transmission of the command word by the Manchester encoder/decoder, (Harris HD64Ø8). The command word, in MIL-1553 format, then propagates through all the remote data Acquisition boards and is received and decoded back at the Controller. Since the command word has a parity bit, (see figure 2), it can be checked for both Manchester and parity errors when it is received back at the Controller. This allows the Controller to take corrective measures if a command word was altered by noise.

As a command word propagates through the daisy-chain connected Acquisition boards, it is received and decoded by all the Acquisition circuits. If the appropriate Acquisition circuit is going to send data back to the Controller, it breaks its daisy-chain repeater connection and drives the light link with its own data words. These data words propagate through the remainder of the daisy-chain and are received by the Controller. The data words do not affect any other remote Acquisition circuits that they pass through because their format differs from that of command words (see fig. 2).

The fields of the command word are shown in fig. 2. The three most significant bits of the command word specify the address of the Acquisition circuit targeted to receive the command. Addresses Ø to 6 are available for individual Acquisition circuits where address 7 is reserved as a global address for all Acquisition circuits.

The three least significant bits of the command word are used to specify the command. Only three commands are specified in the present system. These commands are: Return Configuration, Convert Data, and Reset Sample and Holds. The Return Configuration command is used by the Controller when the system is first powered up, or when it is reset. This command causes the addressed Acquisition circuit to return a data word that defines how many binary words, (Ø or 1), and how many analog words, (Ø to 7), that card was set to gather. This information is used by the microcontroller to build a table of appropriate size in memory for storage of data received from that Acquisition circuit. The Convert Data command just tells the addressed Acquisition circuit to convert, if necessary, and transmit its data down the the Controller. The Reset Sample and Holds command is used with the global address to reset all the Acquisition cards in the system for a new data gathering cycle.

The Multibus interface of the Controller consists of the parallel latches in fig. 3. This interface consists of three byte wide latches; two output and one input. The input byte is used to indicate to the Controller which data acquisition system and what channel in the system is being addressed. It also has a strobe line, which tells the Controller to check the current data on the input latch. If the Controller recognizes its address, it looks up the requested channel in memory and outputs the 16 bit data word to the two output latches.

The last functional areas of the Controller are the diagnostic and setup interfaces. The diagnostic interface consists of the front panel and the D/A. The front panel indicates both the status of the system, (eg. fiber optic loop open or closed), and also what channel is currently being output through the D/A. The diagnostics interface is the UART in fig. 3, which allows a technician to operate the system by itself for purposes of adjustment and testing.

Description of Acquisition Circuit

A block diagram of the remote data Acquisition circuit is shown in fig. 4. This circuit uses a logic sequencer, the Signetics 8251Ø5 FPLS, for its control. The job of the logic sequencer is to monitor the commands on the serial fiber optic bus and to respond appropriately if the address matches its own, and the command is valid. The Acquisition circuit has two functional areas; the fiber optic interface, and the data input and conversion section.

The fiber optic interface consists of the shift registers, Manchester encoder/decoder, and MUX. As a command word is received from the light link input, it is simultaneously decoded by the Manchester encoder/decoder and directed through the MUX out onto the light link output. Thus, the command word propagates through all the Acquisition circuits. If the received command's address

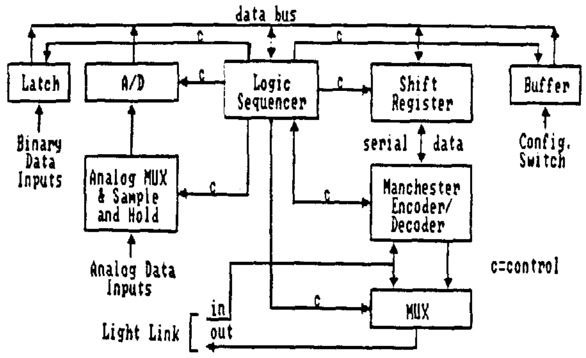

Fig. 4 Block Diagram of Remote Acquisition Circuit

matches that of the Acquisition circuit, it will be executed by that Acquisition circuit. As stated above, the Acquisition circuit has a repertoire of three commands, Return Configuration, Convert Data, and Reset Sample and Holds. If the Acquisition circuit receives a Return Configuration command the logic sequencer switches the MUX so the Manchester encoder/decoder is driving the light link. It then gates the setting of the configuration switches through the buffer and into the shift register. Next, it enables the Manchester encoder. The configuration information is transmitted through the light link back to the Controller. Finally, the logic sequencer switches the MUX back and returns to the wait state.

The Convert Data command causes the logic sequencer to switch the MUX as above. It then transfers the binary input data in the latch to the shift register. Next, it simultaneously enables the Manchester encoder to transmit this data while driving the A/D converter through one conversion cycle to get the first analog data word. The binary word is transmitted first because it requires no time for conversion. At the end of the transmission of the binary data word, the logic sequencer transfers the first analog data word to the shift register. It then repeats the above process of transmitting one word while converting the next for the remainder of the analog data. After this pipelined transmission/conversion process is complete, the logic sequencer then restores the MUX and goes into a wait state as before.

The last command that the Acquisition circuit is capable of executing is the Reset Sample and Hold command. This is executed by the logic sequencer by enabling the sample and holds and the latch, and then waiting for a trigger from the Controller. Since this command is globally addressed, all Acquisition circuits enter this wait for trigger state together. The trigger is a 3 us pulse sent through the light link by the Controller at the start of a data gathering cycle. After the Acquisition circuits receive the trigger, they latch their sample and holds, and registers. Finally, they return to their wait states.

Closing Comments

A prototype of this system has been built and tested in an operating modulator. The system worked flawlessly even while tubes sparked inside the modulator. The circuits for this system will be assembled this summer and installed if Fermilab's linac in the Fall.

Acknowledgments

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