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Readout and Triggering of the Soudan 2 Nucleon Decay Experiment

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The readout and triggering electronics for the Soudan 2 proton decay detector is characterized by its versatility and the large number of identical channels. The versatility will enable one to trigger on many types of events, even unexpected phenomena, and the large number of channels gives very cheap unit prices. There will be a total of ~50,000 preamps for the anode and cathode signals. These will be bussed in groups of 8, giving 6144 channels for pulse height digitization and triggering. This electronics is packaged with 16 channels on each ADC card in Multibus® format crates.

Practically all the electronics is implemented in CMOS to save space and power. The timing and triggering logic on each card are implemented by CMOS semi-custom gate arrays with approximately 1100 gates/chip. Each channel will have an receiver amplifier followed by a 6-bit flash ADC (RCA 3300), the output of which is stored every 200 ns in a 1K deep circular memory buffer.

A highly flexible (software controllable) triggering scheme has been designed. Each receiver amplifier signal is discriminated and the 16 signals on one ADC card are continuously examined for programmable trigger conditions. One condition is to find the maximum adjacency of the 16 channels having a signal, i.e. how many in a row are on, and comparing this with a software-settable threshold. The second condition is to determine the multiplicity of the channels, i.e. the total number that are on, to compare to two different programmable thresholds. This will be implemented with "rolling eights", which means that on each card two of these sets of comparisons are made. One is simply for the 16 channels on that card while the other is for the top eight channels on that card added to the bottom eight channels of the previous card. This chain continues across all 16 channels in the crate, thus producing a uniform triggering efficiency even across card boundaries.

In addition, there is on each ADC card an empty socket, to which all the raw triggering information comes, in which a future CMOS gate array chip could be put to produce other kinds of triggers. Three "trigger request" lines come from each of 24 Multibus crates to a trigger processor crate which will decide (on the scale of < 50 μsec) whether to trigger the readout of the stored data for the whole detector. The trigger processor crate will be controlled by an Intel 8086 microprocessor card which also can make high level trigger decisions on the time scale of tens of milliseconds.

Each of the data crates is controlled by an Intel 8086 CPU card which manages a data-compactor card. When a trigger is generated by the trigger processor, the CPU reads a status word from each data card to determine which channels have data. The CPU then directs the compactor to compact only those channels. The compaction process passes only those data words with pulse height above a programmable threshold, and stores them in a 4K deep FIFO along with their addresses. This FIFO can either be read out directly to the host computer via CAMAC, or its contents can be preprocessed by the 8086 before sending it to the host. Typical readout dead times of less than 30 msec are expected. Each of the 24 8086 CPU's can communicate with the host either through CAMAC, which is used to have the 8086 reconfigure the trigger or perform tests, or through an RS-232 port, which is used for downloading programs or for connecting a terminal to the 8086.

We have built and operated ~ 200 channels of prototype electronics to read out a test module of the real detector. The design of the electronics for the final system is complete and orders have been placed for the CMOS gate arrays and the multilayer printed circuit boards. We expect to have the first of the readout systems by spring 1985.

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