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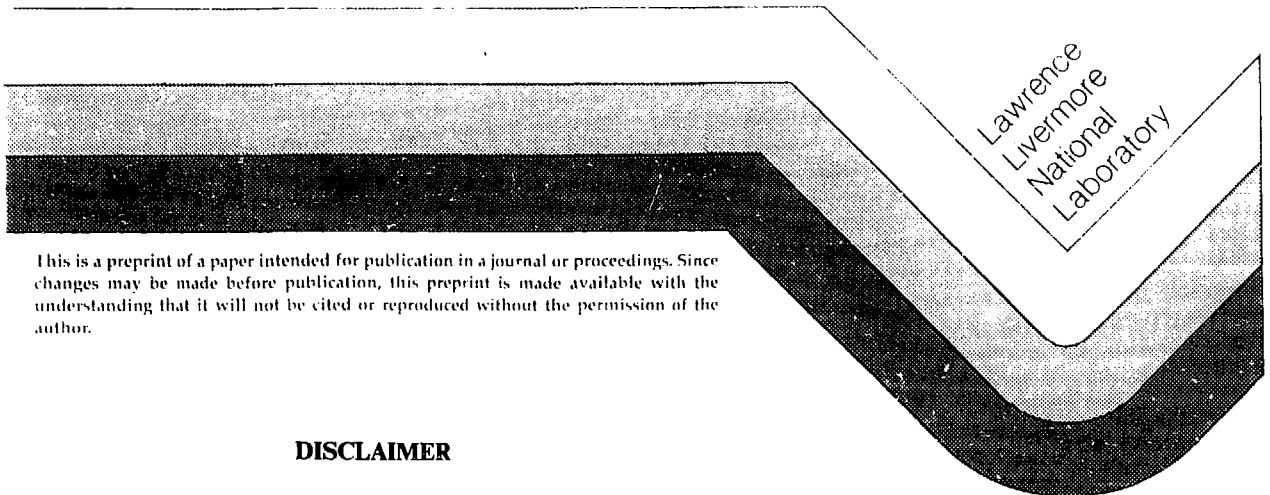
UCRL--92257

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DE86 012339

This paper was prepared for submittal to  
Second International VLSI Multilevel  
Interconnection Conference,  
Santa Clara, CA  
June 24-26, 1985

May 1985



Lawrence  
Livermore  
National  
Laboratory

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# PULSED LASER PLANARIZATION OF METAL FILMS FOR MULTILEVEL INTERCONNECTS\*

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## ABSTRACT

Multilevel interconnect schemes for integrated circuits generally require one or more planarization steps, in order to maintain an acceptably flat topography for lithography and thin-film step coverage on the higher levels. Traditional approaches have involved planarization of the interlevel insulation (dielectric) layers, either by spin-on application (e.g., polyimide), or by reflow (e.g., phosphosilicate glass). We have pursued an alternative approach, in which each metal level is melted (hence planarized) using a pulsed laser prior to patterning. Short ( $\sim 1\mu\text{s}$ ) pulses are used to preclude undesirable metallurgical reactions between the film, adhesion or barrier layer, and dielectric layer. Laser planarization of metals is particularly well suited to multilevel systems which include ground or power planes.

Results are presented for planarization of gold films on  $\text{SiO}_2$  dielectric layers using a flashlamp-pumped dye laser. The pulse duration is  $\sim 1\mu\text{s}$ , which allows the heat pulse to uniformly penetrate the gold while not penetrating substantially through the underlying  $\text{SiO}_2$  (hence not perturbing the lower levels of metal). Excellent planarization of the gold films is achieved (less than  $0.1\mu\text{m}$  surface roughness, even starting with extreme topographic variations), as well as improved conductivity. To demonstrate the process, numerous planarized two-layer structures (transmission lines under a ground plane) were fabricated and characterized.

\*This work was performed under the auspices of the U.S. Department of Energy by Lawrence Livermore National Laboratory under Contract No. W-7405-Eng-48.

†Supported by the Department of Energy, Office of Basic Energy Sciences.

## INTRODUCTION

The fabrication of multilevel VLSI circuits often requires the use of thin-film planarization procedures. The need is particularly acute when one attempts to achieve wafer-scale integration; an efficient, high-power wafer-scale integrated system might require four levels of interconnect *plus* two or more ground or power planes. The most severe topographic problems occur around stacked vias, where a connection extends from the bottom interconnect level to the top level.

Planarization techniques have traditionally involved smoothing the dielectric between the metal layers. For example, spinning on polyimide as the dielectric is often used to achieve planarity. Other dielectric planarization techniques use bias sputter-etching,<sup>[1]</sup> and still others use photoresist to planarize and then plasma back-etch to the underlying SiO<sub>2</sub>.<sup>[2]</sup> Yet another planarization technique uses a scanning cw laser to rapidly flow phosphosilicate glass.<sup>[3]</sup> None of these techniques will planarize a stacked (nested) via, because the dielectric must be removed from the contact area between each level, resulting in a large thickness deficiency at the via.

This work investigates a novel alternate approach to achieving planarity in multilevel systems: the planarization of the *metal* layers. The feasibility of planarizing metals by momentarily melting them is evident when one considers the very high surface tension (about 50 times that of most nonmetallic liquids) and relatively low viscosity (similar to water) of clean molten metals. One can calculate the time-dependent relaxation of low-amplitude, long-wavelength topographic variations in a molten metal surface by neglecting inertial effects (the Reynolds number is low under these conditions). Then it can easily be shown that the amplitude of a Fourier component of spatial period  $L$  will decay exponentially with a time constant of

$$\tau = \frac{3\mu L^4}{16\pi^4 \gamma h^3} \quad (1)$$

where  $\mu$ ,  $\gamma$ , and  $h$  are the dynamic viscosity, surface tension, and thickness of the molten metal. For gold<sup>[4]</sup>,  $\gamma=1130$  ergs/cm<sup>2</sup>; experimental data on its viscosity is unavailable so we shall use the value for silver, i.e.  $\mu \approx 0.03$  poise.<sup>[5]</sup> Thus in only 1 microsecond, all Fourier components of the surface topography in molten gold with periods shorter than approximately 21  $\mu\text{m}$  will be virtually eliminated. Since most VLSI structures of interest are much smaller than that, this would be quite sufficient planarization. If the duration of the melt is much longer than 1  $\mu\text{s}$ , one may induce unacceptable metallurgical reactions in the thin films. For example, molten aluminum will reduce an SiO<sub>2</sub> dielectric to form silicon in a few seconds.<sup>[6]</sup> As another example, we estimate (based on typical diffusivities in molten metals<sup>[7]</sup>) that 1  $\mu\text{m}$  of molten gold will completely alloy with a titanium adhesion layer in about 1 ms.

The above discussion suggests that a very fast (microsecond) heat pulse is optimal for planarizing metals. Initial experimental feasibility of this idea was demonstrated in 1984 by unpublished work of the author with R. F. W. Pease and G. Yoffe of Stanford University. In that work, a high-power scanning electron beam was used to melt an aluminum line sitting in a silica trench. Excellent silica wetting and partial aluminum planarization was clearly observed. However, rastering a fine

electron beam does not produce a perfectly flat surface, because not enough metal area is molten at one time. For this reason, in this work we have used a pulsed laser to melt a large area ( $4 \text{ mm}^2$ ) of metal with a single pulse.

It is instructive to contrast this approach with dielectric planarization techniques. The essential difference is that we require that the dielectric be capable of withstanding high temperatures (e.g.,  $\text{SiO}_2$ ), whereas the planarized metal has a moderate melting point (e.g., Au or Al). Conventional planarization processes often require just the opposite, i.e., a relatively low-temperature dielectric such as polyimide (for spin planarization) or phosphosilicate glass (for thermal planarization) is used with a moderate- or high-temperature metallurgy. Planarization of the metals seems more attractive because refractory dielectrics tend to be of higher quality (e.g., fewer pinholes, greater dielectric strength and higher reliability). Furthermore, for metal interconnect levels, the compelling need is for electrical continuity of the fine wires, and this is easier to achieve with a non-refractory material, which would generally have a high surface mobility at the deposition temperature. Moreover the problem of filling stacked vias is avoided because the planarized metal would be correspondingly thicker over the via area. Note that it may be practical to design a multilevel interconnect process which uses both the laser planarization of metal described in this paper and *also* a dielectric planarization process, to obtain a fully planar interconnect structure.

## PROCESS DESIGN

The use of laser planarization of metal films imposes some constraints on the choice of metals and dielectrics. The molten metal must wet the dielectric; this seems to occur if and only if the solid metal has good adhesion to the underlying dielectric. For example, gold films deposited directly on  $\text{SiO}_2$  do not adhere well, and correspondingly molten gold does not wet  $\text{SiO}_2$  (contact angle of  $140^\circ$ ).<sup>[8]</sup> In contrast, the customary use of an oxygen-active metal as an adhesion layer (e.g., Cr, Nb, Ti, or  $\text{Ti}_{0.1}\text{W}_{0.9}$  alloy) gives good adhesion when the gold is solid, and correspondingly excellent wetting in the liquid phase. Aluminum films deposited directly onto  $\text{SiO}_2$  adhere in the solid phase and wet well in the liquid phase.

In addition to having good adhesion, the metal film should be able to absorb a significant amount of the incident optical power. For this reason, highly reflective metals such as aluminum or silver are more difficult (but not impossible) to work with than gold; the latter has greater than 50% absorbance in the green or blue. The problem with highly reflective metals is not the energy requirement (one can simply increase the incident flux). Rather, it is the fact that when reflectivity is near unity, then seemingly small changes in surface texture, topography, and composition can radically alter the absorbed power. This can lead to instabilities, in which excess absorbed heat modifies the surface in such a way as to further reduce the reflectance, causing still more optical absorption, until the film is vaporized. (One might overcoat such metal films with a thin absorbing layer; this has not yet been tried).

Based on the above considerations, we concluded that gold was an ideal candidate for laser planarization, so most of our experiments were conducted with that metal, although aluminum was briefly tested because of its wide usage in industry.

Having chosen the metal, one must then choose the dielectric. It is essential that the dielectric not be damaged by momentary exposure to the overlying molten metal. This presumably rules out organics such as polyimide. We used pure SiO<sub>2</sub>, mainly because its physical properties are desirable and well characterized. For the Au/SiO<sub>2</sub> multilevel system, an adhesion layer such as Cr is necessary at every interface between the two materials.

Once the metal/dielectric system is chosen, the heat pulse can then be optimized. The optical absorption depth in Au or Al is so short (200 Å at typical wavelengths) that we can consider the heat to be generated at the surface of the metal film. The heat will diffuse a depth  $z=(\alpha t)^{1/2}$  in time  $t$ , where  $\alpha$  is the thermal diffusivity of the gold (1.0 cm<sup>2</sup>/s at 700°C). It therefore takes only 10 ns for most of the heat to penetrate through a micron of gold. As discussed above, a somewhat longer pulse width is desirable in order to allow sufficient metal flow over, say, a 20 μm spatial period. For a 1 μs heat pulse, the gold may be considered to be nearly in thermal equilibrium during the pulse (relatively small vertical temperature gradients). The underlying SiO<sub>2</sub> dielectric has a much lower thermal diffusivity:  $\alpha=0.032$  cm<sup>2</sup>/sec. This is useful for two reasons: the underlying layers are exposed to much lower temperatures than is the surface, and the pulse energy required to achieve complete melting is minimized. Computer calculations were performed to determine the minimum absorbed energy needed to melt 1 μm of Au on top of a 1 μm SiO<sub>2</sub> layer on a silicon wafer. The energy requirements range from 0.4 J/cm<sup>2</sup> at 10 ns pulse duration, rising gradually to 0.8 J/cm<sup>2</sup> for a 1 μs pulse, and thereafter increasing approximately as the square root of the pulse duration (due to heat penetration into the silicon substrate). A pulse shorter than 10 ns would not be useful, because large thermal gradients would be generated in the gold layer, vaporizing the surface before the bottom of the film reaches its melting point. For laboratory work these energies must be doubled to account for the ~50% reflectance of the gold. These energies are minimums; in practice one would operate at somewhat higher values to allow for cold spots in the beam. The laser planarization process for the Au/SiO<sub>2</sub> interconnect system has been calculated and experimentally verified to have a large operating window for pulse lengths of 1 μs. That is, energies can typically be increased a factor of 2 above the minimum values without significant film vaporization or damage.

## EXPERIMENTS

A linear flashlamp-pumped dye laser containing a coumarin dye supplied optical pulses at 504 nm, of which 48% is reflected by the gold films. The pulses had 1 μs duration (full width at half maximum), 150 mJ of energy, and 1 Hz repetition rate. The beam was focused to a 2 mm diameter spot on the wafer. No effort was made to make the spot uniform in intensity; consequently about half of the pulse energy (around the beam circumference) was below the melt threshold and hence wasted. X-Y translation stages were configured with stepping motors to translate the wafer between pulses; typically we spaced the pulses 1 mm apart. A more efficient and versatile arrangement would be to homogenize the beam using a "kaleidoscope"<sup>[9]</sup> or similar arrangement.

Experiments were mostly performed on sputter-deposited gold films on SiO<sub>2</sub>

dielectric layers. Initially the underlying substrates were bare silicon wafers. In later work we deposited a gold pattern ("metal level 1") with a pitch of 4, 8 or 16 microns onto thermally grown  $\text{SiO}_2$ , then coated the gold with a second  $\text{SiO}_2$  layer by chemical vapor deposition, and finally sputter-deposited an upper layer of gold ("metal level 2"). It is important to deposit suitable adhesion layers at the Au/ $\text{SiO}_2$  interfaces (e.g., Cr, Nb, or  $\text{Ti}_{0.1}\text{W}_{0.9}$ ) or else the structures will fail when pulsed with heat. The results of the planarization procedure are illustrated in Fig. 1. These structures are of particular interest to us, as they are microstrips (transmission lines covered by a ground plane). We see that laser planarization of metal level 2 had no apparent effect on the underlying metal level 1, due to the thermal barrier presented by the  $\text{SiO}_2$  dielectric layers. In principle this process could be repeated: coating with  $\text{SiO}_2$ , opening contact windows, coating with Au, laser planarizing, patterning the Au, coating with  $\text{SiO}_2$ , etc. After each level of Au is deposited, the planarity of the surface would be restored by laser planarization.

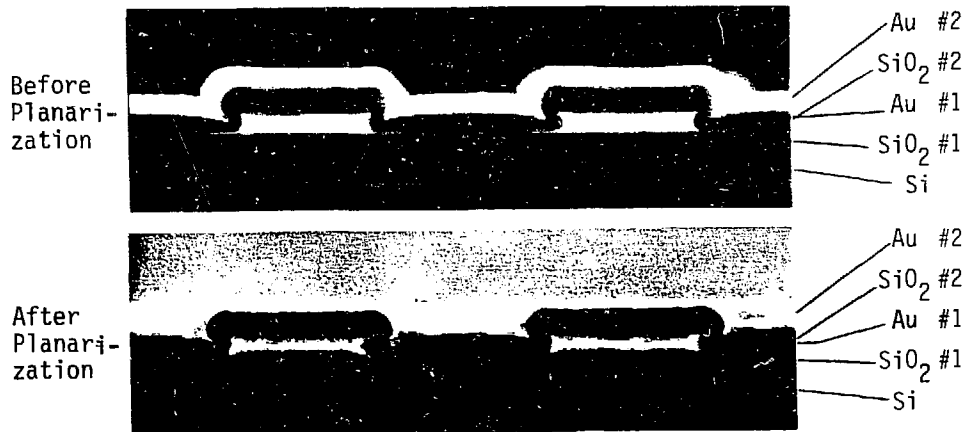


Fig. 1(a): Cross sections of 7- $\mu\text{m}$  wide, 1- $\mu\text{m}$  thick gold lines on 16  $\mu\text{m}$  centers, coated with 1  $\mu\text{m}$   $\text{SiO}_2$  and then a 1  $\mu\text{m}$  gold ground plane, before and after laser planarization.

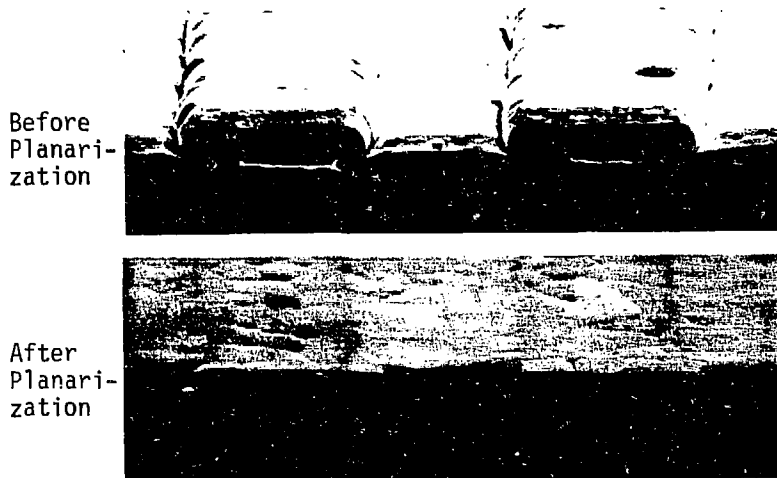
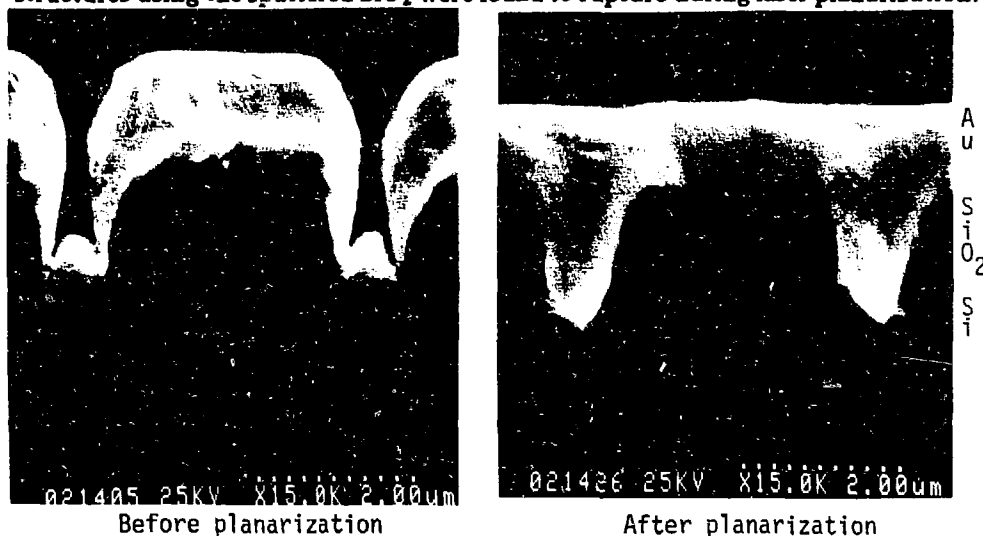


Fig. 1(b): Same as Fig. 1(a), except viewed from a 75° angle instead of 90°.

The wafers were exposed to ambient air during the planarization process; no adverse effects appear to be associated with this procedure. In the case of aluminum, which oxidizes easily, there might be reason to operate in an oxygen-free environment, but we obtained satisfactory results with aluminum without doing so. A few experiments were done using a Kr<sup>+</sup>F excimer laser as the pulse source, but the 10 ns pulse gave a substantially reduced operating window between melting and damage, compared with the factor of 2 window available with the 1 μs pulsed dye laser.

As is evident from Fig. 1, the planarization process was very successful. The CVD and sputtering processes used to deposit the SiO<sub>2</sub> and Au produced extreme step coverage problems, yet the planarized gold is smooth and flat to better than ±500 Å. No changes whatsoever were noticeable in the lower SiO<sub>2</sub> or gold layers. This indicates that the process should be readily adaptable to more levels of metal. The geometries shown were particularly challenging cases, for the gold in these examples was barely thick enough to cover the higher regions after the planarization had been accomplished. As shown in Equation 1, the difficulty of planarization (i.e., melt time required) varies as  $h^{-3}$ , where  $h$  is the metal film thickness. Thicker gold films flow much more easily; Fig. 2 shows an example of a single relatively thick (1.6 μm) gold film before and after planarization.

We found that the deposited dielectric layers must have low internal stress for the planarization process to be successful. For example, sputter-deposited SiO<sub>2</sub> tended to be much more highly stressed than CVD-deposited SiO<sub>2</sub>. Multilayer structures using the sputtered SiO<sub>2</sub> were found to rupture during laser planarization.



**Fig. 2:** Cross section of a silicon wafer which has been etched with vertical grooves, thermally oxidized with 0.4 μm SiO<sub>2</sub>, and coated with 1.6 μm of gold.

### PROPERTIES OF LASER-PLANARIZED GOLD FILMS

For designing a multilevel metal process, it is important to understand what physical changes (besides the obvious topographic ones) occur in the metal films

due to the laser planarization process. We have made extensive experimental studies of planarized gold films like those in Figs. 1 and 2.

One concern is whether the adhesion layer at the Au/SiO<sub>2</sub> interface diffuses significantly into the gold while the latter is molten. Using Secondary Ion Mass Spectroscopy (SIMS) depth profiling to study planarized gold samples having adhesion layers of Cr, Nb, and Ti<sub>0.1</sub>W<sub>0.9</sub>, no radical movement of any adhesion layer was observed. While it is difficult to draw quantitative conclusions from SIMS data, it appears that each type of adhesion layer exhibited a small amount of diffusion into the gold (i.e., a Gaussian-like impurity tail was observed penetrating up into the gold). The concentration levels appear to be in the parts per million when more than about 0.2 μm from the adhesion layer. The fastest diffuser was titanium, which produced a weak but measurable signal as far as 0.5 μm from the interface. The slowest diffuser was tungsten, which did not diffuse measurably into the gold. Since the diffusivities of impurities in molten metals are typically between 10<sup>-4</sup> and 10<sup>-5</sup> cm<sup>2</sup>/s at 1100°C,<sup>[7]</sup> this confirms that the gold could only have been molten for at most a few microseconds. None of these impurity levels are considered significant for multilevel interconnect purposes. The chemical etching properties of the gold appear unaffected by the planarization process.

No change in average thickness of the films was observed at normal power levels. Thus there is no significant vaporization of the films during planarization, even when the same area is pulsed repetitively.

The average grain size of the gold films increased substantially after laser planarization, from about 0.3 μm as-deposited to 1 or 2 μm after planarization (Fig. 1). However, this did not interfere with our ability to chemically etch the gold with edge roughnesses much less than a micron. In fact, the planarized gold is easier to pattern accurately because it is smoother than the sputtered films. We noted that the greater the incident optical pulse energy, the larger the grain size. We attribute this to the fact that these areas have more thermal energy stored in the substrate, hence the cooling time is longer, which allows more opportunity for grain growth before the temperature drops too low. Compared with sputter-deposited films, the texture is very smooth (100 Å roughness). X-ray diffraction showed that the planarized grains are oriented almost exclusively in the < 100 > direction, regardless of initial orientation (which was < 111 > for sputter deposition).

Adhesion of the planarized gold films is better than before planarization. In all cases we measured tensile strengths of greater than 5000 psi. In many cases the final failure occurred in the silicon substrate rather than the Au/SiO<sub>2</sub> interface.

The sheet resistance of the planarized films was determined by 4-point probing, and was found to be approximately 12% lower than before planarization. Typical room-temperature resistivities were 2.95 μΩ-cm before planarization, and 2.6 μΩ-cm after planarization. This is not far from the bulk value of 2.2 μΩ-cm, which would be the lowest possible value. Presumably this reduction in resistance is due to the larger grain size, which reduces electronic scattering.

All of the above physical properties appear to be independent of the number of pulses; i.e., there is no advantage or disadvantage to using multiple planarization pulses. The only defects which appear to result from laser planarization occurred in areas of poor adhesion, presumably where the SiO<sub>2</sub> substrate was contaminated



prior to the Au deposition. In such spots, the poor heat transfer results in overheating and vaporization of the spot, leaving a crater approximately 10  $\mu\text{m}$  in diameter. In addition to these defects, there is a visible artifact which occurs at the border of the melted area, presumably due to a slight difference in level between the planarized and unplanarized areas. This is typically very small (about 100  $\text{\AA}$ ).

## CONCLUSIONS

Laser planarization offers an attractive technique for fabricating multilevel interconnect structures, particularly where a number of ground or power planes are included. The Au/SiO<sub>2</sub> combination is well suited to laser planarization, although successful results were also achieved with the Al/SiO<sub>2</sub> combination. Two levels of metal have been demonstrated in this work. It appears that one can extend this process to circuits containing a large number of interconnect levels and ground/power planes by planarizing after each metal level is deposited. The technique can be used by itself, or it might be combined with a compatible dielectric planarization process to make truly planar multilevel interconnect structures.

## ACKNOWLEDGEMENTS

We would like to thank R. Fabian Pease, Mike Pocha and Irving Herman for their help in the early phases of this work. We also thank Rod Hyde for performing heat-flow computer calculations, Doug Phinney for the SIMS profiling and interpretation, Gordon Smith and Carol Weaver for the X-ray diffraction analysis, and Glenn Griggs and John Feikert for fabricating most of the coatings.

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