RAPID THERMAL ANNEALING OF PHOSPHORUS IMPLANTED SILICON

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Rapid thermal annealing (RTA) of phosphorus-implanted silicon has been investigated by four point probe, Van der Pauw methods and transmission electron microscopy. The results have been compared to furnace annealing. Experiments show that RTA, even at temperatures as low as 605°C, results in good electrical properties with little remnant damage and compares favourably with furnace annealing.

In this study RTAof low energy phosphorus-implanted (100) silicon has been studied as a function of various implantation conditions (dose and energy) and RTA temperatures. The RTA equipment used consisted of two quartz-iodide lamps (400 W and 500 W) and three aluminium mirrors. The sample was mounted on a quartz glass holder to improve uniformity of heating and decrease thermal conduction loss. The samples are 0.5-3.0 ohm-cm p-type (100) Si wafers implanted with 40 Kev and 80 Kev P_4^+ ions to doses of 1.25 x 10^{13}, 1.25 x 10^{14} and 0.625 x $10^{15}/cm^2$. The samples were all of the same thickness and cut to the same size, 6 x 6 mm^2. The temperature-time dependencies of the samples were measured on a control silicon wafer of the same dimensions with a Chromel-Alumel thermocouple bonded to it by an indium pellet contact. The uniformity of temperature on the sample is within 10%.

Each implanted sample was cut into several smaller pieces and those were annealed at a particular RTA temperature (605°C, 675°C, 750°C, 820°C, 900°C, 970°C, 1050°C or 1140°C). The annealing time for all samples was 15 seconds, and one sample was kept for furnace annealing under optimal condition (i.e. 550°C - 2 hours, 850°C - 15 minutes, 550°C - 2 hours) for comparison with those annealed by RTA. After annealing, sheet resistance and Hall effect measurements were performed by four-point probe and van der Pauw methods respectively. From the results, Hall mobility μ_H and average carrier concentration N_s were calculated. Transmission electron microscopy was carried out on some samples to study defects.

The electrical results for 80KeV, 1.25 x $10^{14}P_4^+/cm^2$ are summarised in Fig.1.

Rather surprisingly, the RTA temperatures as low as 605°C gave similarly good electrical properties to those annealed at higher temperatures. In addition, the results of RTA under various temperatures from 605°C to 1140°C are generally similar to those of the furnace annealing. We find that sheet resistance $R_\square$, is in the range 1000-1500 $\Omega/\square$, 180-230 $\Omega/\square$ and 60-110 $\Omega/\square$ for 1.25×10^{13}, 1.25×10^{14} and 0.625×10^{15} P_4^+/cm^2 implants respectively. Generally $R_\square$ for the 40 Kev samples is higher than that of the 80Kev samples due to the very thin implanted layer. In general high carrier concentration corresponds to low mobility. In addition, the carrier concentration of 1.25×10^{15} P_4^+/cm^2 samples are almost the same as those of fully activated 1.25×10^{14} P_4^+/cm^2 samples. These incomplete electrical activities of $1.25 \times 10^{15}/cm^2$ samples may be attributed to exceeding 3×10^{20} carriers/cm^3 which is normally taken as the maximum equilibrium limit for n-type dopants in silicon.

TEM micrographs of 80 heV implanted samples were taken after 605°C RTA, 1140°C RTA, and furnace annealing. Small (10nm or less) loops and clusters can be seen in the $1.25 \times 10^{13}/cm^2$ RTA samples and in all the $.625 \times 10^{15}/cm^2$ samples. In the $1.25 \times 10^{14}/cm^2$ samples some large (40-80 nm) loops are also visible. It may be noted that no defects as such are seen in the $1.25 \times 10^{13}/cm^2$ furnace annealed sample, although background granularity suggests lack of complete crystalline perfection. An example of typical TEM results is given in Fig.2.

These experimental results indicate that RTA temperatures as low as 605°C can provide good electrical properties for phosphorus-implanted silicon. This may have significance in having diffusion of impurities during the annealing process because the diffusion coefficient of phosphorus at 600°C is about six orders of magnitude lower than that at 1000°C, even if various transient enhanced diffusion effects occur for phosphorus. For applications, the present annealing techniques (RTA and/or furnace) give better results for medium doses of phosphorus ($10^{14}/cm^2$) than for lower and higher doses.

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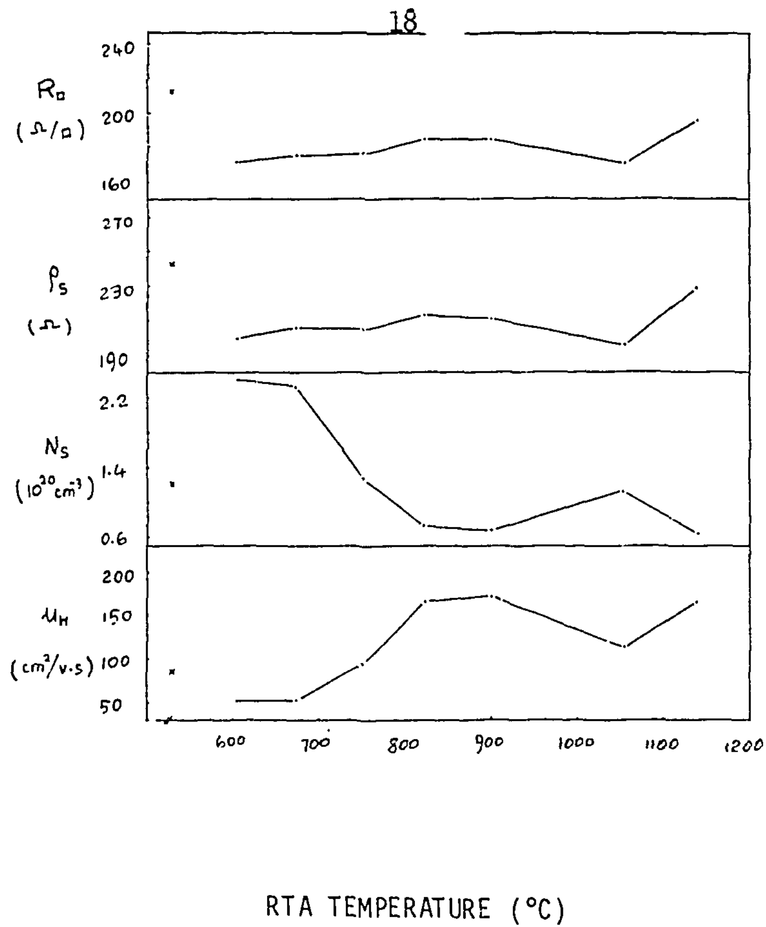

Figure 1. The sheet resistance R□, Hall resistivity ρ_S, carrier concentration N_S and Hall mobility μ_H as a function of RTA temperature (total time 15 seconds) for 80 Kev - 1.25 x 10^{14} P_4^+/cm^2 implanted silicon. x - furnace annealing.

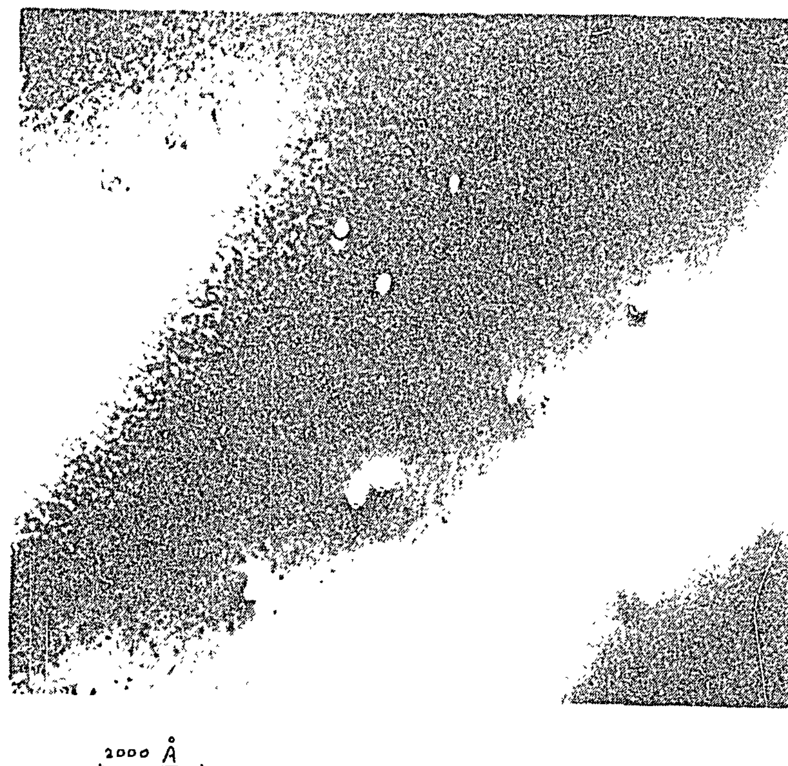

Figure 2. The TEM micrograph of 80 Kev - 1.25 x 10^{14} P_4^+/cm^2 implanted silicon with 1140°C - 15 seconds RTA.