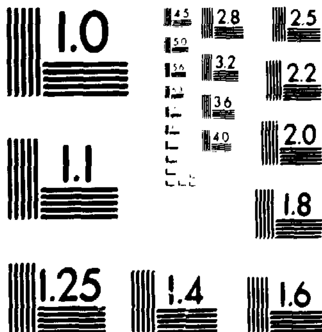

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS
STANDARD REFERENCE MATERIAL 1010a
(ANSI and ISO TEST CHART No 2)

ISTITUTO NAZIONALE DI FISICA NUCLEARE

Sezione di Napoli

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4 Settembre 1987

A. Bove, L. Caiazzo, S. Lanzano, F. Manna, G. Manto, L. Parascandolo, P. Parascandolo, A. Parmentola and G. Paternoster:

THE AUTOMATIC TEST SYSTEM FOR THE L3 MUON DRIFT CHAMBER AMPLIFIERS

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THE AUTOMATIC TEST SYSTEM FOR THE L3 MUON DRIFT CHAMBER AMPLIFIERS

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G. Manto, L. Parascandolo, P. Parascandolo, A. Parmentola,

G. Paternoster, A. Perricone

Dipartimento di Fisica and INFN Naples (Italy)

Abstract: We describe the system we developed to test the linearity of wire chambers amplifiers of the muon spectrometer presently in costruction for the L3 experiment at LEP. The system, controlled by an Apple II computer, is capable of localizing both defective components and faults in the printed board. It will be used to perform the large scale quality control of the amplifier cards.

1. INTRODUCTION

The LEP L3 muon detector is designed to measure the sagitta of the muon tracks into 5 KGauss magnetic field with very high spatial resolution (ref.1 and 2). The detector consists of 80 multiwire drift chambers of 6x2 m^2 (P − chambers) which measure the muon coordinates in the plane perpendicular to the magnetic field and 96 drift chambers (Z − chambers) which measure the coordinate along the beam. The spectrometer surrounds the beams with octagonal simmetry; three layers of chambers are arranged in independent octants for reasons of precision alignement of the detectors relative to each other. The P − chambers single wire resolution is 150 μm; due to their multiple sampling, final spatial resolution of each chamber is 50μm, and momentum resolution will be of the order of 2 % at 50 GeV/c.

The total number of wires is about 28,000 for the P chambers and about 11,000 for the Z chambers. However , the total number of channels is about 22,000 since two collinear wires are electrically linked into the input of one amplifier. A prototype wire amplifier was first built and breadboarded at NIKHEF − H (Amsterdam) (ref. 3), then hybridized and mass produced by Philips. Main specifications of this amplifiers are : gain ($\pm$ 12mV/μA), noise ($<$ 0.1 RMS), linearity deviation ($<$0.2 %), dynamic input and output impedance (50 Ω) and risetime ($<$ 5 nsec). A 16 − fold amplifier card is presently being mass − produced; 550 cards are needed for Z chambers read − out.

This note describes the test system we have designed to perform the large scale quality control of the amplifier boards for the Z chambers. The system is controlled by an Apple II microcomputer which, if set at automatic sequence, performs a serial scanning of all the channels of the board under test, applying pulses of increasing amplitude to their input;amplifier outputs are digitized, a linear fit is performed and relevant parameters are written on floppy disk. Moreover,it is also possible to choose a particular channel applying pulses whose amplitude is software controlled. Our system, while designed for the board schematically shown in fig. 1 , can be easily adapted to different amplifier or board types.

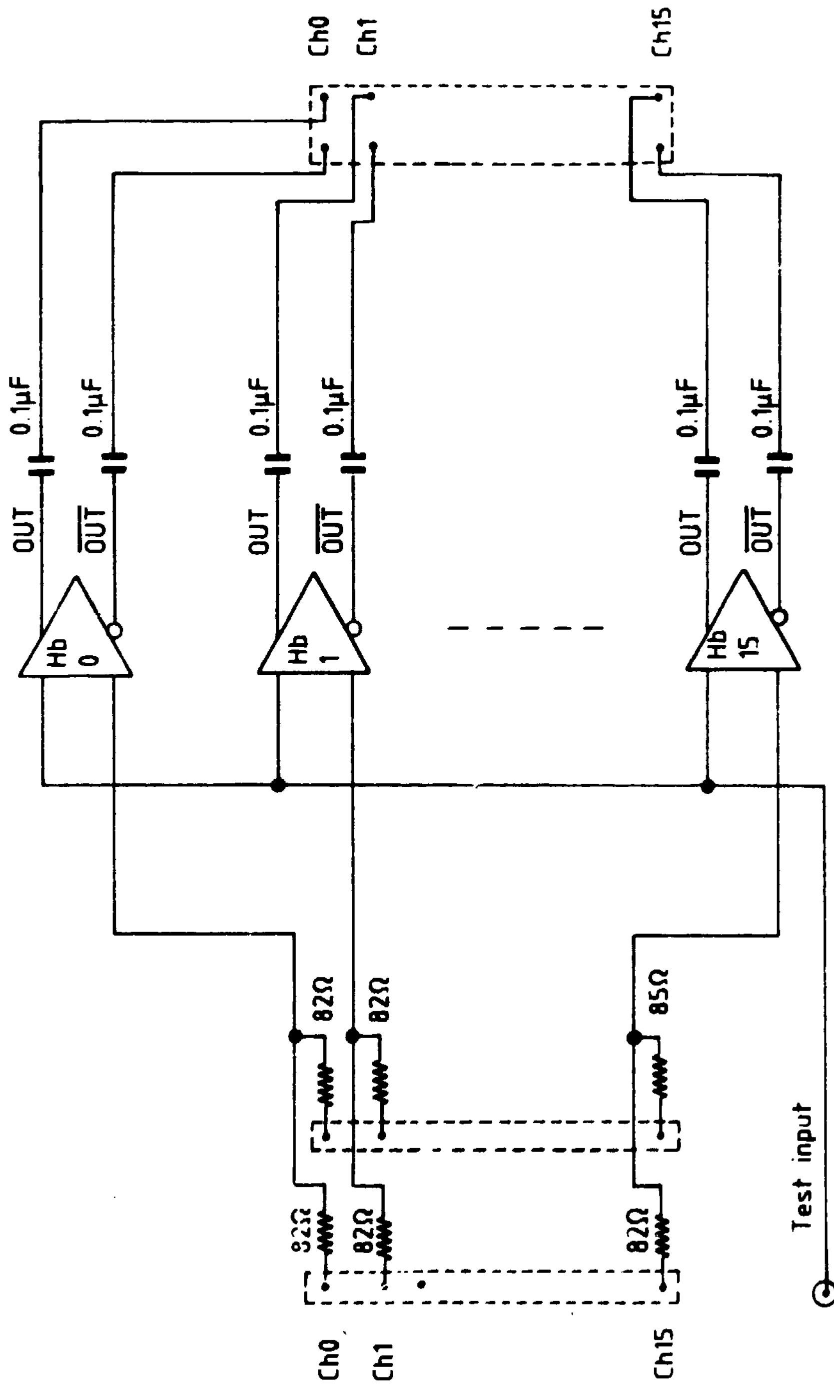


Fig. 1 — Wire amplifier card

2. THE TEST SYSTEM

The system performs the linearity test of each of the 16 channels contained in a card, for an input current range of 31.5 dB (from 2.6 μA to 100 μA); the output is digitized with an 8 bit ADC. As we said ,two collinear wires coming from different connectors are linked into the same amplifier : for this reason the test system considers the board as having 32 inputs , and detects faults on both input connectors, shorts between adjacent lines, faulty chips and interrupted lines. The test system produces pulses of different amplitude which are used to feed the amplifier channels either individually or in groups ,under program control. A pulse height analysis of the output is performed by an ADC converter; the Apple then produces a graphic display of the input – output functional relationship of each channel. A block diagram of the hardware is drawn in fig. 2. In addition to the Apple II itself, the system consists of an Eurocrate containing in total 6 boards ,logic or analog : interface, optocoupler, pulse generator, demultiplexer, multiplexer, ADC. The interface board plugs directly into one of the seven slots available on the Apple backplane.

The first module generates a variable amplitude pulse which will be the input to the next module containing a 32 channels analog demultiplexer plus some circuitry necessary to check the test line, common to all the sixteen amplifiers of one card. The outputs from the amplifier card are connected to a module containing two multiplexers which select one of the 32 outputs, 16 positive and 16 negative. The outputs of these multiplexers feed another module containing a stretcher plus an analog to digital converter (8 bits). A board of optocouplers is also required in order to separate the noisy computer ground from the test system ground. Each of these modules is computer controlled. The test system is built in a memory mapped fashion and a single operation onto one board simply consists of a write (or read) operation performed by the computer into (or from) a register board. To achieve maximum test speed the program is mainly written in assembly language. There is, however ,a BASIC supervisor program which calls the assembly language routines as required.

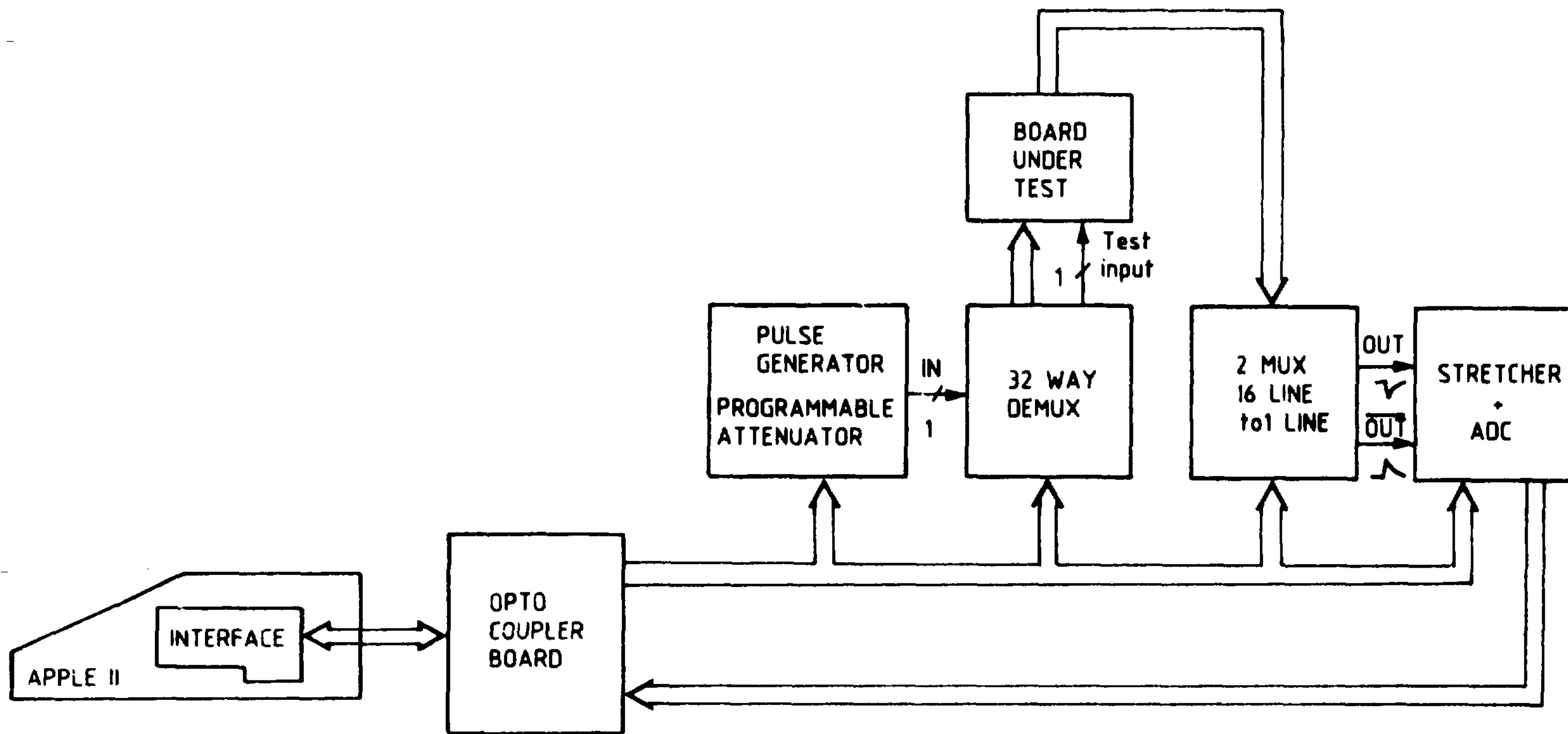


Fig. 2 – Block diagram of the test system

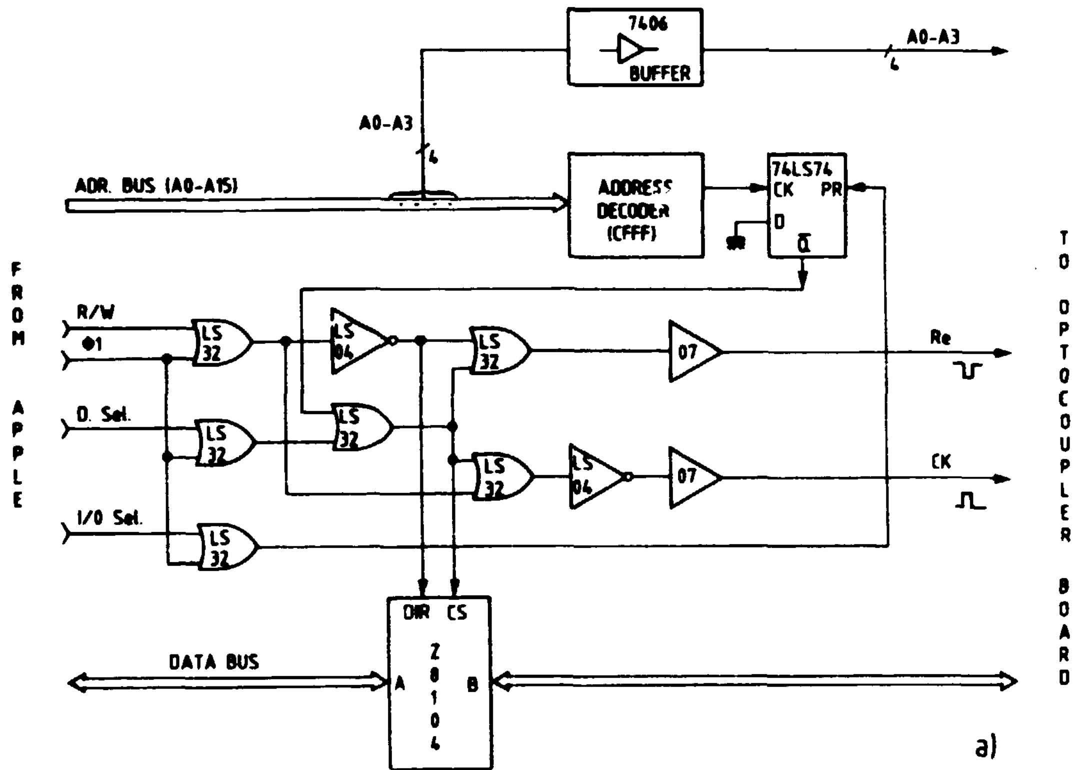
2.1 The interface

The Apple computer is based on a 6502 microprocessor which can reference 64K memory locations (ref. 4). The RAM memory starts at location zero and extends up to location BFFF (49151 in decimal base). The following 4K locations from address C000 to location CFFF , are reserved for input/output operations.

On the Apple backplane eight slots are provided,numbered from 0 to 7. 256 locations are reserved to each slot,and can be used by a peripheral for PROM, ROM or also RAM ; additional sixteen locations can be freely used by each peripheral.On each slot, in addition to microprocessor address bus, data bus and control bus ,two slot dependent signals are available , I/O SELECT signal and DEVICE SELECT signal. The I/O SELECT is low when the microprocessor is holding an address between Cn00 and CnFF where n is the slot number. The DEVICE SELECT signal is low when the address bus is holding an address between C0n0 and C0nF.

The interface we have developed is slot independent and can be activated or disabled under program control (fig.3a). This action is performed by a 74LS74 register which enables the interface, when set by the I/O SELECT signal. In order to disable the interface, the program must reference location CFFF which resets the 74LS74. When the interface is enabled, the CS signal to the Z8104 becomes active, otherwise this chip is in the tri−state, high impedance condition. When the interface is active, the R/W (read/write) signal from the microprocessor is decoded providing two signals : the Re (read enable) signal and the Ck signal. The Re signal is used to read data from the system; the Ck signal is used to clock data into the test system.

The address bus from the microprocessor is only partially used on the test system. The address lines which are used are buffered through a 7406 open collector buffer. The data bus is buffered with an Z8104 bidirectional bus transceiver. The direction of data transmission from Apple to the system or viceversa is controlled by the DIR signal which is derived from the R/W signal OR−ed with $\Phi 1$.



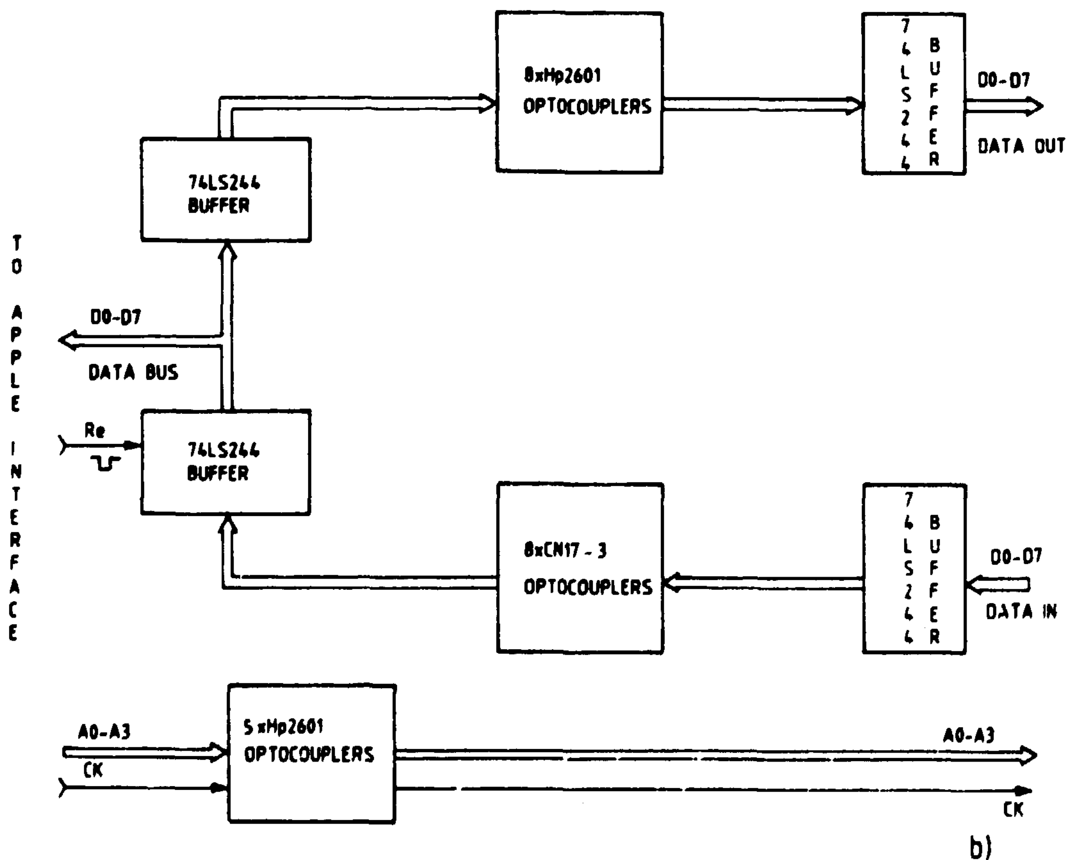


Fig. 3 – The interface to the minicomputer a – Apple interface

b – Optocouplers board

2.2 *The optocouplers board*

The purpose of this board is to achieve electric separation between the Apple computer and the test system, reducing noise by more than one order of magnitude in order to perform measurement of low currents (fig. 3b). Two types of optocouplers are used on this board : a fast one to decouple data and pulses coming from the Apple and a slower one for data going to the Apple from the system. The fast optocouplers are Hewlett Packard HCPL2601 having a typical delay time of 75 nsec ; the other type is a common Siemens CN17 − 3 having a delay time of 2 μsec.

2.3 *The analog test pulse generator*

When generating a pulse, Apple simply makes a reference to the memory location C0C7. This action produces a pulse at the output of the 74LS138 decoder (fig. 4). Although the electric separation of the grounds makes this pulse clean enough , the waveform shows at both edges some rippling disturbance of more than 10 millivolt which makes it unsuitable as a reference.

Linearity measurements demand precise test pulse in order to obtain reliable results. To keep pulse aberrations to a minimum we use the 74LS138 output to switch a fast diode bridge made with four HP2900 whose output, in absence of pulses, is zero. Two reference voltages bias the bridge. In the presence of a pulse, the bridge switches cleanly and quickly producing a pulse which is further clamped at 300 mV with a selected fast switching HP2900 diode. In this way the characteristics of the Apple pulse has no influence on the measurement.

The output from the bridge drives a fast buffer made with four transistors forming a complementary emitter follower, capable to drive a substantial cable capacitance without distorsion.

The attenuator bank consists of six calibrated attenuators, ranging between 0.5 and 16 dB. Each attenuator has a dB attenuation twice as large as the previous one, so that the maximum attenuation amounts to 31.5 dB. The interconnection lines between the attenuators and from the attenuators to the

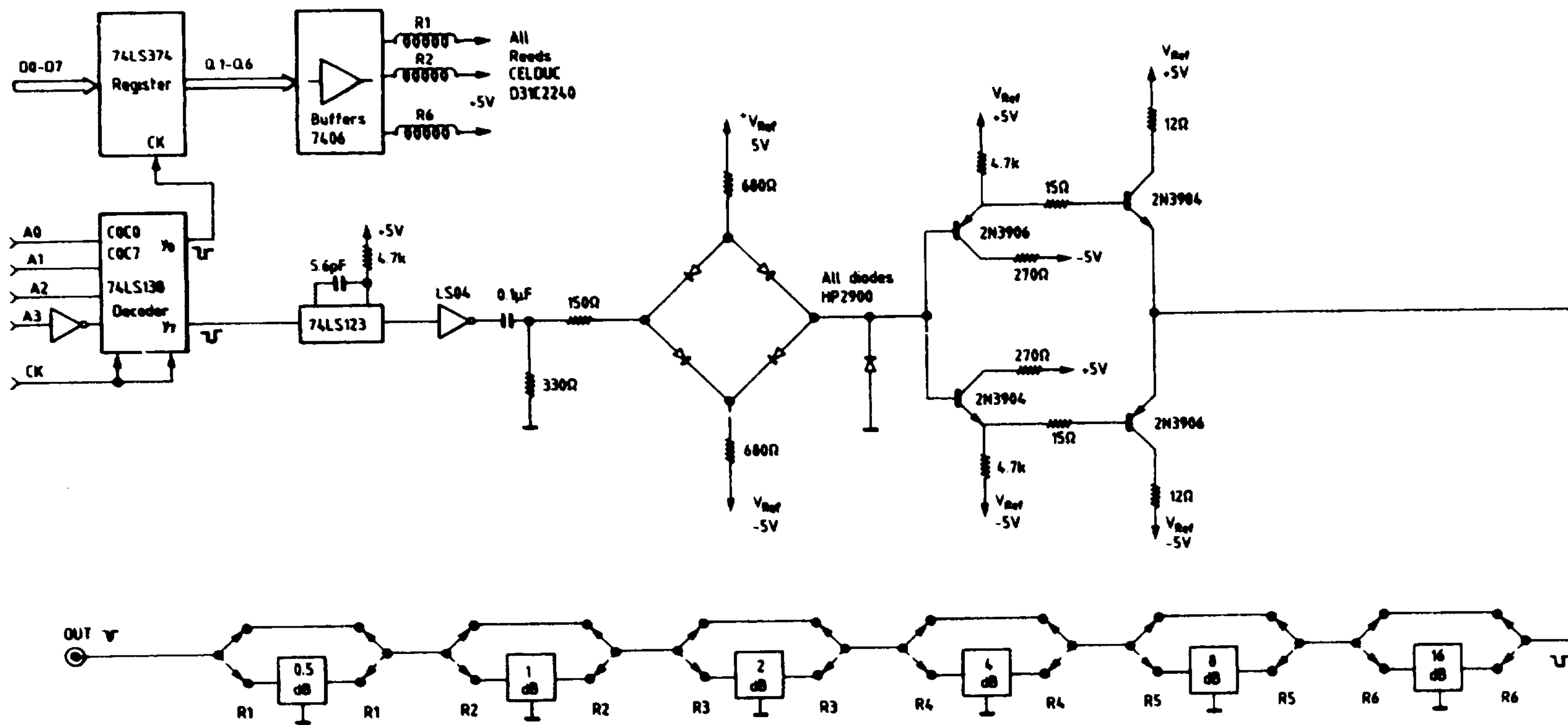


Fig. 4 – Pulse generator and programmable attenuator module

output are made so that the characteristic impedance is 50 Ω : the lines are 2.8 mm wide over the mandatory ground plane.

To change pulse heights, the Apple writes a different six bits number onto the register board. Each attenuator is inserted if the corresponding bit in the register is set. The switch action is performed by 12 reed relais (two for each attenuator). The use of the reed relais introduce almost no degradation of the characteristics of the input pulse (3 nsec risetime ,50 nsec width).

When the Apple wants to change the value of the attenuation, it performs a store of the new attenuation value into the C0C0 location. This action produces a pulse at the output Y0 of the 74LS138 decoder which is used as a clock for the 74LS374 register.

2.4 The logic modules of the test system

. The first module works like a decoder enabling the tester to pulse one (or more) out of 32 channels or to pulse directly the common test line. As shown in fig. 5 , in this board we have 32 reed relais plus a selection logic. Other 3 reed relais are used to select a special data path in order to pulse the common test line.

This board occupies five locations in the Apple memory (C0C1 through C0C5). Four of these locations are used to select the channel or the channels to be pulsed simultaneously in case of check for crosstalk. The fifth location is used to store the control word which selects the path of the pulses.

Two cabled bus consisting each of 16 coaxial cables plus a single cable for the test line are the outputs from this module. Cables are terminated at the far end on their characteristic impedance of 50 Ω, and through the RC networks C0 and C1 of fig. 5 are plugged into the two input connectors of the card being tested.

The outputs of the amplifiers are taken in a similar manner. As shown in fig. 6 a little board plugs directly onto the output connector and from there 32 cables feed the analog multiplexer module containing two analog multiplexers made by 32 reed relais one for positive outputs and the other for the

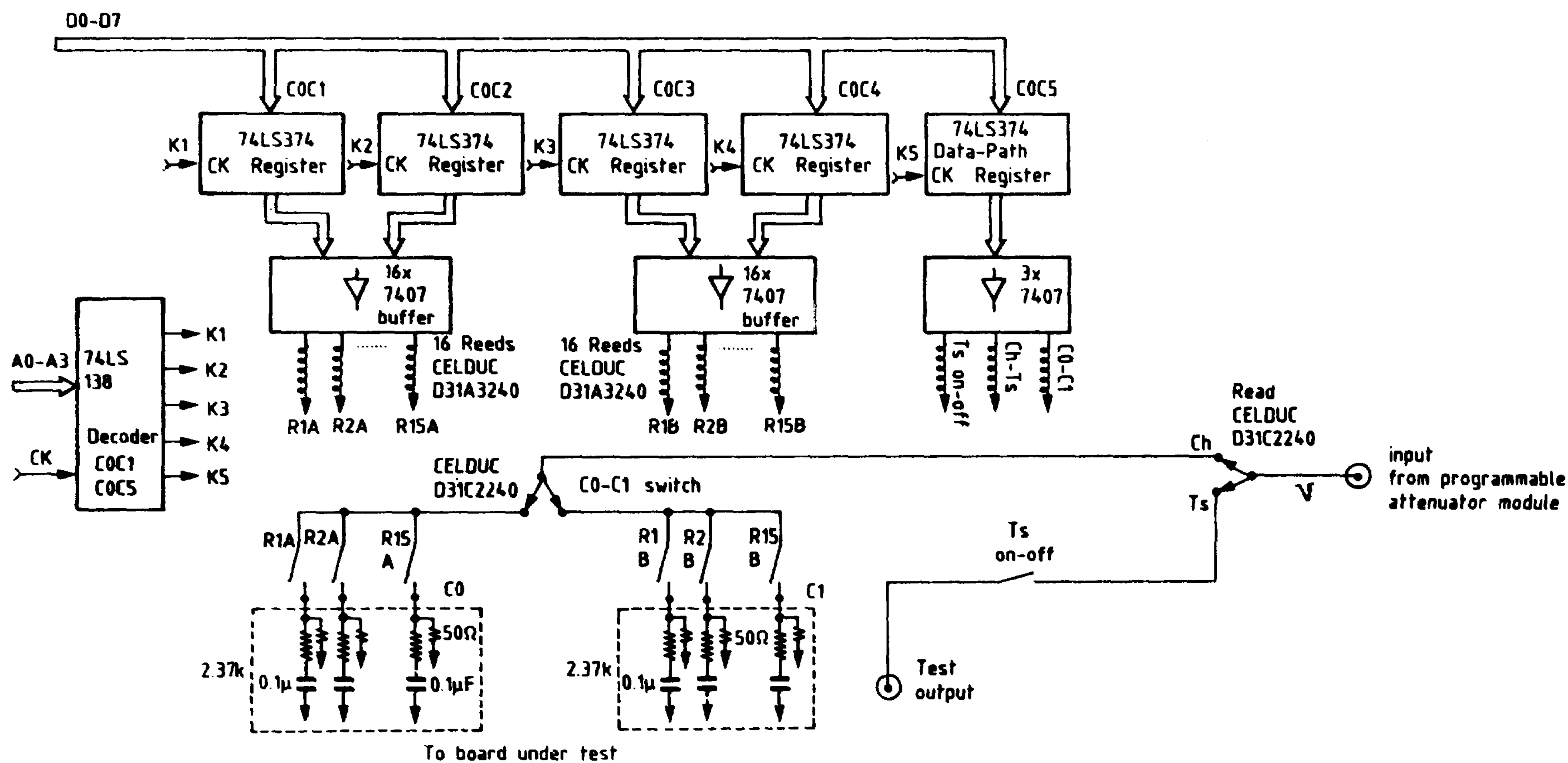


Fig. 5 – Programmable demultiplexer board

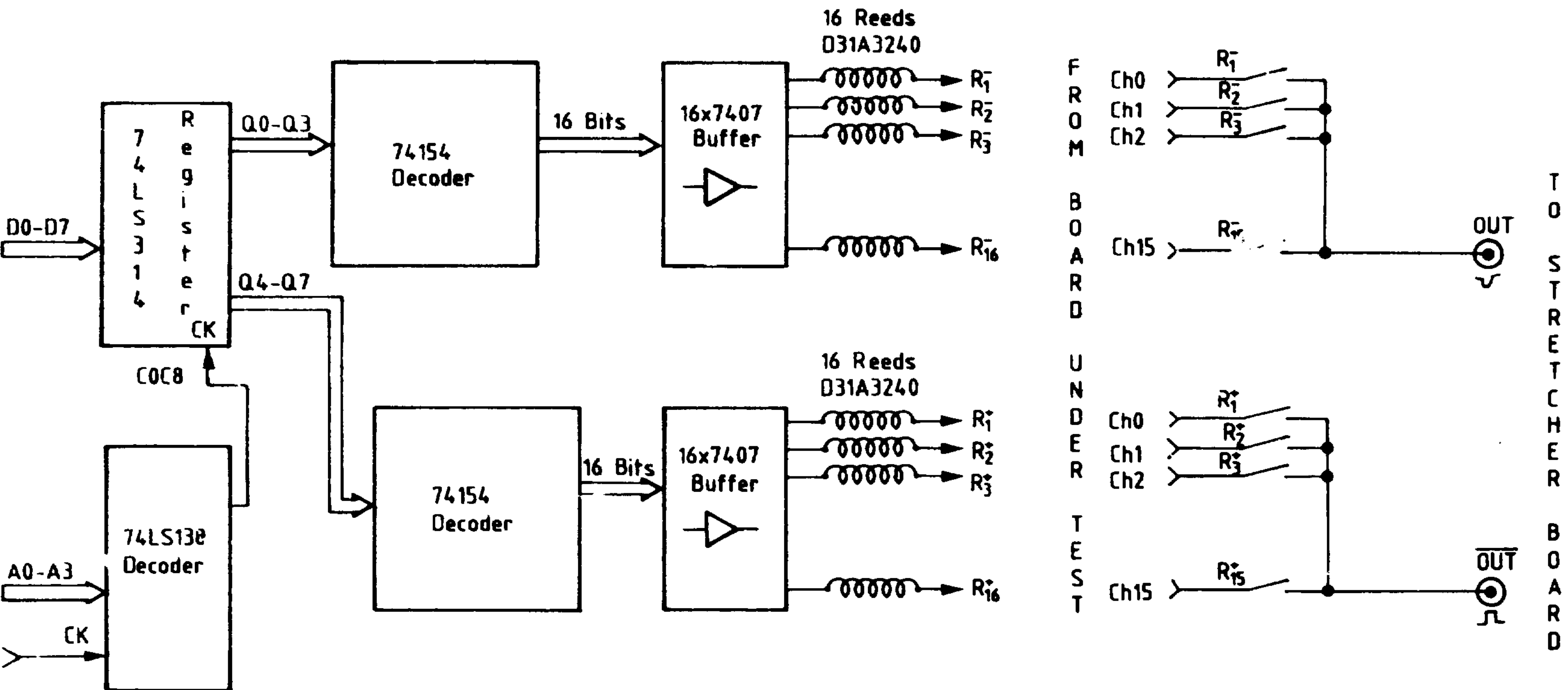


Fig. 6 – Programmable multiplexer module

negative ones. The memory location the Apple refers to, when loading the channel to be analized, is C0C8. The upper four bits control the multiplexer serving positive inputs while the lower four bits control the other multiplexer. There are two outputs, positive and negative, coming from this board and connected to the stretcher and ADC card.

2.5 The analog module

The stretcher accepts only positive inputs so that, in order to analyze negative signals, they must first be inverted. This action is performed by a pulse transformer suitable for a pulse width of 50 nsec. The switch between positive and negative is carried out by a reed relais.

The stretcher circuitry has been developed at CERN for the CHARM II experiment and it is described in greater details elsewhere (ref. 5). The circuitry has been slightly modified here to take into account the different range of operation. The integral linearity of this stretcher is better than 1%. Referring to fig. 7 the first array (type CA 3083) together with the memory capacitor (500 pF mica) form a peak detector network. As the memory capacitor is charged trough a 10 Ω resistor, the time constant is 5 nsec. After five time constant the capacitor will be charged to 99.3% of the peak of the input pulse (settling time 25 nsec). After the trailing edge of the input pulse the capacitor starts slowly to discharge (drop rate 2.5 mV/μsec). The second CA 3083 array acts as a voltage amplifier with a gain of 2. The memory capacitor is reset after read-out by a TTL pulse applied to the base of the T6 transistor which in turn switches the T3-T4 differential pair.

The output of the stretcher is connected to an ADC converter, an ADC 0820 of National Semiconductor which uses an half-flash conversion technique with a maximum conversion time of 2.5 μsec. The most important feature of this converter is that input signals with slew rate of less than 100 mV/μsec do not need an external sample and hold.

This board occupies two locations in the Apple memory map, C0C6 and C0C7. The first location is used to choose between positive and negative pulses while a reference to C0C7 has two conse-

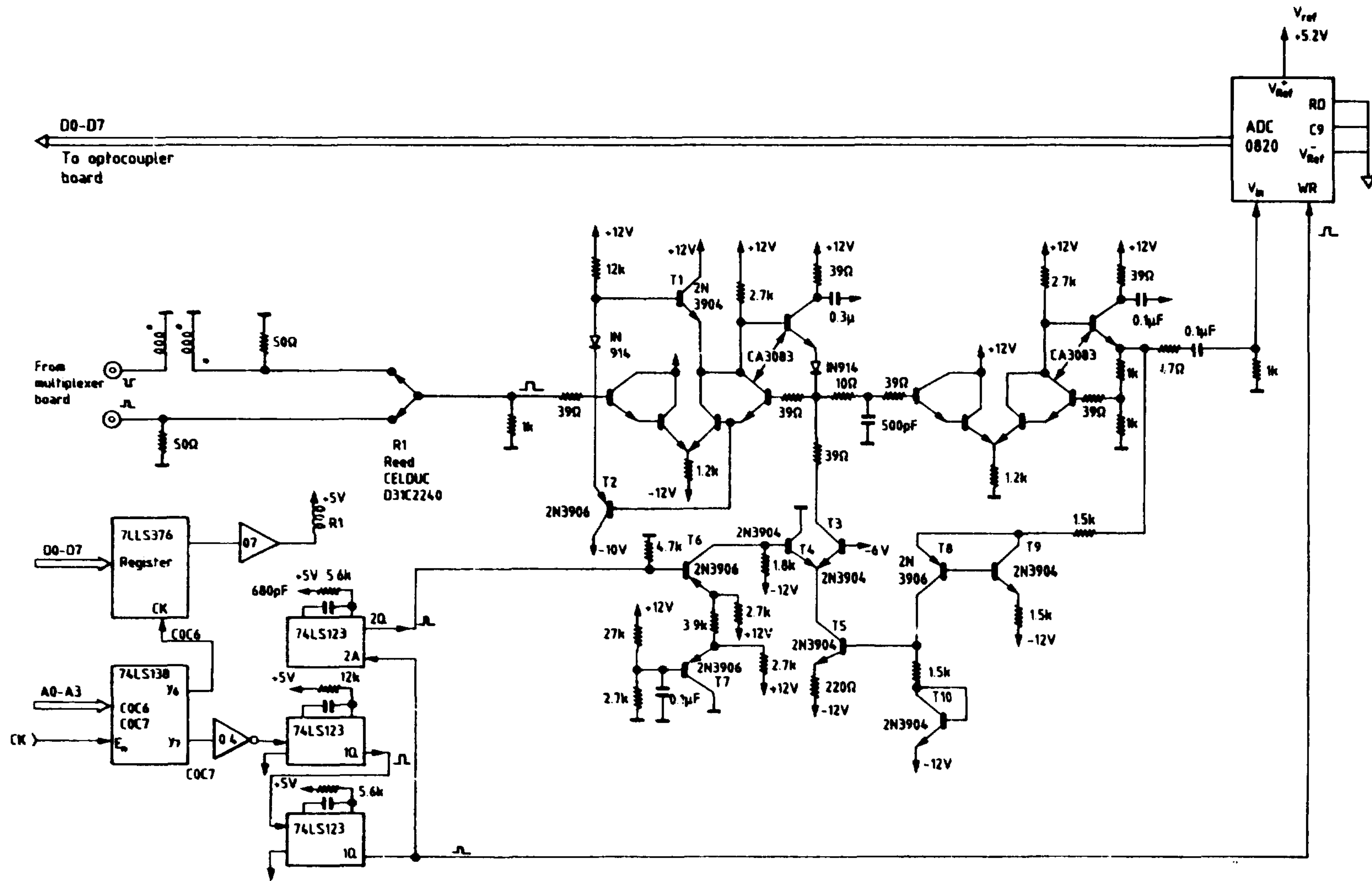


Fig. 7 – Stretcher and ADC board

quences : it starts the reference pulse in the attenuator board and here it lets the ADC converter make a sample of the input and then reset the stretcher.

3. CONCLUSIONS

The test system described in this note , significantly different from commercially available test system, performs the test of the linearity of each of the 16 channels with 1% resolution. The data logger capability of Apple provides the possibility to save on floppy disks the results of the test.

Another important feature of the test system is its capability to differentiate easily between a faulty device and an interconnect failure. This feature enables to pinpoint many problems in seconds, reducing substantially repair time and labor costs.

References

(1) L3 Technical proposal , May 1983 , section 5

(2) U. Becker et al., "Resolution study for large drift chamber" N.I.M. 220 (1984) 338 – 342

(3) "The L3 wire – amplifier NH19 – 6111", NIKHEF – H Internal Report (unpublished)

(4) APPLE II Reference manual, Apple Computer Inc.

(5) J.C. Berset et al.,"Peak detector type 7322", CERN EP electronic note 84 – 01 ,january 1984