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THE CHATEAU DE CRISTAL DATA ACQUISITION SYSTEM

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Abstract

This data acquisition system is built on several dedicated data transfer busses : ADC data readout through the FERA bus, parallel data processing in two VME crates. High data rates and selectivities are performed via this acquisition structure and new developped processing units. The system modularity allows various experiments with additional detectors.

1. Introduction

The Château de Cristal is a 4πγ ray spectrometer. The geometry versatility [1] of this system affords 38 or 74 BaF2 detectors which can be set in coincidence with other radiation detectors (γ or particles). This system has been first designed for γ-γ or particle-γ coincidence measurements in heavy ions induced reactions where the γ multiplicity of the events, the total γ ray energy and good timing are the basic caracteristics necessary to study nuclear reactions mechanisms as well as the structure of nuclei at high angular momentum.

The data acquisition system [1,2]for the "Château de Cristal" and the other detectors has been conceived as performant and versatile as possible to allow a good timing, on-line accurate selectivities and a high data rate.

The performance of the data acquisition system is due to the use of various data transfer busses, of parallel processing and software optimization with several microprocessors facilities The data transfers proceed through dedicated busses : CAMAC for initialization purposes, FERA (Fast Encoding and Readout ADC [3]) for ADC readout, VME, VMX... for data managment with 68000 microprocessors. The "Château de Cristal" and its data handling has been constructed through a collaboration of six laboratories [1,2]: CEN Bordeaux, ISN Grenoble, IPN Lyon, CSNSM Orsay, IPN Orsay and CRN Strasbourg belonging at the French Nuclear Physics Institut (IN2P3). This facility is now installed at the MP Tandem in CRN Strasbourg.

2. Data acquisition overview : SAGABUS

The experiments using the Château de Cristal needs the individual energy and time of all the BaF2 involved in the set-up as well as additional parameters (time, energy, time of flight..) of additional detectors. A general overview of the electronics and the data handling is shown on figure 1.

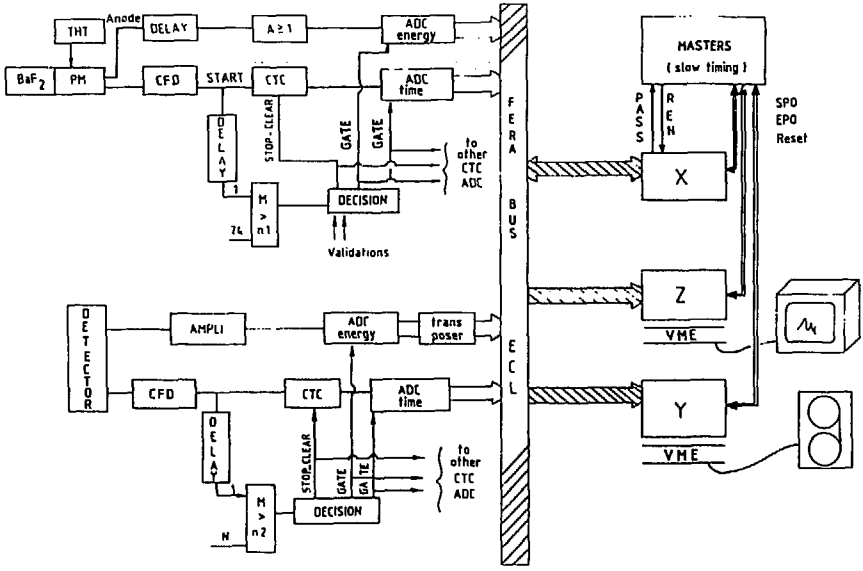
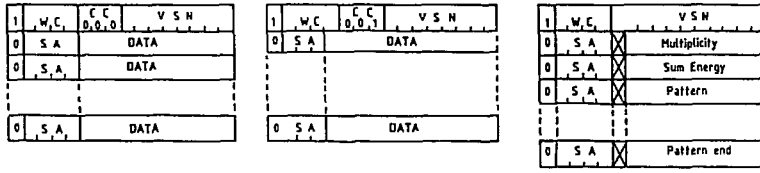


Fig. 1 General overview of the data acquisition system for the "Château de Cristal".



4300 FERA ADC GE ADC X module

Fig. 2 - FERA data format of ADC's and X processing :
VSN : Virtual Station Number ; SA : Camac Station Adress ;
CC : Coding Code (extension of the Lecroy FERA format).

The data handling versatility and efficiency helds in the use of several dedicated busses for data transfer and parallel processing this is the SACABUS system (Systeme d'Acquisition A BUS) : all the ADC's readout proceed via the fast ECL bus (100 ns/16 bits). The data storage and visualization is handled by 68000 microprocessors using the VME bus and local busses (see § 4). The data acquisition is organized to use the same charge 4300 Lecroy ADC's system for time and energy parameters (up to 11 bits) for data transfers on the FERA bus. A specific unit [1,2] has been developped to interface the Ge ADC in NIM standard to obtain an extended version of the FERA bus for 12 bits ADC. The data format of these FERA transfers is shown on figure 2.

The on-line event selection is performed at two levels :

- before encodage via the fast part of the masters unit [1,2] one may require a minimum multiplicity level or various coincidence requirements with external detectors

- after encodage : the X processing unit reads the data and delivers to the slow part of the masters unit a validation mark for each event satisfying predefined windows in energy, time, multiplicity and/or sum energy.
  - The Z modules (DMI units) build the spectra of software selected ADC
  - The Y module ("DMA" unit) buffers the chosen ADC's parameters to be stored on tape via the VME bus.

In this system all the data are processed in parallel in the X, Z, Y units. While the X units are driven via the FERA control lines (REN, PASS,...) the Z and Y units are activated by the masters unit Start Program Order (SPO) at the beginning of the FERA data transfer, the data are processed in Z and Y which send to the masters a End Program Order (EPO) when their processing is finished. However the Z,Y units may be reseted before the end of processing by the masters for example if the windows in X are not satisfied, this minimize the dead time due to physically uninteresting events. Since the X windows are set on logical encoded data this selection is very accurate and reduce drastically the data stored on tape, meanwhile on-line spectra can be build via several Z modules with and without these conditions affording a very good on-line test of the experiments.

Two versions of the Z unit allow the DMI of spectra and biparameteric matrices.

The data transfer is optimized by the use (fig. 1)of two VME dedicated crates (one for the visualization tasks the other for the storage on tape) and the availability of local busses.

3. Processing units

The X, Y and Z units have been designed to process the data of the FERA bus formatted as shown in figure 2. These modules are interfaces to data bus : VME and local bus for Y and Z, and FERA itself for X.

3.1 Z module (DMI)

The Z module is a one slot VME module [1] dedicated to DMI. This unit can manage three 256 ko dual port RAM DSSE IMEM [4] the DMI is performed via the local bus (P2 connector) of these VME boards. Figure 3 shows a diagram of the Z unit.

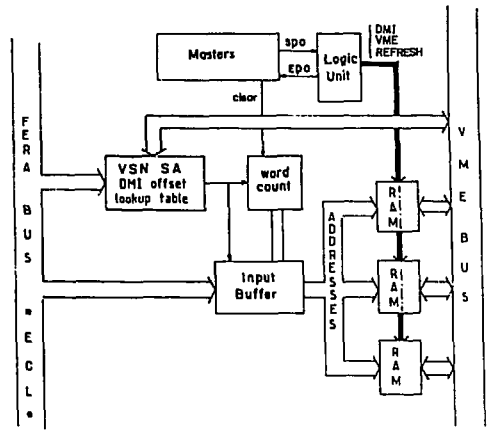


Fig. 3 - Z module schematics

The FERA data are selectively buffered according to a look-up table previously loaded. Each parameter of the experiment is uniquely defined by the VSN and SA of the FERA format (fig. 2).The concatenation of VSNSA is an index in the look-up table of the Z unit.

Each word of the look-up table contains the DMI offset in the dual port RAM and a bit flag whose setting corresponds to an authorized DMI for this parameter. Spectra length range from 256 to 32k channels.

The selected data are piled up in the input buffer at the ECL transfer rate (100 ns/16 bits). Once all the ADC have been read the masters sends a SPO order which starts the DMI process (420 ns/point to be up dated) ; when the job is done for all the data in the input buffer, Z sends a EPO to the masters.

If the event is rejected by the masters a Reset of the Z input buffer is immediate. Note that the ADC may start coding as soon as an SPO or a Reset is send by the masters since at this point all the data have been read. Several Z units can be used with their associated dual port RAM each of these Z may be related to a dedicated X unit hence on-line conditionned spectra may be build at no time cost and the physicist can compare the same ADC parameter spectrum with several on-line selections (multiplicity bin for example).

A bidimensional DMI unit (Z' [1]) is available to build biparametric matrices.

3.2 Y Module ("DMA")

The Y module (fig. 4) is two VME boards [1] dedicated to interface the FERA data to the VME bus. The FERA data are stored in the input buffer if the appropriate bit is set in the look-up table for the corresponding VSN.SA, these data are finally stored on tape by the master CPU (§4.2). The handshaking with the masters is similar to the Z unit one. At reception of SPO from the masters the Y unit activates an Interrupt (IT) (or set a bit in the command register) towards the 68000 microprocessor master of the VME bus which then transfers the data from the input buffer to a VME RAM (§ 4.2). When the job is done the microprocessor reset the word count, Y sends a EPO to the masters and is ready for a new event.

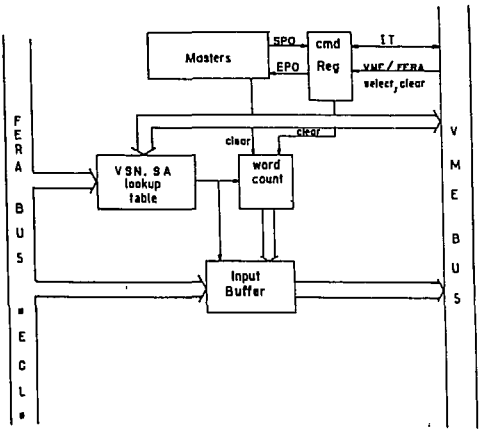


Fig. 4 - Y module schematics

3.3 X Processing unit

The X module (fig. 5) is a two slot CAMAC unit [1] that builds on flight multiplicity, sum energy and pattern of the detectors which fired in the Y flux. These informations are calculated for each event whose timming and/or energy satisfy pre-loaded windows (upper level-lower level) and are transfered (fig. 2) on the FERA data bus to the Z and Y units. Additional windows on the resulting multiplicity and sum energy can be used to mark the event in the masters unit. This validation can be used by the Z units to build on flight conditioned spectra.

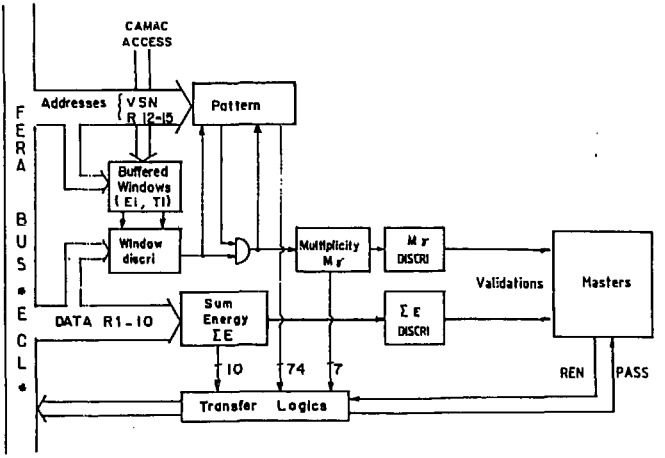


Fig. 5 - X Processing schematics.

4. Data handling

The aim of a data acquisition system is to keep a close control of the experiment through spectra or biparametric matrices build on flight and to store the events on a magnetic tape which is a universal support. The number of ADC's parameters involved in the "Château de Cristal" implies the use of large memories and fast processors to handle the data, besides a data storage on 6250 BPI tapes is necessary to minimize the magtapes number. The VME bus standard and 68000 microprocessors have been choosen on account of the performance, the cheapness and availability of several CPU and I/O boards. The great modularity allowed by this standard facilitate the developments of specific units and the local busses facilities enhance the data acquisition system. As shown on figure 1 the FERA data are processed in parallel in two dedicated VME crates working in an asynchronous way, the data transfers being handled by the masters unit. The CAMAC bus (fig. 6) is used only for the initialization of CAMAC units. A serial link between the two VME crates insures the spectra transfer between the "Z VME" crate and the "Y VME" crate dedicated to storage on tape [2].

4.1 *Z VME crate*

This crate (fig. 6) is dedicated to the CAMAC (and High Voltage) initialization and to the visualization of spectra and matrices build by the Z units. Several Z units are used to afford selective control spectra mapped in a contiguous memory space, each Z unit manage up to 192k channels. The visualization of spectra and matrices is done via the DSS5 chroma 8 [4]. This VME board has a scanning faster than the conventional RS232 graphic terminals. A hard copy software has been implemented in EPROM in this board and uses the P2 connector. The initialization procedures [2] are individual tasks running when the acquisition is off. The software has been made easy to the physician to define versatile ADC configurations and load the look-up tables of X and Z units. Theses tasks create (or modify) files to save all the experiment parameters and to change some parameters quickly (for example X windows). These initializations include an automatic pedestal adjustment of all the 4300 ADC used in the experiment. The visualization task affords all the usual spectra manipulations with commands appropriate to manage the large number of spectra [2].

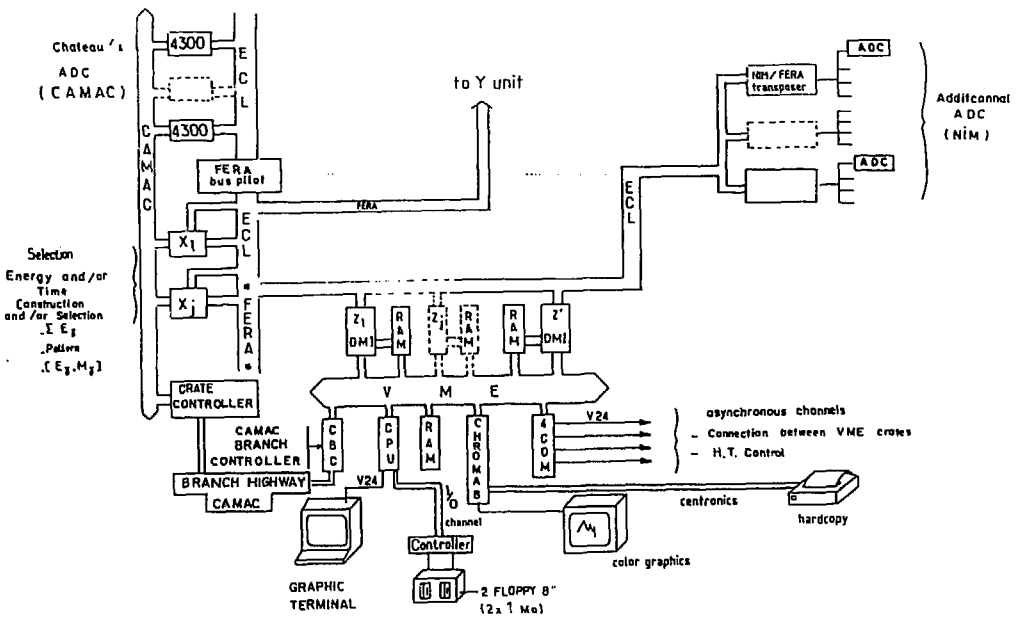


Fig. 6 - Z VME crate configuration

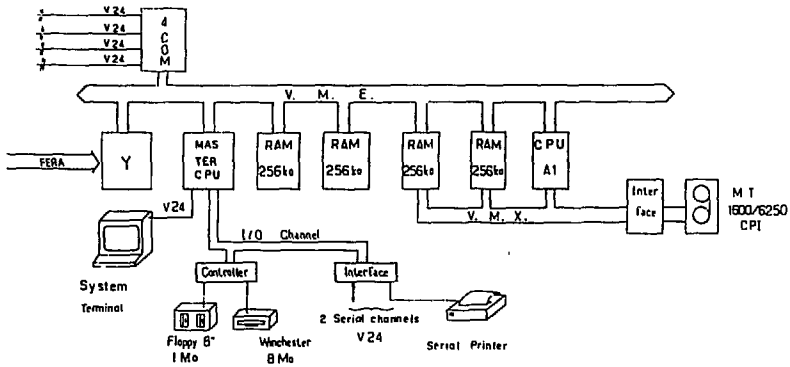


Fig. 7 - Y VME crate configuration

4.2 Y VME crate

This crate (fig. 7) is dedicated to storage on magtape of the FERA data stored in the Y module. The tape unit supports 1600 and 6250 BPI densities with a streamer mode. To keep the performances in this mode the VME interface to this tape unit has been carefully studied. This interface is an association of VME boards (fig. 7) : two 256ko dual port (VME/VMX) RAM (DSSE DPRX [4]), a 68000 processor unit (DSSE-CPUA1 [4]) and the effective interface board to the Pertec Streaming Tape Unit (STU). The RAM are used in flip-flop and the CPUA1 incorporates in EPROM the MT driver. The use of the VMX bus allows to keep the tape in streaming mode for high data rates. The only task running in this crate while the acquisition is on handles the events in Y towards the DPRX memories. The best performances of the data acquisition are obtained in scanning the flag set in Y module when an event is to be read. The master CPU (MVME110 [5]) transfers each event without reduction and pile them in the DPRX as an image of the future magtape records with event separators and end of records identifier (fig. 8 and 9). The CPU handles the flip-flop and initiates to the CPUA1 a MT transfer when one DPRX is full.

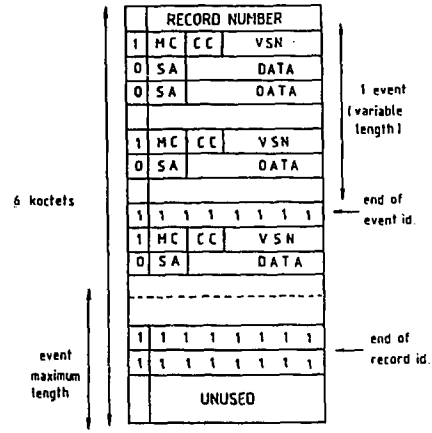


Fig. 8 - Record formatting

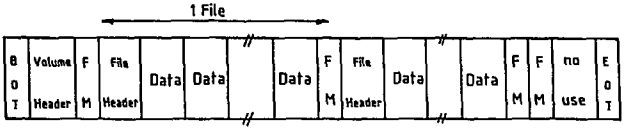


Fig. 9 - Data Structure on magtape.

The mean speed (fig. 10) of data acquisition on tape is the writing tape speed for 6Ko records above 40 words/event. Below this event length, the data handling and checking become the major contribution to the data acquisiton speed.

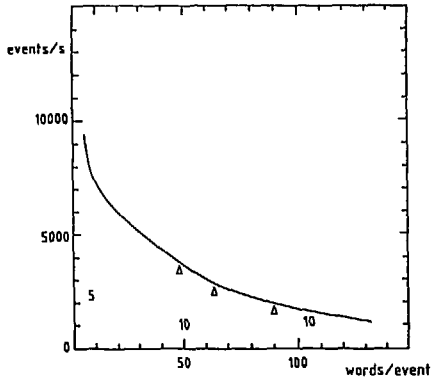


Fig. 10 - Data acquisition speed caracteristics : the numbers are measured mean dead time and Δ are measured at = 100 % dead time (full tape speed)

Conclusion

The Château de Cristal data acquisition system is now running in its full configuration since summer 86. The versatility of this SACABUS system with the conjonction of the FERA bus and the VME bus has proven its efficiency by the amount of experiments done with this system [6]. Several smaller versions are now implemented in other IN2P3 laboratories in France.

We are now looking forward to enhance the data acquisition possibilities with other processing units(new X version and 68020 dual port CPU) and the new developments in optic numeric disks. We should note also that the off-line data analysis should be carefully studied to enhance data reduction procedures.

Acknowledgments

I am grateful to all the colleagues who worked for the elaboration and evolution of the Château de Cristal particularly to F. Beck in charge of the project and the technical staff with Ch. Ring and D. Lecouturier and their teams.

References

[1] F. Beck, Ch. Ring and M.M. Villard, "Fast electronics and data handling system done for the gamma 4π array "Château de Cristal". To be submited to NIM.

[2] D. Cadeac "Contribution à la gestion et à l'acquisition de données du multicompteur BaF2 du Château de Cristal". Thesis October 1986. University of Bordeaux and references therein.

[3] FERA is a trademark of Lecroy

[4] DSSE is a trademark of Data Sud S.A., Montpellier, France.
CPUA1, DPRX, CHROMA 8, 4 COM are products of Data Sud S.A.

[5] MVME is a trademark of MOTOROLA, Inc.

[6] F. Beck "Studies of nuclear behaviour with Château de Cristal". Aussois March 9-13 1987 - and references therein.