Fermi National Accelerator Laboratory

TM-1488

Fermilab Accelerator Control System Analog Monitoring Facilities*

K. Seino, L. Anderson, and J. Smedinghoff
Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

October 1987

*Submitted to the Europhysics Conference on Control Systems for Experimental Physics at CERN, Geneva, Switzerland, September 28-October 2, 1987

FERMILAB ACCELERATOR CONTROL SYSTEM
ANALOG MONITORING FACILITIES

K. Seino, L. Anderson, J. Smedinghoff
Fermi National Accelerator Laboratory
P.O. Box 500, MS307
Batavia, IL 60510, USA

Thousands of analog signals are monitored in different areas of the Fermilab accelerator complex. For general purposes, analog signals are sent over coaxial or twinaxial cables with varying lengths, collected at fan-in boxes and digitized with 12 bit multiplexed ADCs. For higher resolution requirements, analog signals are digitized at sources and are serially sent to the control system. This paper surveys ADC subsystems that are used with the accelerator control systems and discusses pratical problems and solutions, and it describes how analog data are presented on the console system.

Introduction

In the early 1970's, E. Anderson, R. Ducar, G. Tool and others had purchased general purpose 12 bit multiplexed ADCs (MADCs) from Dynamic System Electronics (DSE) Corp. and other companies. Those MADCs had or have been used in the linear accelerator (LINAC), the booster, the switchyard and the Main Ring. In 1979, K. Seino designed new MADCs in order to replace ailing old MADCs in the Main Ring and the switchyard. However, the majority of them were diverted to newly evolving areas such as the Tevatron and the p-bar. When work was done for these areas, R. Ducar and others designed a fan-in box, and they established a standard how analog signals should be connected to the MADC. In 1983, W. Knopf, A. Thomas and others designed a new intelligent MADC controller called CAMAC 190, many of which are widely used in the accelerator division of the Fermilab.

In 1985, L. Anderson, M. Shea and others designed and installed MIL-1553B based 14 bit ADC systems for accurately measuring magnet currents in the p-bar facility. When M. Shea and others upgraded the LINAC control system in 1983, they designed and built ADC chasses, which were controlled by a binary I/O board in Multibus crates. For other subsystems such as the vacuum control system and the refrigeration control system, Multibus ADC boards are used. Some of them were designed and built in house, and some others were purchased from outside.

For console displays, J. Smedinghoff and others have developed a parameter program and a continuous fast time plot program (FTP), and are planning to implement a snapshot fast time plot program in the future. These programs are universal and usable with different sources of data which return from different areas of the accelerator complex.

ADC systems

General purpose MADC

Thousands of analog signals are monitored in different areas of the Fermilab accelerator complex. Most of analog signals are digitized with 12 bit MADCs (Multiplexed ADCs). Original MADC units had been purchased from outside, and these units are being replaced with newer MADCs which were designed in house.

The MADC was designed in house back in 1979 [1] in order to satisfy the following objectives.

(1) Use the latest components, ICs and subassemblies to make the unit reliable.
(2) Make the unit modular for easy maintenance and repair work.
(3) Make the unit electrically and mechanically compatible with old ones so as to replace them without holding back the accelerator operation for long periods of time.

The functional blocks of the MADC are multiplexers, an instrumentation amplifier, a sample and hold, an ADC, display/ control circuits and power supplies. Two stages of multiplexers were employed in order to multiplex 64 differential analog inputs. In the first stage, 64 differential inputs were multiplexed with 8 multiplexers, yielding 8 differential outputs. Further in the second stage, 8 differential inputs were reduced to one differential output. Harris Semiconductor HI-507A differential 8 channel multiplexers functioned very well with low leakage. The instrumentation amplifier was built with three high speed operational amplifiers (Analog Devices AD509). The amplifier had a temperature coefficient of better than 0.01 %/ Deg C, a common mode rejection ratio of greater than 74 dB at 60 Hz and a settling time of 6 us to 0.01 %. The sample/ hold was Burr Brown SHM60, and the ADC was Burr Brown ADC60-12.

Analog signals originates at various locations in the accelerator complex. They are sent over coaxial or twinaxial cables with varying lengths and are collected at fan-in boxes (or called analog entry boxes). The fan-in box is typically mounted on the top of a relay rack, in which the MADC unit is installed. Analog signals are fed from the fan-in box to the MADC via multiple pair cables, which are terminated with multi-contact round shell connectors at the MADC end. CAMAC 190 module, which resides in the same rack as the MADC or the

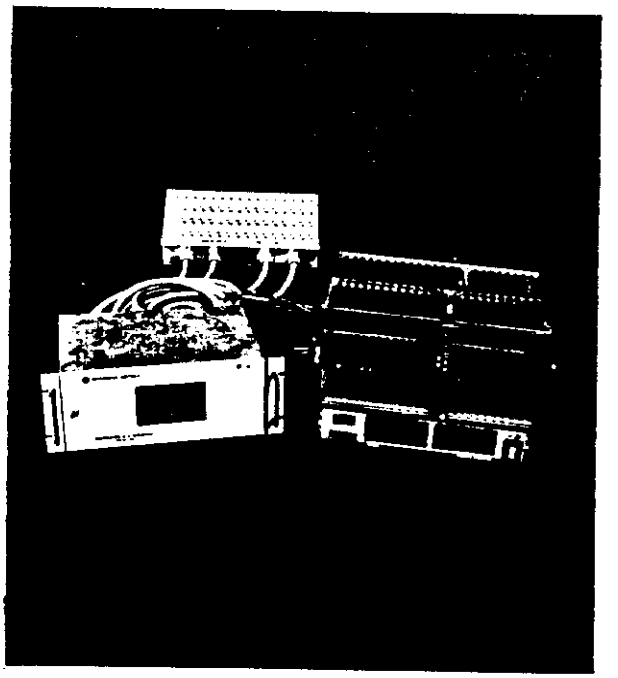

Fig. 1. Components of the general purpose MADC system.

one next to it, reads the MADC data and sends them to the accelerator control network (ACNET). The components of the general purpose MADC system is shown in Fig. 1.

A second generation MADC is now being designed. Over 120 units of the first generation have been produced and installed, and they have been well accepted by users in the Fermilab accelerator division. However, there were difficulties in getting units assembled by subcontractors. The second generation MADC is being developed with the following objectives.

(1) Use commercially available parts for the chassis and the card cage.
(2) Completely eliminate wire wrapping, mass terminate all wires and cables and make them detachable subassemblies.
(3) Make power supplies as removable modules so that they can be replaced easily.
(4) Use a LCD display and a touch sensitive switch assembly for the front panel display and controls.

High resolution ADC system

When p-bar systems people requested 14 bit ADC readings on some of their magnet currents, we first studied possibilities of replacing a 12 bit ADC with a 14 bit ADC in the general purpose MADC. However, because voltage sources would be widely scattered in service buildings and because there would be large ground loop problems, a decision was made to digitize analog signals at sources and to transmit data via a serial link to the ACNET.

The MIL-1553B standard was chosen for the serial link. The ADC module, the Remote Terminal (RT) module and power supply modules were housed in an Eurocard Compac case or a 19" Subrack. The CAMAC 1553 controller module is located in a CAMAC crate along with the CAMAC 190 MADC controller module. The 190 module sends a channel number and a strobe to the 1553 module, and it waits. The 1553 module executes a 1553 cycle, sending a command to the RT module and receiving status and data words from the RT module. The 190 module then reads the data from the 1553 module. The entire read cycle takes approximately 100 us. The 1553 data bus consists of a single run of a twinaxial cable (RG108A/U) terminated at both ends of the cable. The RT modules and the controller are passively coupled to the data bus using transformers and isolation resistors. One 1553 controller can control up to 30 RT modules. The components of the 1553 based 14 bit ADC system are shown in Fig. 2.

CC130 MADC controller module

The CC130 MADC controller module was designed for the Main Ring control system by M. McGown back in 1978. This design was the first attempt to store digitised MADC data into a local memory so that the front end computer could empty the buffer memory by reading the data at its convenience. This module was designed with TTL logic circuits without using any microprocessor. However, it performs a variety of things.

(1) Single channel read (two single channels).
(2) List read via block transfer.
(3) Storing up to 2048 words for up to four channels, with programmable sample rates, with internal or external arm/ disarm.

CAMAC 190 MADC controller module

The CAMAC 190 MADC controller module was initially designed for the Tevatron control system

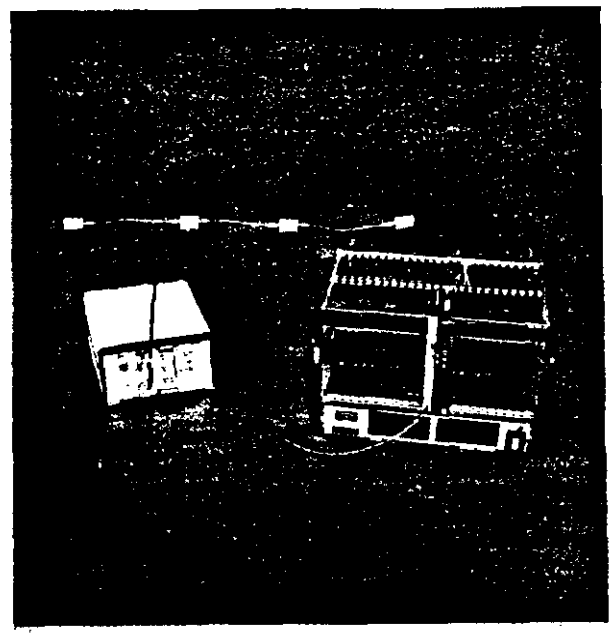

Fig. 2. Components of the 1553 based 14 bit ADC system.

by W. Knopf, A. Thomas et al. in 1983 and 1984 [2]. This design was done in a sophisticated way using Zilog Z8002 microprocessor, Intel 8089 I/O processor, Tevatron clock decoder, timers and others. It is versatile and can be operated in many different ways. The following summarizes the main features of this module.

(1) Six plot channels of time-stamped recording in pre-trigger, post trigger or continuous collection mode. Simultaneous non-interfering collection on all six plot channels with sample rates up to 2.1 KHz per channel. Single plot channel with sample rates up to 70 KHz.
(2) Up to eight lists of time-stamped readings of all channels (or contiguous subset of channels) collected at specified times.
(3) Local alarm monitoring of any data collected in list mode.
(4) Arm and trigger on all modes utilizing combinations of external inputs, coded clock events and programmable internal rate generators.
(5) Internal decoding of events on the Tevatron clock.
(6) Data read via the Tevatron block transfer at the maximum rate of 285 KW/ sec.
(7) Full support for MADC with up to 128 analog inputs.

Other ADC systems

M. Shea designed and installed the LINAC (Linear Accelerator) control system using IBM's SDLC (Synchronous Data Link Control). For the LINAC control system, he used commercial ADC boards (Datel ST800-S32, Multibus) in noisy areas, and he designed and built ADC chasses for less noisy areas. The chassis receives 16 analog input signals via two 8-pin coaxial connectors. Each channel of analog signals is routed to a sample/ hold amplifier (Harris 2425), and the outputs of these amplifiers are input to a 16 channel multiplexed ADC (Analogic 6812). The digitised output is buffered with tri-state devices and routed through 50 conductor connectors and cables. A multiple of chasses are daisy-chainned and

connected to a binary I/O board in a Multibus crate. The binary I/O board sends out a chassis/ channel address and a strobe, and it reads data from the chassis.

J. Zagel designed multiplexed ADC boards using Analog Devices AD571s (10 bit, 25 us), and he installed them on his vacuum control system. One board accommodates from 8 to 16 analog channels, and all channel readings are updated approximately once every two seconds.

J. Zagel purchased and installed 64 channel, multiplexed ADC, Multibus boards (ADAC 735, 12 bit, 20 us) on his refrigeration control systems. In addition to the ADC boards, he designed and installed buffer amplifier boards in order to protect the ADC boards from overvoltages and to provide a low impedance interface to the ADC boards. Average values of from 8 to 12 readings per channel are displayed on the console system, and the display is updated approximately once every two seconds.

Analog boxes were designed using 8 bit flash ADCs (TRW TDC1001), and they were installed for beam position/ loss monitor systems. The analog box consists of a mother-board and twelve daughter-boards, each of which has two ADC channels. Readings are taken at every turn of the beam.

Console application programs

Parameter program

The parameter program provides display of MADC readings along with settings, analog alarm limits and digital status on the consoles of the Fermilab accelerator control network. The parameter program is connected to 70 parameter pages. Parameter pages can have a few or many subpages, one of which is displayed at a time. Subpages can display up to 25 parameter lines. The device name and descriptive text are displayed on the left side of a parameter line. Live data for the device is displayed on the right side of the line. The numeric data can be scaled into three different units - hexadecimal, MADC volts or engineering units (Amps, Deg K, KV, etc.). The color of a reading value is used to show its alarm status. Alarm limits can be changed by typing in new values. Device settings can be changed by typing in new values or by turning a knob. Digital control (on, off and reset) is also provided.

Fast time plot program (Continuous)

The Fast Time Plot utility (FTP) program allows the operator to plot up to four analog channels (analog reading versus time or fifth analog reading) in real time on the storage scope or the color graphic monitor which are parts of the console system. Data collection rates go up to 720 Hz, and plots are updated at a minimum rate of 3 Hz. Data are scaled to primary units (MADC Volts, etc.) or engineering units (Amps, Deg K, Rads/ sec, etc.). Analog readings can be combined into simple expressions using add, subtract, multiply and divide operators before being plotted.

In order to start up plots, the operator first specifies necessary options and parameters, and then clicks in a certain area of the plot interface window, which can be included in any console

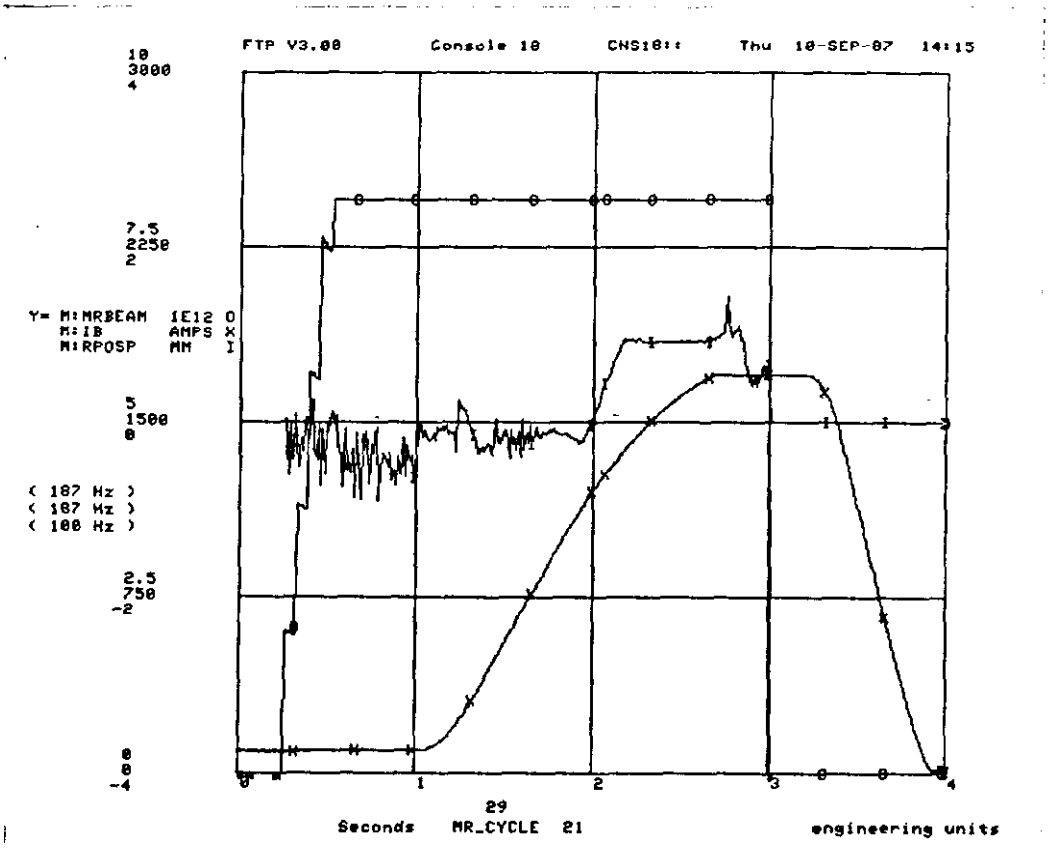

Fig. 3. Sample continuous fast time plot.

application program. Specifyable parameters and options are as follows.

(1) Data sample rate: 1 Hz, 15 Hz, 50 Hz, 100 Hz, 200 Hz, 360 Hz, 720 Hz, Auto, Event.
(2) Time base: Repeat on every Supercycle, every Main Ring cycle or every Tevatron cycle; repeat on selected Main Ring cycles; once.
(3) Scaling: Volts, Eng-U, log.
(4) Data display: connect points with lines, plot characters, blink data from most recent cycle

Fig. 3 shows an example of continuous FTP. For further details on the parameter program and the continuous FTP program, the reader should refer to [3] and [4].

Fast time plot program (Snapshot)

This program has not been implemented as of this writing. However, an outline of the draft on snapshot plots is presented here.

Snapshot plots will plot data collected at rates faster than those available with continuous plots. Snapshot plots will be supported with CAMAC 190 modules and possibly other data sources which will use data formats similar to the 190 modules. In order to run a snapshot plot, the operator will spefify what to plot, the data collection rate and an arm event. A grid will be drawn on his screen, and he will wait. After the arm event, 2048 data points will be first collected at the specified rate by the 190 module, and these data points will be then plotted on operator's screen. Snapshot plots will be automatically restarted after plotting so that fresh data may be collected and plotted at each arm event.

For further details on the snapshot FTP program, the reader should refer to [5].

Practical Issues

Input cables and connections

A twinaxial cable such as RG108A/U is generally recommended. Because it maintains differential connections from the source to the MADC, and because some common mode noises are rejected at the MADC. A polarity convention for twinaxial cable connections needs to be established. The Accelerator Controls department of the Fermilab has a standard "The convention for twinaxial cable connections is pin for high and socket for low." Connectors need to be terminated onto the twinaxial cable in a proper way using right tools. Proper termination of connectors onto the cable is crucial to system reliability.

Source and its impedance

The source needs to be properly grounded. Because the inputs of the MADC amplifier lose their leakage paths, and thus the output voltage of the amplifier is affected by input bias currents.

Many users put a 1 K ohm resistor in series with the output of their buffer amplifiers. They think, if the input resistance of the MADC is much greater than the series resistor, the measurement on their signals is not affected. However, when the MADC switches from one channel to another in a high speed, this is not true. K. Seino analyzed the problem with a SPICE program [6]. The results of the analysis can be roughly explained as follows.

(1) Let R1 = Source Resistance, C1 = Cable Capacitance, V = Source Voltage, R2 = MADC Resistance thru Multiplexers, C2 = MADC Input Capacitance, V2 = Voltage Left on C2 from Previous Channel.
(2) When the multiplexers have selected a new channel, C2 quickly charges up to a voltage governed by

$$\frac{C1}{C1 + C2} V + \frac{C2}{C1 + C2} V2$$

in speeds related to the time constant R2 * C2.
(3) Then C2 slowly charges up to V following the time constant R1 * C1.

Acknowledgments

R. Klecka played a major role in the production, check-out and installation of over 120 MADC units. He made improvements on the mechanical design of the MADC and the fan-in box. He is currently working on the mechanical design of the next generation MADC.

References

[1] K. Seino, A New Multiplexed ADC Unit, Fermilab TM-931 (December 1979).
[2] A.D. Thomas et al., Fermilab Controls Hardware Release No. 26.2 (March 12, 1987).
[3] J. Smedinghoff, The Fast Time Plot Utility, Fermilab Controls Software Release No. 153.0 (August 8, 1985).
[4] J. Smedinghoff, The Fermilab Accelerator Control System Parameter Program and Plotting Facilities, Nucl. Instr. and Meth. A247 (1986).
[5] J. Smedinghoff, Fermilab ACNET Design Note No. 49.1 (January 6, 1987).
[6] K.C. Seino, The MADC (Multiplexed ADC) - How to Make Connections to It?, Fermilab TM-1453 (May 1987).