BNL 40464

BNL--40464

DE88 003491

OG 979

DESIGN OF A CHARGE SENSITIVE PREAMPLIFIER ON HIGH RESISTIVITY SILICON

V. Radeka, P. Rehak, S. Rescia
Brookhaven National Lab., Upton, NY 11973

E. Gatti, A. Longoni, M. Sampietro
Politecnico di Milano, 32 Piazza Leonardo da Vinci,
20133 Milano, Italy

P. Holl, L. Strüder
Max-Planck Institut, Föhringer Ring 6, 8000 München, Western Germany

J. Kemmer
TU München, 8048 Garching and
MBB GmbH, Postfach 80 11 49, 8000 München 80, Western Germany

Talk given by P. Rehak at 1987 IEEE Nuclear Science Symposium, Sheraton-Palace Hotel, San Francisco, CA, Oct. 19-23; Proc. to be published in IEEE Trans. on Nucl. Sci., 35, No. 1 (Feb. 1988).

DESIGN OF A CHARGE SENSITIVE PREAMPLIFIER ON HIGH RESISTIVITY SILICON

V. Radeka, P. Rehak, S. Rescia
Brookhaven Nat. Lab., Upton, N.Y., 11973.

E. Gatti, A. Longoni, M. Sampietro
Politecnico di Milano, 32 Piazza Leonardo da Vinci, 20133 Milano, Italy*.

P. Holl, L. Strüder**
Max-Planck-Institut, Föhringer Ring 6, 8000 München, Western Germany.

J. Kemmer
TU München, 8048 Garching and
MBB GmbH, Postfach 80 11 49, 8000 München 80, Western Germany.

ABSTRACT

A low noise, fast charge sensitive preamplifier was designed on high resistivity, detector grade silicon. It is built at the surface of a fully depleted region of n-type silicon. This allows the preamplifier to be placed very close to a detector anode. The preamplifier uses the classical input cascode configuration with a capacitor and a high value resistor in the feedback loop. The output stage of the preamplifier can drive a load up to $20pF$. The power dissipation of the preamplifier is $13mW$. The amplifying elements are "Single Sided Gate JFETs" developed especially for this application. Preamplifiers connected to a low capacitance anode of a drift type detector should achieve a rise time of $20ns$ and have an equivalent noise charge (ENC), after a suitable shaping, of less than 50 electrons. This performance translates to a position resolution better than $3\mu m$ for silicon drift detectors.

1. Introduction

A relatively new type of semiconductor detectors, Semiconductor Drift Detectors[1] have a very low anode capacitance. Typical values for multianode detectors and for large area cylindrical detectors are about $70fF$. This very small value of the detector capacitance should lead to a very low noise performance which was really observed[2]. Until now, however, tests were done using electronics constructed from the best commercially available discrete transistors. The input capacitance of the smallest available FET 2N 4416 is about $4pF$. The total input capacitance achieved with a 2N4416 FET as the first transistor was $6pF$. Thus there is a factor of 100 mismatch between the low output capacitance detector and the input capacitance of commercially available FETs.

The realization of the first amplification stage directly on the wafer of the detector has two advantages

1. the input transistor can be made small enough to match the small detector capacitance,
2. stray capacitances due to the connection between the detector anode and the first transistor can be kept at a minimum.

The realization of matched preamplifiers with a minimum stray capacitance should decrease the noise of the detector-preamplifier system, resulting in a substantial improvement of energy and position resolution of silicon drift detectors and fully depleted Charge Coupled Devices (CCDs).

For spectroscopic applications the estimated noise of a cylindrical large area drift detector operating at room temperature is about 50 electrons r.m.s. which corresponds to an energy resolution of $400eV$ FWHM.

A calculated position resolution for a multianode detector of an area of $4 \times 4cm^2$ is about $3\mu m$ in both, x and y direction. This resolution is a factor of three better than the resolution obtained up to now with a commercially available electronics and corresponds to 10^8 pixels achieved with only 500 read-out channels.

Fully depleted CCDs are realizable on the same type of high resistivity silicon material as drift detectors. The designed preamplifier or even a simple source follower realized from designed amplification elements on a fully depleted CCD should have an equal performance as the electronics on standard CCDs.

We believe that the calculated improvements in the performance of the drift detectors and fully depleted CCDs with an

This manuscript has been authored under contract number DE-AC02-76CH00016 with the U.S. Department of Energy. Accordingly, the U.S. Government retains a non-exclusive, royalty-free license to publish or reproduce the published form of this contribution, or allow others to do so, for U.S. Government purposes.

* This research is also supported by the Italian INFN and CNR.

** Also *MBB* GmbH

integrated amplifier are large enough to justify the effort needed to develop low noise, fast electronics on high resistivity detector grade silicon.

The second section describes the basic differences between the traditional electronics and the one under development to satisfy all requirements and constraints due to the different kind of silicon and the technology used for the detector production.

The third section is dedicated to the design of the amplifying elements and to the design of a high value resistor for the preamplifier feedback loop.

In the fourth section the configuration and layout of the preamplifier is described. The results of the circuit simulation by "SPICE" program are shown. The noise analysis of the configuration is presented.

2. Constraints Imposed by the Detectors

Seemingly, there is a wide choice of different devices for the first amplifying element of the preamplifier. The four considered amplifying elements are

1. bipolar transistor
2. depleted base transistor within the very structure of the drift detector anode region
3. MOS FET in all four main configurations
4. junction FET.

A bipolar transistor when used as the first transistor of the preamplifier may add additional noise due to its base current. In order to make the contribution of this base current noise negligible, the beta of the first transistor has to be larger than 10^4. We have the feeling that such transistors are difficult to produce with a relatively high yield.

A depleted base transistor[3] can be incorporated only in a way where holes rather than electrons are carriers of the controlled current in the transistor. The lower mobility of holes as compared to electrons decreases the theoretical performance of the transistor. Moreover, the dimensions of the first transistor are dictated by the geometry of the drift detector. In all considered cases it was not possible to achieve the capacitance matching between the geometrical capacitance of the configuration and the diffusion capacitance of the incorporated depleted base transistor.

A MOS FET suffers from a much lower resistance to radiation damage as compared to other amplifying elements and it has a higher excess 1/f noise. Moreover, the gate oxide of the MOS transistor has to be grown on a $< 111 >$ crystallographic plane rather than on a $< 100 >$ plane as for standard MOS FETs. MOS transistors on a $< 111 >$ plane have a lower performance than the ones on a $< 100 >$ plane.

We have chosen a variation of the junction FET as the amplifying element for the fast low noise preamplifier integrated on the detector material. Junction FETs are still the best transistors for low noise amplification in nuclear spectroscopy. Moreover, the production steps for this kind of transistors can be made compatible with the detector production[4].

There are, however, considerable differences between silicon used to produce detectors and silicon used for the production of standard FET transistors. Silicon used for drift detector production is n-type silicon with a resistivity between 1 and $10k\Omega cm$ (donor concentration $0.5 - 5 \times 10^{12}/cm^3$). The wafer surface is oriented along the $< 111 >$ crystallographic plane.

Silicon used for the production of n-channel junction FETs varies slightly according the manufacturer, however, it is generally p-type, the resistivity being in a range between $1 - 100m\Omega cm$. The surface orientation is $< 100 >$.

There are important constraints for the preamplifier design from the limited choice of production steps compatible with the technology of the detector production. To obtain a very long carrier life time (to keep the leakage current low) there is only one high temperature process in the detector production. No second oxidation, no diffusion and no polysilicon processes are presently possible. The detectors are made mainly by ion implantation[4].

To conclude the list of additional requirements on the amplifying element, we have to realize it close to the anode of the detector. In the anode region the silicon is completely depleted due to the bias voltage on the rectifying junction on the other side of the wafer.

3. Amplifying Elements and High Value Resistors

The geometry and the operation of the "Single Sided Gate JFET" is similar to a standard n-channel MESFET[5] on semi-insulating GaAs.

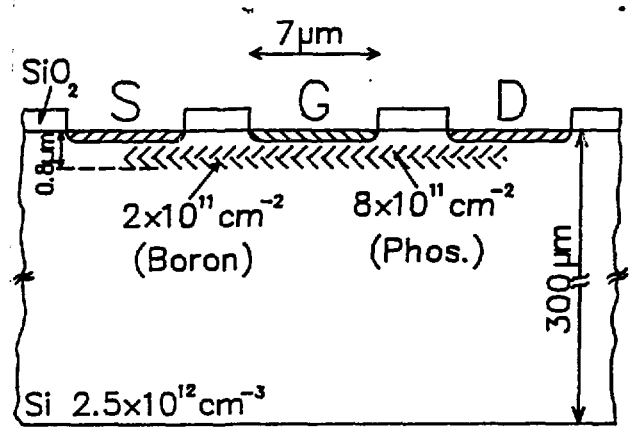

Fig. 3.1: Cross section of a "Single Sided Gate JFET". The gate is indicated by (G), source and drain by (S) and (D) respectively.

The cross section of the JFET realized on high resistivity silicon is shown in Fig. 3.1. The transistor can be called "Single Sided Gate N-Channel FET". The starting material is detector grade n-type silicon with a resistivity of $2k\Omega cm$. The desirable structure is obtained exclusively by ion implantation technique. Different impurity concentrations are implanted at suitable energies and doses. The gate is obtained by a low

energy, high dose Boron implant. Drain and source terminals are low energy, high dose Phosphorus implants. The FET channel is realized by a deep high energy ($520keV$) low dose ($8 \times 10^{11} cm^{-2}$) Phosphorus implant. There is also an additional deeper high energy Boron implant ($480keV$) with a total dose of $2 \times 10^{11} cm^{-2}$.

The high energy Phosphorus implant produces a low resistance path between source and drain which is the n-channel as in in a standard n-channel JFET. The function of the high energy Boron implant requires some explanation.

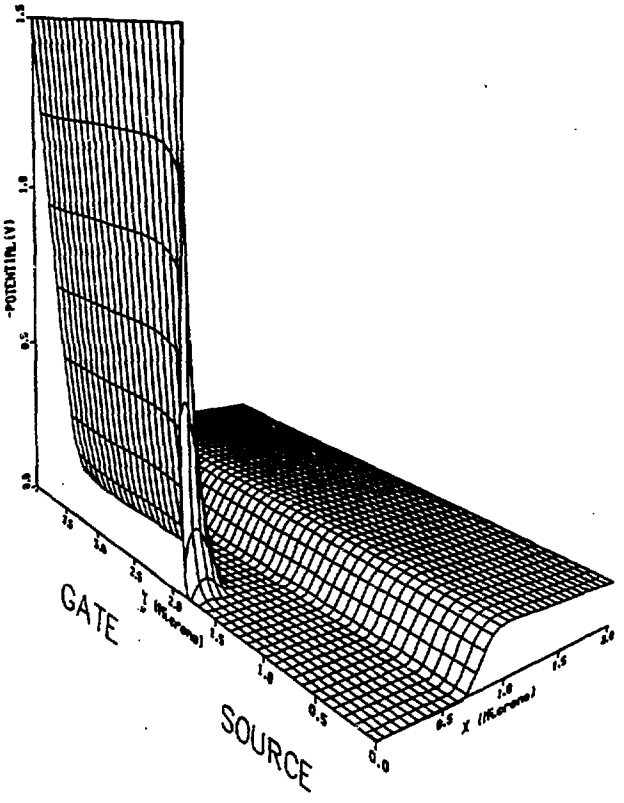

Fig. 3.2: Minus potential of the source and gate region of the transistor with a negative bias applied to the gate and a zero voltage to the drain. Only $2\mu m$ depth is shown.

The implanted Boron forms a p-type region centered about $0.8\mu m$ deep in the silicon bulk. This region is completely depleted from all mobile charges because of the high negative bias voltage of the p^+ implant on the opposite face of the wafer. Fixed negative charges in the lattice of the crystal produce a barrier to retain the electrons within the channel. Fig. 3.2 shows an approximation to the electron potential energy in the source and gate region of the transistor with a negative bias applied to the gate and a zero voltage to the drain.

Characteristics of this kind of transistor were calculated using a complicated 2D code "PROUDS"[6].

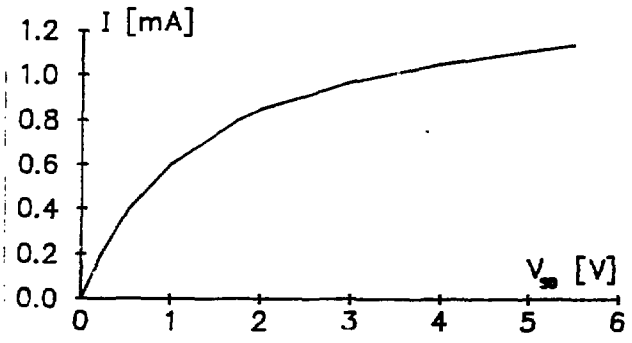

Fig. 3.3: Characteristics of the "Single Sided Gate N-Channel JFET". The width of the transistor is $100\mu m$, the gate length is $7\mu m$. The gate bias for the shown curve is $0V$.

The I_D curve of the transistor for the gate bias of $0V$ is shown in Fig. 3.3 (to produce this curve 70 hours of CPU on CRAY-XMP supercomputer were used). By comparing characteristics simulated for different gate voltages we were able to estimate the transconductance of the transistor. The transit time of an electron in the channel was calculated to be about $300ps$.

The pinch-off voltage of a "Single Sided Gate JFET" cannot be designed to be low without compromising low gate leakage current requirements. The reason can be seen in Fig. 3.2. The mobile holes of the gate have a tendency to diffuse against the negative potential into the channel region. The tail of the hole distribution in the gate may overcome the potential barrier of the channel and be swept to the opposite side of the wafer. The escape of holes would contribute to the gate leakage current.

To prevent the diffusion of holes into the channel region the gate must operate at a relatively high negative voltage as compared to the channel voltage. This means, that the pinch-off voltage is high. The design value is about $3V$. This value of pinch-off voltage dictates the energy of the deep Phosphorus implant. A higher value of the pinch-off voltage means higher power dissipation of the preamplifier.

We can see that the output impedance of the FET in the saturated part is not very high. Against our intuition the output impedance in a part of the characteristics used for amplification is not affected by the presence of the implanted Boron barrier. The simulations of characteristics in configurations with and without the barrier gave a similar value for the output impedance. The transistor with the implanted Boron barrier has, however, a much sharper voltage cut-off. This feature is important for switching applications and for the operation of the device at small current densities. The relatively low value of the output impedance is due to the penetration of the electric field from the drain to the channel region through the depleted region of the silicon bulk.

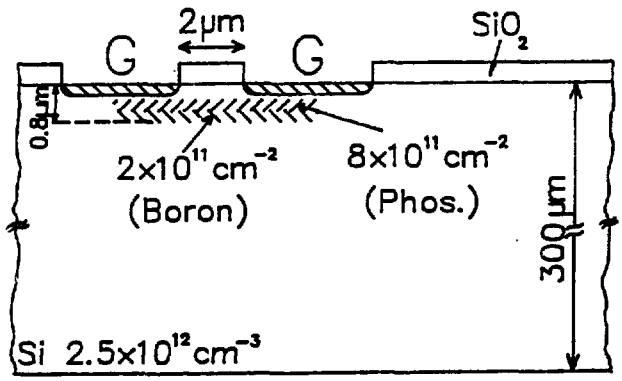

Fig. 3.4: Cross section of the high value feedback resistor. The implanted layers are identical to the layers of the transistor.

The cross section of the high value feedback resistor is shown in Fig. 3.4. The current flow is perpendicular to the paper plane. The length of the resistor in this direction is $250\mu m$. The high energy implants are obtained at the same time as the implants for the transistors.

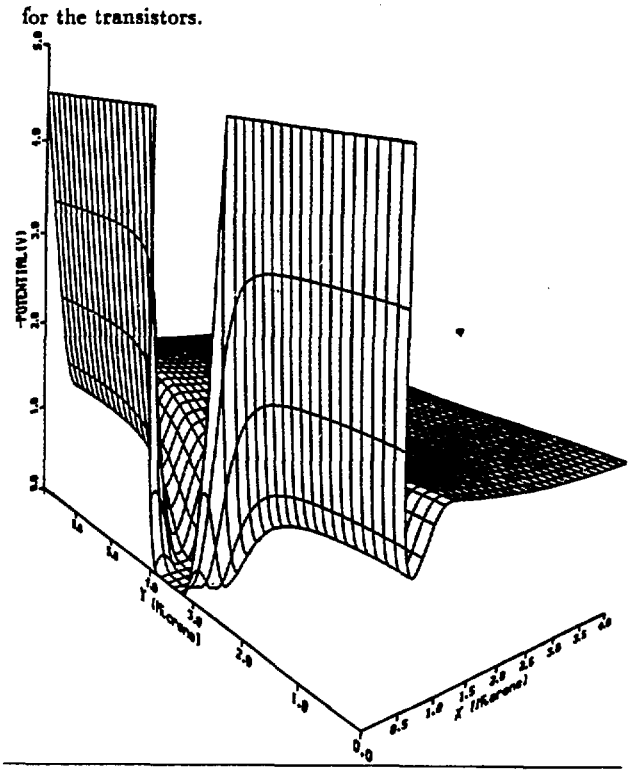

Fig. 3.5: The minus potential in a resistor cross section. Current flows in a direction perpendicular to the paper plane.

The minus potential of the resistor cross section is shown in Fig. 3.5. The silicon is not depleted right under the $Si\text{-}SiO_2$ interface where the current flows. The resistance per unit length is related to the number of mobile carriers in this undepleted region by

$$R = 1/(n\mu q),$$

where n is the linear density of mobile electrons in the undepleted region of the resistor; μ is the electron bulk mobility; and q the electron charge (positive).

We can change the number of mobile electrons and thus the resistivity by applying a different bias on the resistor gate. With a gate bias of $-4V$ the total resistance is about $10M\Omega$. The capacitance per unit length is the derivative of the mobile charge with respect to the gate voltage. The capacitance is only a weak function of the voltage. Its value is about $0.3fF/\mu m$.

The above numbers for the resistance and the capacitance include also the contribution of the conductive channel along the $Si\text{-}SiO_2$ interface. The interface is not depleted because of the presence of positive charges in the SiO_2 close to the interface. We have considered to use this "surface conductivity" for the realization of high value resistors. We preferred to realize the resistor within the bulk for the very same reason, that we have preferred JFET rather than MOSFET.

4. Charge Sensitive Preamplifier

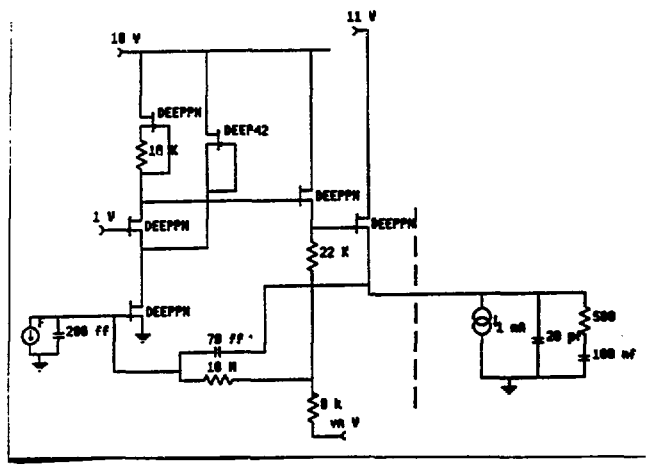

Fig. 4.1: Charge sensitive preamplifier on high resistivity silicon.

Fig. 4.1 shows the diagram of the charge sensitive preamplifier. It is a slight variation of a classical cascode with a Darlington follower using only the previously described n-channel FET. There is one more transistor connected as a current source to supply an additional current to the input transistor. The input transistor has a three times higher steady current than the grounded gate transistor and the transistor resistor combination used as a load for the cascode. The smaller current in this path allows a realization of a higher open loop gain.

The capacitive feedback is taken from the source of the output transistor to improve the linearity of the circuit. The DC feedback through a $10M\Omega$ resistor is applied after a resistive division of the output voltage of the first follower. This division $8/(22+8)$ which provides a voltage level shifting also increases the decay time constant of the amplifier.

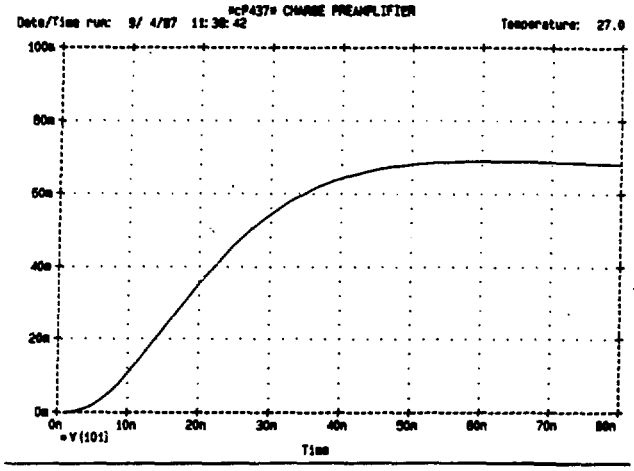

Fig. 4.2: Impulse response of the charge sensitive preamplifier. Fast time scale.

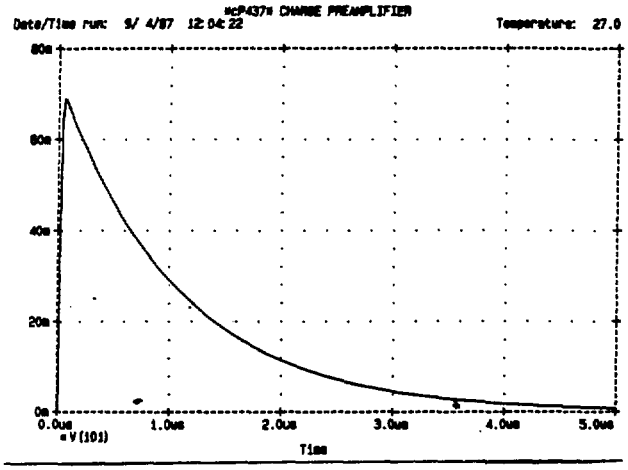

Fig. 4.3: Impulse response of the charge sensing preamplifier. Slow time scale.

The "SPICE" simulated impulse response of the preamplifier is shown in Fig. 4.2 and Fig. 4.3 for two different time scales. The rise time is about $23ns$; the decay time constant is $1.5\mu s$. The waveform is similar to the output waveform of the previously used discrete components preamplifier which allows us to use the same signal processing electronics.

The noise of a well designed preamplifier is dominated by the noise of the input transistor. In this variation of the cascode configuration the transistor connected as a current source for the input transistor and transistor resistor combination used as the load contribute to the total noise. With the designed values the total contribution of all other noise sources adds 20% to the noise of the first transistor.

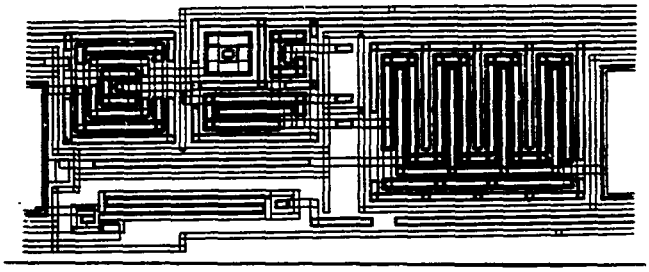

Fig. 4.4: Layout of the charge sensitive preamplifier.

Fig. 4.4 shows the layout of the amplifier. The input bond pad (on the left hand side) and the output bond pad (right) are not fully shown. The individual transistors are realized in self closed rectangular patterns and are more complicated than simple crossing realizations of MOS transistors. At the upper left side there is the input cascode realized in a concentrical geometry. A large output transistor on the right hand side occupies almost one half of the preamplifier surface.

5. Conclusion

The integration of front end electronics seems possible on high resistivity silicon wafers suitable for fully depleted radiation detectors. The integration of this electronics promises a large improvement in the performance of detectors with very low anode capacitance.

6. References

1. E. Gatti and P. Rehak, Nucl. Instr. and Meth. 225, 608 (1984).
2. P. Rehak et al., Nucl. Instr. and Meth. 248, 367 (1986).
3. J.M.C. Stork and J.D. Plummer, IEEE Transactions on Electron Devices, ED-28, 1354 (1981).
4. J. Kemmer et al., Nucl. Instr. and Meth. 226, 733 (1982).
5. S. M. Sze, Physics of Semiconductor Devices, New York: John Wiley & Sons, 1981, p. 338..
6. M. Berger and E. Stein, Nucl. Instr. and Meth. A253, 382 (1987).