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Precision Charge Amplification and Digitization System for a Scintillating and Lead Glass Array*

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PRECISION CHARGE AMPLIFICATION AND DIGITIZATION SYSTEM FOR A SCINTILLATING AND LEAD GLASS ARRAY

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ABSTRACT

A 544-channel low-noise, high-rate, precision charge amplification and ADC system was constructed for the Fermilab Experiment 705 electromagnetic calorimeter, which employs SCG1-C scintillating glass and SF5 lead glass instrumented with photo-multiplier tubes. A general discussion of the system is given, and the charge amplification, fast trigger pulse generation, and analog to digital conversion aspects of the system are presented in more detail. Performance is evaluated using data from Experiment 705 and from off-line tests. Short and long term pedestal stability, baseline recovery and rate capability, linearity of response, and crosstalk between channels are discussed.

System Overview

The accurate detection and measurement of photons over a large range of energies is central to the goals of Fermilab Experiment 705 [1,2], which took data with a high mass dimuon trigger and a large transverse energy trigger from June of 1987 to February of 1988.

The dimuon trigger selects events containing muon pairs with mass greater than 2.4 GeV/c^2; these events are reconstructed and inspected off-line for J/ψ (3097) candidates. Reconstructed J/ψ's are combined with photons in an attempt to reconstruct the radiative decays of the χ_1 (3510) and χ_2 (3555) charmonium states. For Experiment 705, the photons from these decays lie in the 1-30 GeV energy range. Excellent energy resolution, on the order of several percent, is necessary if the χ_1 and χ_2 states are to be resolved.

The large transverse energy trigger selects events which are likely to contain large transverse momentum photons, some of which result from hard collisions between the quarks and gluons in the target and beam particles. These photons can have energies in excess of 200 GeV in the kinematical region probed by Experiment 705.

To measure photon energies and positions (and therefore momenta), a large acceptance electromagnetic calorimeter was constructed as part of the Fermilab High Intensity Laboratory open geometry spectrometer. The calorimeter consists in part of several arrays of SCG1-C scintillating glass [3] and SF5 lead glass blocks instrumented with photo-multiplier tubes. The SF5 blocks all have cross sectional area 15 x 15 cm^2, while the SCG1-C blocks have either 15 x 15 cm^2 or 7.5 x 7.5 cm^2 cross sectional area.

Photons depositing their energy in the calorimeter produce cerenkov light in the lead glass and cerenkov as well as scintillation light in the scintillating glass. Each photo-multiplier tube produces a charge pulse proportional to the energy deposited in a single block.

The experiment ran at average interaction rates between 300 kHz and 1 MHz. During stable accelerator operation, beam was present over a ~20 second spill followed by a ~50 sec interval without beam. During the spill, the instantaneous interaction rate could be much higher (5 to 10 times) than the average interaction rate. Data were taken at average interaction rates between 2 kHz and 800 kHz, with some running at 1 MHz and 2 MHz. Most running took place at average interaction rates of ~300 kHz and 800 kHz .

A system of electronics was constructed to integrate and digitize the photo-multiplier tube charge pulses in all blocks for interactions of interest taking place in the spectrometer. The same system provided fast output pulses proportional to deposited energy from a subset of the blocks for use in the formation of the large transverse energy trigger [4]. These fast output pulses were also used to obtain time digitized information for energy deposited in the blocks.

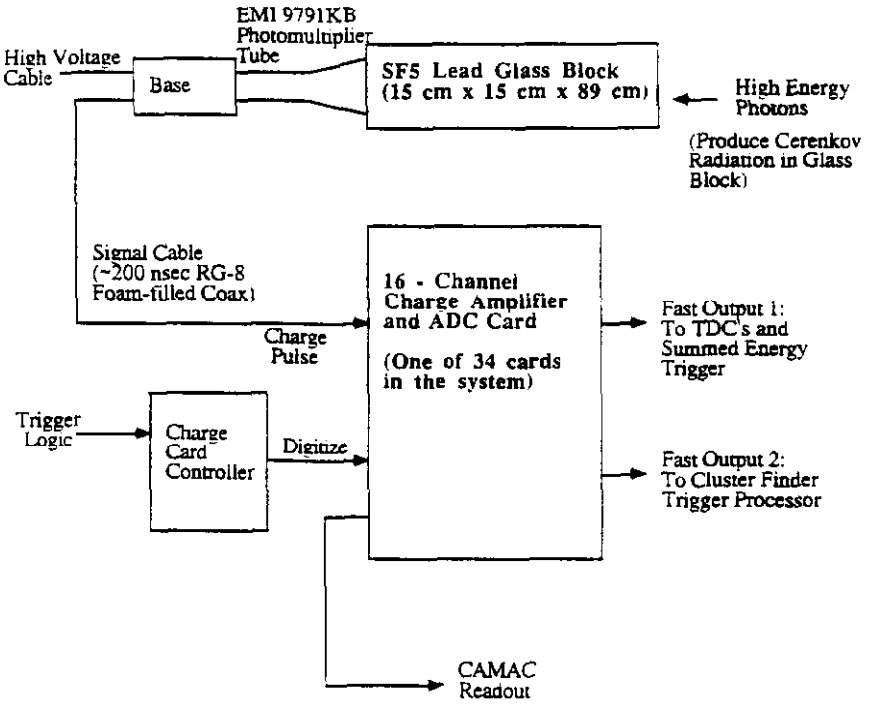

Figure 1. Block Diagram of a Single Channel

Figure 1 shows the electronics associated with a single SF5 lead glass channel in block diagram form. A photon "showers" in the block, giving rise to cerenkov light which is collected by a 5" EMI 9791KB photo-multiplier tube. (3" RCA 6342AV photo-multiplier tubes are used on the small cross section SCG1-C blocks.) The charge pulse produced propagates through a ~200 nsec 50 Ω RG-8 foam-filled coaxial cable to one of the sixteen inputs of a Charge Amplifier and ADC Card. (Shorter lengths of RG-58 and RG-174 coaxial cable are added at the receiving end to achieve equal timing of all block signals.)

The 12 x 20 in^2 multi-layer Charge Amplifier and ADC Cards are housed in three modified CAMAC crates for readout and control. Each crate is powered by its own +24V, -24V, +6V and -6V supplies. Two of the crates in the system contain thirteen cards each; the other crate contains eight cards.

Charge pulses entering a channel are continuously integrated by a charge integrating amplifier. For each input pulse, two fast output pulses proportional to the integrated charge in the input pulse are produced; these pulses are sent directly to the trigger logic electronics and a set of TDC's.

If a positive trigger decision is made and the event is to be read out, a Charge Card Controller module in each of the three crates causes the Charge Amplifier and ADC Cards to store the charge integrating amplifier outputs for each channel from just before and just after the event. The differences between the before and after values, representing the energies deposited in each channel by the event of interest, are then digitized. The integrator output from just before the event is digitized as well.

The digitized values for all channels are read out through CAMAC by a data acquisition program employing "smart" crate controllers designed by members of the McGill University Department of Physics [5].

The Charge Amplifier and ADC Card

Charge Integrating Amplifier

The charge integrating amplifier for a single channel is shown in Figure 2. Components and voltages associated with biasing networks are not shown. Each channel is powered by individually regulated +24 V and -24 V lines. Bias currents to the pair of common base transistors T1 and T2 are supplied through emitter follower networks (not shown) for further filtering.

Transistors T1 and T2 are both normally conducting. The output of slow operational amplifier U1 is the low frequency portion of the input voltage; operational amplifier U2 tries to keep its negative input at this voltage, so that collector voltages of the two transistors are held at the baseline for low frequencies.

The photo-multiplier tube current pulse from an SF5 block has a rise time of ~15 nsec and falls exponentially with time constant ~20 nsec. The signal is therefore dominated by frequencies for which the .022 μF capacitors in series with the emitters of T1 and T2 present very low impedance, and these high frequency components see an input impedance of ~50 Ω (recall that *both* transistors transmit signal current), so that the transmission line impedance is matched. The input current pulse is integrated on the capacitor C_{int}. For the SF5 blocks, C_{int} = 150 pF and R_{int} = 170 Ω (470 Ω in parallel with 270 Ω.)

The value 150 pF for C_{int} is chosen so that the integrated charge from a 100 GeV input pulse will give ~2 V integrated voltage; the largest voltage the channel can digitize is ~2.5 V. The resistor R_{int} is chosen to achieve optimal integration time (~25 nsec from 10% to 90% of full amplitude for SF5) by compensating for the exponential tail of the input signal.

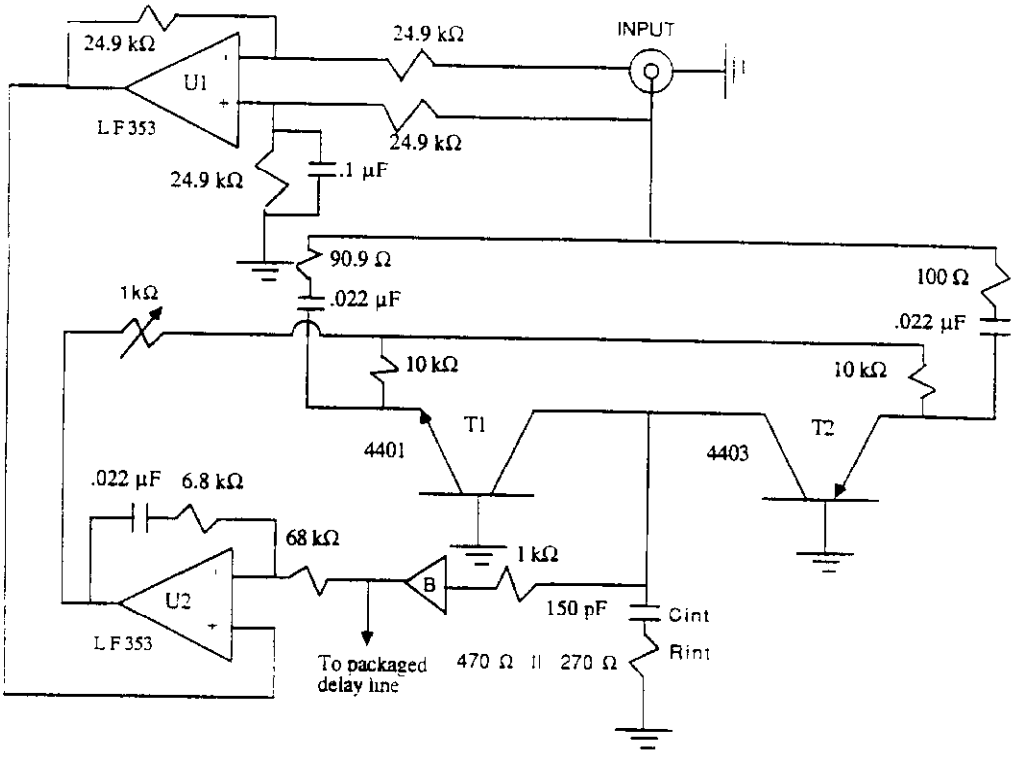

Figure 2. Charge Integrating Amplifier

The high impedance buffer B presents the voltage on C_{int} to the 68 kΩ resistor in series with the negative input of U2. A voltage is produced at the ouput of U2 (~ -.1 times the voltage on C_{int}) which brings C_{int} back to the baseline voltage with time constant ~10 μsec. (This is true only for the fast pulse, for which U2 is effectively in a closed loop configuration with a gain of approximately -6.8 kΩ / 68 kΩ; for low frequencies, the gain of U2 is just its open loop gain.)

The signal shapes for the SCG1-C scintillating glass blocks are different, so that the product of C_{int} and R_{int} is different for SCG1-C channels. Furthermore, it was desired to digitize energies up to 150 GeV in the large cross section SCG1-C blocks and 250 GeV in the SCG1-C blocks with small cross section; C_{int} values of 220 pF and 390 pF respectively were used in these classes of blocks.

Fast Trigger Output and Sample-and-Hold Networks

Figure 3 shows schematically the fast trigger pulse generation and sample-and-hold networks for a single channel. The buffered output voltage of the charge integrating amplifier is presented to a 400 nsec packaged delay line. Signals from the input end of the delay and a 160 nsec tap point are differentially amplified to give a monopolar voltage pulse with amplitude 0-1 V proportional to the integrated charge in the channel. Two output pulses are generated for each channel, both capable of driving a load of 50 Ω.

The shapes of the fast trigger pulses in each channel are adjusted for optimal rise and decay times (e.g. ~24 nsec and ~70 nsec respectively for SF5 channels) and a reasonable plateau (e.g. ~112 nsec at >90% of full amplitude for SF5) so that trigger strobe timing is not critical.

The fast trigger gains of all channels are adjusted so that a 100 GeV test pulse will give a 400 mV amplitude fast trigger pulse. Channels capable of digitizing 250 GeV can then give trigger pulse amplitudes of up to 1 V, the peak output voltage of the difference amplifier's linear range. The DC offsets of the fast trigger outputs are adjusted to within ~1-2 mV of 0 V with a potentiometer adjustment on each channel.

The 400 nsec delay provides the time necessary for the external trigger logic to make a decision, using in part the fast trigger output pulses described above.

The output voltage from the delay package charges two sample-and-hold capacitors C1 and C2 as long as the JFET switches S1 and S2 are closed. If an event is to be digitized, switch S1 is opened at time T1, just before the signal of interest appears at the delay line output, so that the C1 voltage level reflects the state of the charge integrating amplifier output just *before* the event of interest is integrated. Switch S2 is opened 250 nsec later at time T2, so that the voltage on C2 reflects the state of the integrator output just *after* the event of interest is integrated.

The T2 - T1 value is chosen to best match the rise time of the voltage on the sample-and-hold network capacitors C1 and C2. The chosen time of 250 nsec allows the C2 voltage to rise to the full charge integrator output level. For example, it takes 130 nsec for the C2 voltage in an SF5 channel to rise from 10% of its full value to 90% of its full value.

The C1 and C2 voltages are differentially amplified, and the differences for the sixteen channels on the card are sent to the multiplexing and ADC stage which follows. The C2 voltage is multiplied by a gain α slightly greater than unity relative to the C1 voltage before the difference is calculated to compensate for the exponential decay (~10 μsec time constant) of the charge integrating amplifier output between the time at which it is a maximum and time T2.

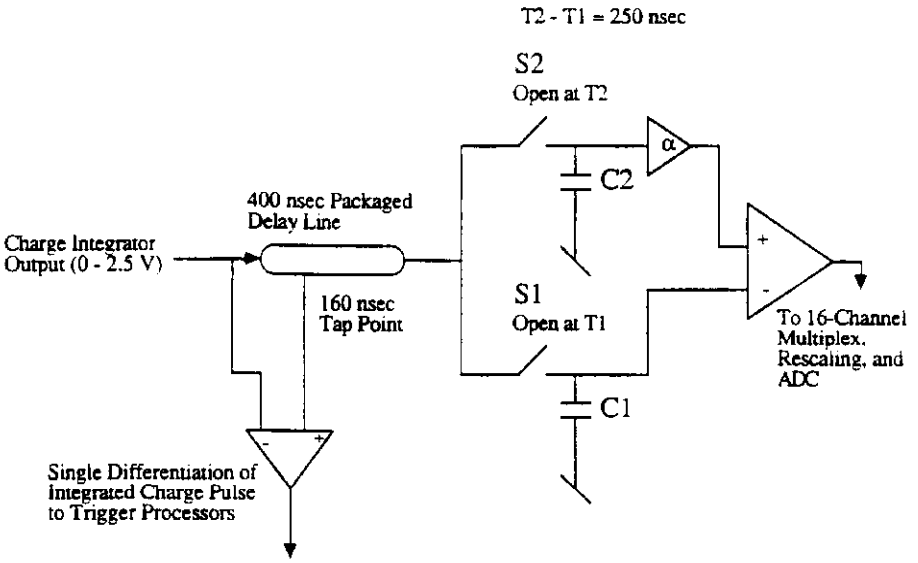

Figure 3. Fast Trigger Output Generation and Sample-and-Hold Networks

The voltage level sent to the multiplexing stage when no input signal was integrated ("pedestal") depends on the leakage charges Q1 and Q2 injected by the JFET switches S1 and S2 each time they are opened. Typically Q1~Q2; the gain factor $\alpha>1$ thus insures that some positive non-zero voltage value will be digitized. (If Q1>Q2 it is sometimes necessary to boost the output voltage level by a fixed amount so that the pedestal voltage will be positve.)

If pedestals are to be stable it is crucial that the leakage charges Q1 and Q2 be the same for each switch opening and not, for example, depend on the time since the last opening of S1 and S2. For one type of analog switch, the Harris CMOS 201HS, the digitized pedestal value was found to be highly dependent on gate frequency, or more particularly, on the time since the last gate [6]. Replacement of the 201HS with another switch, the National Semiconductor JFET LF13201, eliminated this problem, which was a major annoyance in this particular application because of the stringent requirements on pedestal fluctuations, described in more detail later.

The quantity α was adjusted on each channel with a potentiometer before data taking. Proper choice of α optimizes the return to "pedestal" after charge has been deposited. If α is too large, the digitized output will be greater than the nominal pedestal for some time interval following the deposit of charge in the channel, so that an event occuring in this time interval and which deposits no energy in the channel in question will nevertheless measure non-zero energy in the channel. If α is too small, the digitzed value will be smaller than the nominal pedestal or, if non-zero energy is deposited in the channel, the measured digitized value will be smaller than the correct value. In either case, the digitized value will eventually return to the nominal pedestal, on a time scale on the order of μsec.

Analog to Digital Conversion

The output voltages ($\alpha V_{C2} - V_{C1}$) for the sixteen channels of each card are multiplexed to a single Analog Devices 5200 12-bit successive approximation ADC. Before being presented to the ADC, each channel's output voltage is multiplied by a factor of 8 if the digitized value would be less than 1/8 of full scale, or a factor of 1 if this is not the case: in this way, an effective sensitivity of 15-bits is obtained for small signals.

The voltage level of capacitor C1 for each channel is coarsely digitized (3 bits) so that information about the output level of the charge integrating amplifier just before each digitized event is retained.

The digitized values for the sixteen channels are shifted into a FIFO to await read-out through CAMAC. The three crates are read out serially. The readout sequence within a crate is as follows: the FIFO's of the cards in the crate are read sequentially by card, so that all channel 1's are read first, then all channel 2's, and so one until all channel 16's have been read and the crate has been completely read out. In this way, readout can proceed at the full CAMAC rate (1 MHz) even if the ADC digitization rate is much slower.

Cards are typically still digitizing their channels as the crate is being read out; if the FIFO on a card does not have a word available, no Q response is sent from the card and the controller continues to interrogate the card until the ADC has a value ready.

The output from each channel is a sixteen bit word. The lowest twelve bits contain the digitized value (0-4095 counts) of ($\alpha V_{C2} - V_{C1}$) representing the energy deposited in the channel for the event being read out. The thirteenth through fifteenth bits are the digitzed value of the C1 capacitor voltage, representing the baseline subtracted for the event of interest. The sixteenth bit is set ON if the channel's analog output was multiplied by 8 before digitizaton.

System Performance

Pedestal Fluctuations, Energy Resolution, and Noise

Electronic noise from photo-multiplier tubes, base electronics, pickup on coaxial transmission lines, and in the electronics itself will manifest itself as fluctuations in the digitized pedestal for a channel, which may be expressed in digital counts or, of greater interest to the experiment, in energy units.

Pedestal fluctuations enter the fractional energy resolution $\sigma(E) / E$ of a calorimeter as a term inversely proportional to energy E:

$$\sigma(E) / E = (\sigma_{PED} / E) + (A / \sqrt{E}) + B$$

where σ_{PED} is the pedestal width in energy units. A is ~2% for SCG1-C scintillating glass and ~5% for SF5 lead glass, and B is the "systematic term" which represents various errors in energy measurement which are proportional to E. Major contributions to B include uncertainties in relative gains between channels and losses in measured energy due to leakage and albedo.

The contributions to the systematic term B which are due to uncertainties in relative gains between channels are minimized for Experiment 705 by conducting an elaborate set of calibrations in which electrons or positrons of known momentum are sent into every block of the calorimeter. Gain are tracked between calibrations using an LED pulser system which puts light into every block in test triggers taken between spills. (The LED pulser amplitude itself is tracked with three PIN diodes.) The uncertainties in gains are currently ~1%, and better results are hoped for with refinements in the interpretation of calibration data.

If E is the energy of a *group* of channels (typically a photon deposits its energy over no more than 9 blocks, with >90% in four blocks), then σ_{PED} is the sum in quadrature of the pedestal widths for the channels involved, or the algebraic sum if the fluctuations are for some reason "maximally" correlated.

The pedestals are found to be quite stable over long periods of time (several counts over a period of months), as long as the electronics is kept in thermal equilibrium. When a crate is turned on "cold," the pedestals of all channels fall slowly over a period of 20 minutes or so, and then stabilize with widths between 1 and 3 digital counts.

Lack of precision in the digitized value for a charge pulse of a given amplitude would further degrade energy resoluion. Table 2 shows the measured values in digital counts and their sigmas for a full scale test charge pulse over a range of attenuations injected into an SF5 channel. The average and sigma are calculated over 25 digitizations at each attenuator setting. Note that the x10, x100, and pedestal values are in the x8 regime of the ADC card; the x1, x2, and x4 values would normally be multiplied by a factor of 8 off-line. The digitized value is seen to be precise to less than a part in 1000 for the x1 regime and to a few parts in 1000 for the x8 regime.

Table 1. Average Pedestal Widths for SF5 and SCG1-C Block Channels

Block Type	Maximum Energy (GeV)	Average Pedestal Width (counts)	Average Pedestal Width (MeV)
SF5 (15 x 15 cm^2)	100	1.71	5.45
SCG1-C (15 x 15 cm^2)	150	1.54	7.10
SCG1-C (7.5 x 7.5 cm^2)	250	1.66	13.6

Pedestal fluctuations will become a major term in the energy resolution for photon energies on the order of a few GeV if σ_{PED} ~ 100 MeV. It was therefore desired to keep the noise in each channel at the single count level. For the SF5 channels, this corresponds to ~3 MeV, while for the two types of SCG1-C channel a single count is either ~5 MeV or ~8 MeV. The worst case value of σ_{PED} for SF5 for example will then be 27 MeV for nine blocks with "maximally" correlated pedestal fluctuations. (Off-line examination of pedestal data taken during the run shows that pedestal fluctuations are not in fact correlated.) Table 1 shows the measured pedestal widths in digital counts and energy units (MeV) for the three classes of blocks used in the calorimeter.

About one half of a digital count is typically contributed to the pedestal width by the photo-multiplier tube and cable noise. If the charge amplifier is disconnected from the delay package input (see Figure 3), the pedestal width decreases by about .4 digital counts; the sample-and-hold network typically contributes about a digital count to the pedestal width.

Baseline Stability and Rate Capability

To run at average interaction rates up to ~1 MHz it is necessary to insure that the digitized value for a channel will have returned to its pedestal value within ~1 μsec of an event depositing energy in the channel. In addition the sample-and-hold rise time must be short enough to insure that a subsequent event occurring within ~1 μsec of the event of interest will not degrade the digitized value for the event of interest.

Figure 4 shows the digitized response of a single channel to a test pulse with close to full scale amplitude [7]. The ordinate is T1, the opening time of switch S1 (see Figure 3) relative to the time which gives maximal digitzed output. Switch S2 is opened 250 nsec after S1. The rising and falling edges of the response curve reflect the shape of the sample-and-hold network response, in particular its rise time.

Table 2. Repeatability of Digitzed Signal (See Text)

Attenuation of Charge Pulse	Average Digitized Value (counts)	RMS (counts)	Multiplier (pre-digitization)
x1	3676	2.0	x1
x2	1938	1.1	x1
x4	1004	0.6	x1
x10	3473	1.7	x8
x100	702	1.3	x8
Pedestal	397	1.6	x8

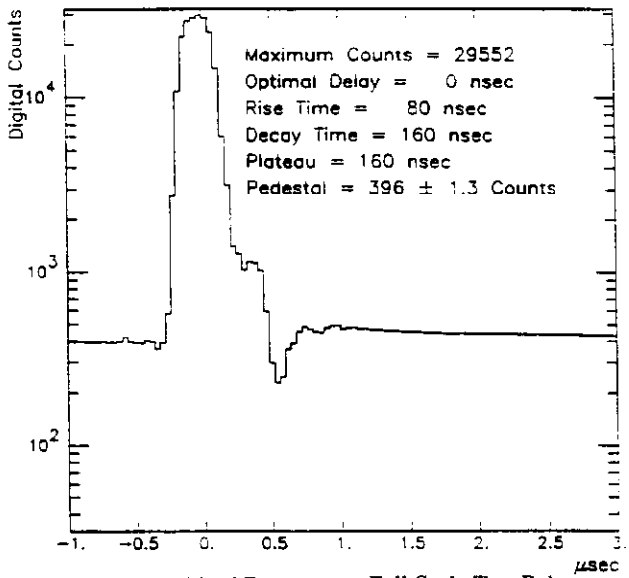

Figure 4. Digitized Response to Full Scale Test Pulse for Various Sample-and-Hold Times

For T1 well before or after its optimal value, the digitized value of ~400 counts corresponds to the channel's pedestal. For T1 within 80 nsec of the optimal delay, a digitized value ≥ 90% of full amplitude is obtained. It is seen that for an event occuring 1.5 μsec after an event depositing *full scale energy* in the channel of interest, the digitized value will be nearly unaffected by the previous event.

For T2 greater than about 1.5 μsec, the digitized value is close but not equal to the pedestal value. By adjusting the relative gains of the C1 and C2 voltages (the gain factor α in Figure 3) the return to baseline may be optimized for each channel. The channel shown is slightly over-compensated for the exponential decay of the integrator output, so that the digitized output value is still returning to pedestal "from above" for T1 = 3 μ sec, the longest delay shown in the plot.

The shoulder and undershoot in the digitized response for T1 near 300 and 500 nsec respectively are caused by a reflection at the amplifier input which propagates back to the unterminated photo-multiplier tube output and back to the amplifier input [8]. This effect is linear with input signal amplitude, and has an amplitude of ~2% relative to the signal.

Linearity of Response

The signal presented to the ADC is intended to be proportinal to the integrated charge in the channel for the event being digitized. As described above, analog values corresponding to less than 1/8 of full scale are first multiplied by a factor of 8; other signals are digitized directly. The departure from predicted linear response for a channel are shown in Figures 5a and 5b.

To generate these plots, the response of a channel was measured for a full scale test charge pulse of the appropriate shape attenuated by a factor between 1 and 90 dB, in steps of .5 dB.

Figure 5a shows the deviation from linearity for the small signal range of inputs, which are multiplied by 8 before digitization. The ordinate is the fraction of full scale charge integrated by the front end amplifier, and so only ranges from "zero" (pedestal) to about .12 (1/8 of full scale). It is seen that the response of the channel deviates only slightly (less than ~1% for the entire range) from a linear least square fit to all the points in the test. The large fractional deviations at the low end of the scale reflect the pedestal width (1.4 digital counts.) The mean pedestal value for this channel is 394 counts.

Figure 5b shows the deviation from the extrapolated line from the x8 region for points in the x1 region (greater than 1/8 of full scale). It is seen that there is some "sag" to the response for large signals, which gradually approaches a deviation from linear behavior of ~ -6% at the largest digitized values.

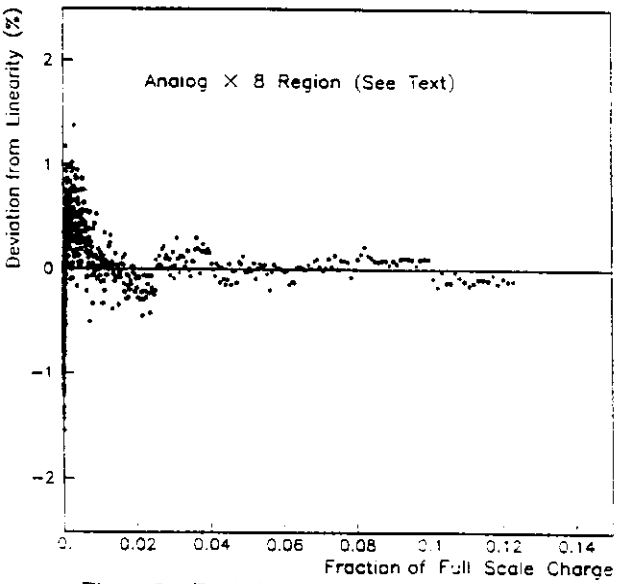

Figure 5a. Deviation from Linear Response to Test Pulse Less than 1/8 of Full Scale

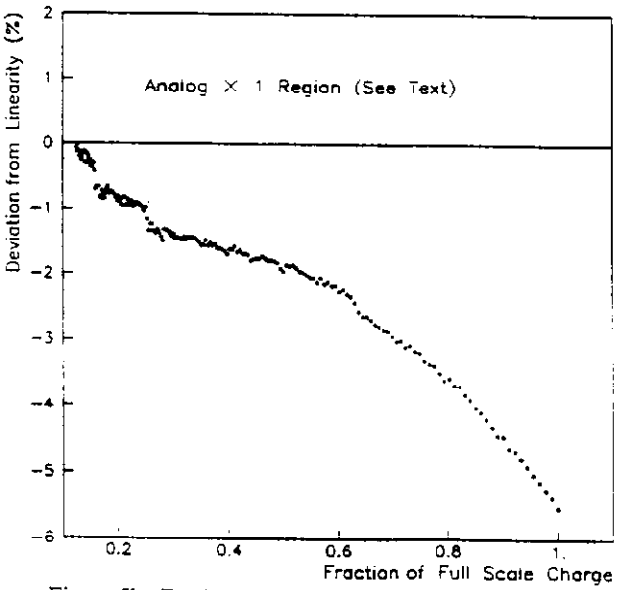

Figure 5b. Deviation from Linear Response to Test Pulse Greater than 1/8 of Full Scale

Crosstalk

In addition to the the pedestal fluctuations described in an earlier section, some inaccuracy in the digitized value for a channel can arise from crosstalk with neighboring channels.

Figure 6 shows the digitized response for a channel when a full scale test pulse is injected into one of the channel's nearest neighbors. A clear bipolar shape relative to pedestal is seen, which is close to pedestal near the "optimal" T1 value, but can be as far as ~40 counts away from pedestal, or about 1.5 parts in 1000 of the signal in the neighboring channel.

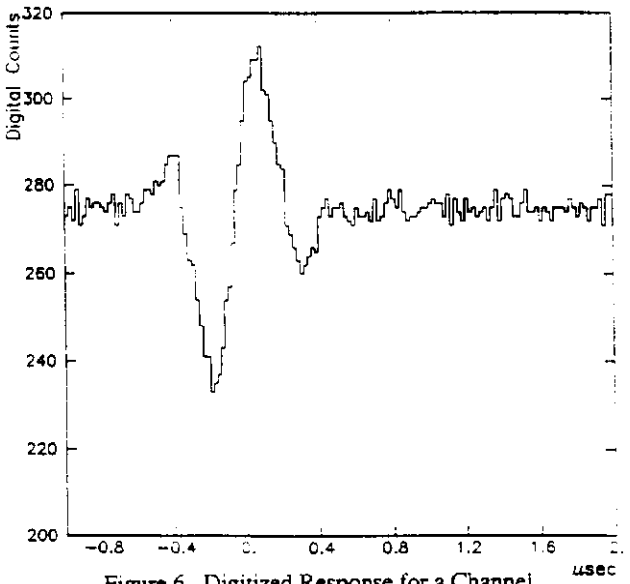

Figure 6. Digitized Response for a Channel When Full Scale Pulse in Injected into A Nearest Neighbor Channel

Channels which are not nearest neighbors on the card are found to have much smaller levels of cross-talk (for example, ~2 parts in 10000 for the next closest channel.) Further tests show that the crosstalk effect is linear; that is, crosstalk is present for nearest neighbor channels at the level of 1.5 parts in 1000 over the entire energy range.

Conclusions

A 544-channel charge amplification and ADC system for a photo-multiplier tube array was successfully operated in the Experiment 705 spectrometer at average interaction rates approaching 1 MHz.

Pedestal fluctuations between ~3 MeV and ~15 MeV per channel were obtained, giving a contribution to the energy resolution of less than ~5%/ E. For example, the energy resolution for single calibration showers is found to be

$$\sigma(E) / E \sim (4.8\%/ E) - (1.8\% / \sqrt{E}) + 1.3\%$$

in the regions employing SCG1-C glass, with the term in $1/\sqrt{E}$ somewhat worse for SF5 glass, as expected. The pedestals were found to be stable to within several digital counts over a period of months.

Off-line tests show that the digitized pedestal value for a channel is unperturbed by a prior or subsequent event depositing full scale charge within 1 μsec of the event of interest. The digitized response of a channel is repeatable at the one or two count level for fixed input amplitude across the entire dynamic range. (After the x1 data are rescaled off-line this spread is somewhat worse of course.)

The digitized response of a channel is linear to within less than 1% for signals less than 1/8 of full scale. For larger signals, the response falls below the value predicted by the small signal fitted slope; the magnitude of the deviation from linear behavior is slowly increasing, reaching ~-6% at the largest digitized values.

Crosstalk is present at the level of 1 part in 1000 for neighboring channels, and 2 parts in 10000 for next to nearest neighbors.

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[6] The effect showed up first as a broadening of the pedestals measured in actual data taking relative to those measured with a test pulser triggering digitization at a fixed frequency. It was then noticed that the pedestals measured at various fixed frequencies, while all quite narrow, differed in their mean values by many counts from frequency to frequency. Finally, it was found that the measured pedestal value depended strongly on the time interval since the last digitization. This dependence appeared to continue out to time scales of minutes. (That is, the measured pedestal after an interval of one minute was different by many counts from the pedestal measured after an interval of say one second.)

[7] All channels were calibrated before data taking so that a test input pulse with the correct shape for the channel and representing the channel's full scale energy would give a digitized output close to 30,000 counts (after multiplying by 8 as described under Analog to Digital Conversion above.) This provided a small "overhead" for each channel of several thousand digital counts above its nominal full scale energy

[8] The photo-multiplier tube outputs were not back-terminated in 50 Ω since this would have spoiled the integration of the low frequency components of the charge pulse as well as the baseline stabilization of the charge integrating amplifier. The shoulder maximum occurs when T2 lies on the (same-sign) reflection appearing on the integrator ouput. The minimum occurs when T1 lies on the reflection. If a test pulse is injected with only a short delay line, no disturbance in the digitized output is seen.