Fermi National Accelerator Laboratory

FERMILAB-Conf-89/118

ACP/R3000 Processors in Data Acquisition Systems*

J. Deppe, H. Areti, R. Atac, J. Biel, A. Cook, M. Edel, M. Fischler,
I. Gaines, D. Husby, M. Isely, M. Miranda, T. Nash, E. Paiva, T. Pham, and T. Zmuda
Fermi National Accelerator Laboratory
P.O. Box 500, Batavia, Illinois 60510

February 1989

*Presented by J. Deppe at "Real Time Computer Applications in Nuclear, Particle, and Plasma Physics," Williamsburg, Virginia, May 16-19, 1989.

ACP/R3000 Processors in Data Acquisition Systems

J. Deppe, H. Areti, R. Atac, J. Biel, A. Cook, M. Edel, M. Fischler, I. Gaines, D. Husby,
M. Isely, M. Miranda, T. Nash, E. Paiva, T. Pham, T. Zmuda

Advanced Computer Program
Fermi National Accelerator Laboratory*
Batavia, IL 60510

Abstract

We describe ACP/R3000 processor based data acquisition systems for high energy physics. This VME bus compatible processor board, with a computational power equivalent to 15 VAX 11/780s or better, contains 8 Mb of memory for event buffering and has a high speed secondary bus that allows data gathering from front end electronics.

Introduction

The Advanced Computer Program (ACP) group at Fermilab has been involved with high performance processors and high speed bus interconnects for a number of years. The resulting ACP systems have been in use as high level trigger processors and data acquisition systems at various experiments[1]. One of the explicit requirements of the system architecture was the ability to integrate the best processors available at any given time. The processors in the ACP-I systems, as they are called now, are based on the Motorola 68020 CPU and 68881 FPU. The processors did not function under any of the 'commercial' operating systems, as all the system level software was provided by the ACP group.

The advent of high performance Reduced Instruction Set Computer (RISC) architecture, with an order of magnitude better performance than that provided by the 68020, made it attractive to upgrade the processors used in the ACP systems. The chip set chosen for this is the R3000 chip set designed by MIPS Computer Systems Inc.

ACP/R3000 Processor

The ACP/R3000 processor board, which is currently at prototype stage, is designed to comply with the VME bus specification Rev. C.1. The processor consists of:

1. 25 MHz R3000 chip set with R3010 FPU,
2. 32 Kb of Instruction Cache,
3. 32 Kb of Data Cache,
4. Fifo Interrupter,
5. Serial port,
6. 8 Mb of main memory with parity,
7. VME bus A-32/A-24/A-16, D-32/D-16/D-8 single transfer Master/Slave interface,
8. VME bus A-32, D-32 block transfer Master/Slave Interface,
9. VME bus interrupt generator and handler and
10. ACP defined Xbus for memory expansion.

Physically, the processor consists of two boards, a memory mother board implementing features 6 through 10 and a CPU daughter board implementing the rest. Together, they occupy one VME bus slot. A block diagram of the processor board is shown in figure 1.

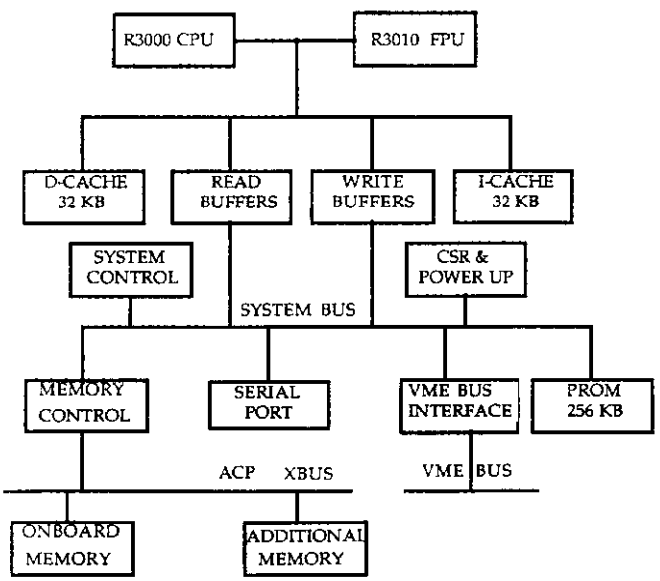

Figure 1. ACP/R3000 Processor Block Diagram.

* Work supported by the U.S. Department of Energy under contract #DE-AC02-76CH03000.

ACP/XBUS

Memory expansion to the processor is accomplished through the ACP/Xbus interface. The ACP/Xbus is essentially the main memory bus with the addition of arbitration logic and has the following features:

1. It uses the A and C rows of the VME bus P2 connector,
2. It implements byte parity on all data transactions and
3. It supports up to four master/slave modules.

An ACP/R3000 memory board provides a convenient way of expanding the physical memory, without increasing the VME bus usage. Up to three memory boards may be connected to the processor, through the ACP/Xbus mechanism, providing a total of 32 Mb of physical memory. The dual data path of VME bus and ACP/Xbus provides a peak transfer rate of 20 Mb/s minimum and a maximum rate that depends on system configuration. In addition, the ACP/Xbus allows as many as four ACP processors to be clustered together and share the available resources.

In addition to being used for memory expansion, the XBUS interface can be used as an auxiliary data path for outside communication. This is the feature that makes the ACP/R3000 attractive in on-line data acquisition applications.

Software Support

The software support for the ACP/R3000 is comprehensive. At the lowest level, a monitor, which resides in PROM , provides basic functionality. The monitor is provided by MIPS and is modified for this board. It includes power up tests and handles the booting of the machine. It has some disk access capability, and it can load from cartridge tape. Its main function will be to boot the UNIX™ operating system, which is also provided by MIPS. The source code is currently being modified for the port to this board. The port will be a full implementation of this UNIX, which is based on System V and includes most of the Berkeley upgrades.

Another important feature is the diskless boot, which is needed when booting multiple processors. One processor boots from the disk , and the other processor boots from the first, using it as a disk server. The result is that only one disk is needed in a multiple processor system.

Networking software that will be supported includes TCP/IP over VME and the ACP Branch Bus, and NFS.

At the highest level of software support, the ACP Cooperative Process Software (ACP/CPS) handles the division of jobs into processes that can run on multiple nodes. This software handles the communication between processes. Features such as remote subroutine calls allow code running on one processor to call a subroutine that runs on another processor, with all parameter passing handled automatically and transparently to the programmer. Besides running on the ACP/R3000 boards, ACP/CPS runs on VAX and assorted workstations such as Sun and Silicon Graphics. This allows jobs to be split over different machines, if desired.

The ACP/CPS system consists of a job manager and a set of subroutines that provide for inter-process communication.

Compilers provided by MIPS for the R3000 include C and FORTRAN. The FORTRAN compiler is comparable in features and quality to VAX FORTRAN.

Applications

High performance data acquisition systems require large data transfer rates along with powerful processors. The ACP group has designed a high speed differential bus, called the branch bus, as a means of interconnecting crates of CPUs. The bus has a peak transfer rate of 20 Mb/s and implements byte parity. A number of modules, called Branch Bus Controllers (BBCs) have been developed by the ACP group. These controllers allow QBUS, Unibus, or VME bus based processors to be branch bus masters. These modules are available commercially from Omnibyte Corporation. A Fastbus based Branch Bus Controller, developed at Fermilab is also in existence. Once the high speed interconnect scheme is in place, a number of systems for various on-line applications may be developed.

The Collider Detector at Fermilab (CDF) experiment employs an ACP-I system on-line, as a level 3 trigger processor [2]. This system is shown in figure 2. A number

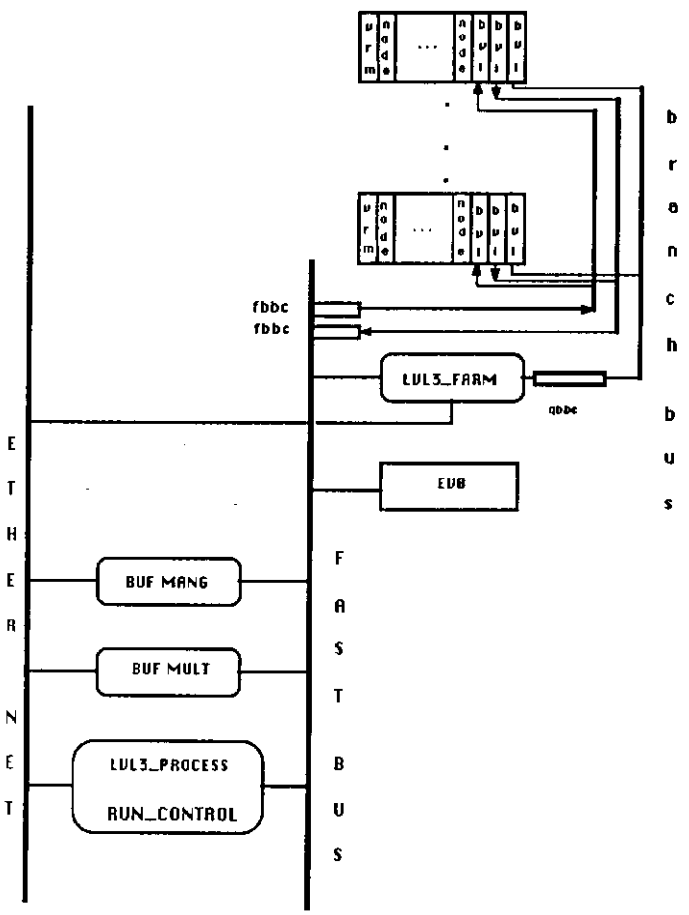

Figure 2. CDF Data Acquisition Diagram.

of VME crates, housing the 68020 based CPU boards, are connected to the event builder via the branch bus. While the data transmission and retrieval mechanism into the system is dependent on the needs of the experiment, the system architecture is quite general. A study of this type of system shows that its efficiency as an on-line filter depends on the data flow mechanism through the system and the processing power of the CPUs. In most cases, the data flow is not the restricting factor, and the performance of the system improves with the power of the CPUs.

An obvious upgrade to the systems of this type is accomplished by replacing the 68020 CPUS with the ACP/R3000 CPUs. The advantage of the R3000 based systems are: an increase in processing power (a factor of 20 over the 68020 based systems), larger physical memory and most importantly, the ability to run more sophisticated software. Since FORTRAN is the language of choice for most physicists, the availability of a superb compiler for the ACP/R3000 is a tremendous advantage. The software tools available for this processor make system and application software development easier.

The large amount of physical memory available to the user of the ACP/R3000 may be used to buffer event data from experiments. As an example, consider a small data acquisition system with one VME crate of ACP/R3000 processors and an interface to a data logger (magnetic tape, 8mm video cartridge, etc.). One of the processors is assigned supervisory tasks, such as event building, data logging, and monitoring, and the rest are assigned to data processing. The event data from various pieces of the experimental apparatus are sent to the processors, except the supervisor. Thus, each CPU has the responsibility of processing data from a particular part of the apparatus. The data port is the ACP/XBUS port, freeing the VME bus for the data logging and supervisory processes. This system is shown in figure 3.

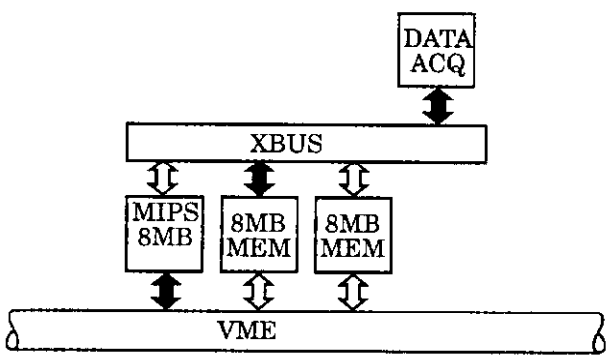

Figure 3. XBus used for I/O.

This system can accommodate the case where the supervisory tasks require more power than one CPU can provide. Added CPU power is obtained by clustering up to four ACP/R3000 CPUs on the ACP/XBUS. This is also shown in figure 3.

In conclusion, the ACP/R3000 CPU, with its dual bus (VME and ACP /XBUS) scheme and the sophisticated high level software support, is well suited for high performance data acquisition trigger processing applications.

References

[1] R.Hance, et. al., "The ACP Branch Bus and Real Time Applications of the ACP Multiprocessor System", IEEE Transactions on Nuclear Science, August 1987, vol. NS-34, Number 4, p.878.

[2] B. Flaugher, et. al., "Integration of the ACP Multiprocessor Farm with CDF Fastbus Data Acquisition System", IEEE Transactions on Nuclear Science, August 1987, Vol. NS-34,Number 4, p. 865.