Fermi National Accelerator Laboratory

TM-1606

A New Semicustom Integrated Bipolar Amplifier for Silicon Strip Detectors

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July 11, 1989

Operated by Universities Research Association, Inc., under contract with the United States Department of Energy

A NEW SEMICUSTOM INTEGRATED BIPOLAR AMPLIFIER FOR SILICON STRIP DETECTORS

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The QPA02 is a four channel DC coupled two stage transimpedance amplifier designed at Fermilab on a semicustom linear array (Quickchip 2S) manufactured by Tektronix. The chip was developed as a silicon strip amplifier but may have other applications as well. Each channel consists of a preamplifier and a second stage amplifier/shaper with differential output which can directly drive a transmission line (90 to 140 ohms). External bypass capacitors are the only discrete components required. QPA02 specifications are shown in Figure 1.

QPA02 is designed to have a large impulse gain (17 mv/fc with output terminated). This insures an output signal which is much larger than external noise pickup on the output cable, and allows the output to directly feed a discriminator. The impulse response is designed to peak in about 10 ns and return to baseline in another 20 ns (base to base is about 30 ns), for an input (detector) capacitance of 20 pf. The impulse response is quite sensitive to the value of input capacitance, so ideally all channels of the detector should have similar capacitance values. Process variations in on-chip resistance also have an effect on the impulse response of the chip. To compensate for this, a scheme has been developed which uses deposited nichrome resistors on the chip that can be laser trimmed. Process variations can thus be compensated for, with a resultant standardized impulse response. In this scheme, a test resistor on the chip is probed and measured, and the amplifier then accordingly trimmed to one of five possible discrete configurations to achieve "standard" impulse response. On-chip capacitance variations also affect the response. However, all explicit capacitors are formed from back biased junctions, which have a smaller quoted variation from nominal than do resistors.

Actually, it is possible to trim the amplifier to a different impulse response if desired by trimming to the "wrong" configuration. For example, if the process resistance is measured to be at nominal (in the center of its quoted possible range), the response can be made faster or slower by trimming the chip as if the process resistance was at the high or low end of its range, respectively. For a large number of chips, this is only practical if they all have about the same process resistance value (which is likely for any given wafer). Only the standard impulse response is guaranteed to be achievable since the process resistance is unpredictable.

However, limited experience has shown that there is a good chance that chip resistances come out close to nominal.

CIRCUIT DESCRIPTION

A complete schematic of the chip is shown in Figures 2, 3, and 4. Figure 2 shows the four channels as "black boxes". There are actually two each of two slightly different types of amplifier, PREAMPA and PREAMPB. However, the differences are insignificant and are only a result of physical layout considerations and component availability on the chip. All four channels share a common bias voltage, VB, which is developed on the chip with a diode string. VB is brought out to an external pad only for the purpose of bypassing. This is necessary to prevent channel to channel crosstalk and to limit random noise. Each channel has its own signal ground (VEE) so that crosstalk from common impedance coupling through a shared ground connection is avoided. An output driver ground (GND) is shared by all four channels. The chip has two supply voltage lines, VCC1 and VCC2. VCC1 is the supply voltage for the first and second stages, and is nominally +4.5V. However, this can be varied to "adjust" the impulse response if desired. VCC2 is the supply for the output driver transistors. It is kept separate from VCC1 to avoid crosstalk and so that it may be run at a lower voltage to reduce power consumption if desired. VCC2 can be run as low as +2.5V (for VCC1=+4.5V), or can be run at the same voltage as VCC1 for simplicity. VCC2 should not be set more than 2 volts lower than VCC1 to avoid forward biasing the base-collector junctions of the output transistors.

Figures 3 and 4 show the detailed amplifier schematics. The preamplifier is simply a large area input transistor (common emitter) with a cascode transistor, and an emitter follower to serve as a buffer for the feedback resistor and the next stage. Q6 and Q7 are used as pole shifting capacitors which can be left in or laser trimmed out to compensate for process variations in RC1. In like manner, RE2 -RE6 form an attenuator which can be changed by laser trim to compensate for variations in the feedback resistor.

The input preamplifier and a similar bandwidth limited preamplifier used for DC tracking both feed a differential second stage, which is simply a bandwidth limited voltage amplifier. Q14-Q17 are capacitors which form a pole with the collector resistors. Q18-Q21 are used as pole shifting capacitors to compensate for variations in the collector resistors. The transimpedance of the complete amplifier is set at its standard value by trimming the nichrome emitter resistors in the current mirror which biases the stage.

The differential output is driven by emitter followers which are biased on-chip to avoid having to use an external pull down resistor. A laser

trimmable back termination is in series with each output. The range of impedance for each output is approximately 40-70 ohms. Nominal trim specification is 50 ohms per side. The outputs of all channels should be capacitively coupled to the load. It is desirable to keep a constant impedance from the amplifier output to the load.

Figure 5 is a pinout of the chip bonded in the 28 pin surface mount prototype package provided by Tektronix. This package could be used in a final system design, or other packages can be considered. Fermilab E771 uses a small custom leadless 25 mil pitch package, which contains 2 chips (8 channels), to achieve high density. This type of packaging allows 128 channels to be mounted on a double sided PC board which measures 4 by 2 1/2 inches.

TEST RESULTS

SETUP

The circuit used to test the amplifier is shown for one channel in Figure 6. A 100:1 attenuator is used at the input to avoid very small signals on the input cable. A square wave edge is sent through a 10 pf, 1%, surface mount capacitor to the amplifier input. This essentially injects an impulse of charge and is an approximation of a real detector signal. All channels have outputs capacitively coupled and terminated in 50 ohms to ground.

IMPULSE RESPONSE

The impulse response of the QPA02 for a 4 fc input is shown in Figure 7 for different laser trim programs (and thus different impulse responses). Only the positive going output is shown for simplicity. The response is shown for input capacitances of 15 pf, 20 pf, and 25 pf. This is the worst expected variation for a silicon strip detector and fanout with nominal capacitance of 20 pf. All prototype chips which have been received and tested have close to nominal process resistance. In this case, for standard response, trim program #3 should be used. The responses for non-standard trim programs #1 and #5 are also shown in Figure 7.

For a range of nominal input capacitances different than 20 pf, it is possible to retain the standard impulse response by adjusting VCC1. For example, for Cin = 10 pf and Cin = 30 pf, the impulse response is faster and slower respectively, for VCC1 = +4.5V. However, if VCC1 = +3.77V for Cin = 10 pf and VCC1 = +5.15V for Cin = 30 pf, the standard response is obtained. This is shown in Figure 8 for a 4 fc input. Of course, for higher Cin, the S/N ratio will decrease.

GAIN AND DYNAMIC RANGE

The impulse gain for standard pulse response was measured at the differential output to be 17 mv/fc, with each output loaded with 50 ohms. The DC transresistance was measured to be about 500,000 V/A. Both of these values agree closely with the TSPICE predicted values.

The dynamic range is limited mainly by the amount of pull down current through the negative going output transistor and the impedance being driven by that output. The current through each output transistor is set at about 4 ma by an on-chip pulldown resistor. If each output drives 50 ohms (100 ohms transmission line), the theoretical limit for negative going output swing is 200 mv. The measured dynamic range is shown in Figure 9. In reality, linearity starts dropping off above 100 mv per side, which corresponds to 2 or 3 MIPs. A 5 MIP (20 fc) pulse has about a 10% gain error. If desired, external pull down resistors can be added to increase the dynamic range. Figure 10 shows the output pulse shape at the positive and negative going outputs for 10 MIP and 100 MIP inputs. The output for 100 MIP swings far enough so that the output transistor base-collector junction becomes forward biased when VCC2 = +2.5V. If VCC2 is raised to +3.0V, this effect disappears. According to Tektronix, a forward biased base-collector junction can cause latchup on the chip. However, this was not observed. For safety, all base-collector junctions should probably be kept reverse biased.

INPUT IMPEDANCE

TSPICE simulations have shown the input impedance below 30 MHz to be about 200 ohms, with a slight peaking at 20 MHz. Above 30 MHz, the input impedance drops rapidly. Experimentally, an input impedance of approximately 195 ohms was measured.

NOISE

The noise was measured by using a discriminator and varying the threshold to obtain (discriminator output frequency)/(amplifier input frequency) ratios of 0.883 and 0.117. The difference in these two thresholds is then the FWHM of the output noise, assuming the noise is Gaussian. This is then referred to the input by dividing by the charge gain. Figure 11 is a plot of measured noise vs. input capacitance (trimmed for standard impulse response). Also plotted is the noise calculated from TSPICE runs. The measured noise between Cin = 10 pf and Cin = 30 pf falls on a line described by:

Input Noise (rms) = 930 e- + 32 e-/pf.

The noise was also measured for the amplifiers trimmed to non-standard response:

Trim Program #1: Noise = 940 e- + 30 e-/pf

Trim Program #5: Noise = 930 e- + 37 e-/pf

POWER DISSISIPATION

The current draw for each supply was measured for the standard chip:

VCC1 (+4.5V): I = 20.7 ma, Pd = 93 mw
VCC2 (+2.5V): I = 37.7 ma, Pd = 94 mw

The total power dissipation for the chip is 187 mw, or 47 mw/channel. Of course, the dissipation will be higher if VCC2 is increased. The VCC2 current stays relatively constant as VCC2 is increased.

CROSSTALK

The typical crosstalk between any two channels is less than 1%. However, to achieve this requires attention to good layout and high frequency bypassing.

LAYOUT CONSIDERATIONS

Since the QPA02 is a very high gain fast amplifier, the PC board layout, shielding, and bypassing are critical to proper operation of the chip. Chip tests on an actual detector plane for Fermilab E771 have brought out several relevant points.

First of all, it is important that all inputs be fully shielded from the chip outputs. This entails enclosing the detector and as much of the input leads as possible in a Faraday box which is well grounded to the chip ground. The input feedthrus should cause minimum disruption in shield continuity to maintain shield effectiveness. For example, Fermilab E771 uses amplifiers on a PC board which plugs into an edge connector mounted at the inside boundary of the shield. This requires a long narrow slot in the shield, which destroys its effectiveness. Thus it was necessary to place ground plane on each side of the board, which contacts the shield through RF gaskets (input traces were then run on inner layers of the PC board). The ground planes on opposite sides of the board are connected together with a number of via holes spaced evenly across the board. Thus the shield currents actually flow across the slot through the PC board.

This is very effective in preserving shield integrity in this application.

Any PC board layout for QPA02 should have at least one layer fully devoted to ground plane. All signal grounds (VEE), bypass capacitors, and output driver grounds (GND) should be connected as directly as possible to this low impedance ground. Separating VEE and GND is not recommended.

QPA02 has duplicate supply voltage pads, located on either side of the chip. It is sufficient to connect supplies and GND to only one side of the chip.

Bypass capacitors to the ground plane are essential at three points: VCC1, VCC2, and VB. The VCC2 bypass is found to be most layout critical. The emitter followers will tend to oscillate unless VCC2 is very well bypassed, especially if the outputs are not terminated properly. E771 uses small surface mount capacitors mounted inside the chip carrier package directly next to the wire bonds in order to minimize the inductance in series with the bypass capacitor. If this is not done, the circuit is somewhat sensitive to discontinuities in load impedance caused by connectors, etc. The chip mounted in the Tektronix leaded package cannot be bypassed this closely, but if done with care, the chip is stable as long as the outputs are properly terminated.

SUMMARY

QPA02 has been tested and demonstrated to be an effective silicon strip amplifier. Other applications may exist which can use this amplifier or a modified version of this amplifier. For example, another design is now in progress for a wire chamber amplifier, QPA03, to be reported later. Only a relatively small effort was required to modifiy the design and layout for this application.

Note: Unless otherwise noted, all specifications are at T=25 C, VCC1=+4.5V, VCC2=+2.5V, VEE=GND, R(load)=100 ohms, C(in)=20pf.

Amplifier type:	Common emitter transconductance
Channels/chip:	Four
Inputs:	One ground and one input per channel, accepts negative and positive current signals.
Input voltage:	Quiescent level = + 0.70 volts, +/- 0.05 volts
Input Impedence:	Nominally 200 ohms.
Outputs:	Two per channel, differential.
Output voltage:	Quiescent level = +1.5 volts, +/- 0.25 volts.
Output DC Offset:	+/- 200 mv max.
Output Impedance:	Laser trimable, 45 to 70Ω/side, (90 to 140 diff)
Output Voltage Swing:	+/- 100 mv differentially for linear operation, +/- 200 mv max. (50Ω/side).
Output transistor current:	4ma (set internally). Can be increased with external pulldown resistor to increase dynamic range.
Output recovery:	Less than 35ns to 10 mv for 250,000 e input pulse.
Cross talk:	Less than 1% between any 2 channels.
DC Gain:	250 mv/ua +/-10 % per output, 500mv/ua diff.
Impulse Gain:	17 mv/fc (output terminated)
Power:	VCC1: 20ma at +4.5 volts nominal. VCC2: 32ma at +2.5 volts nominal. Total power nominally 42 mw per channel.
Risetime (10-90%):	6 nsec +/-2ns for C(in)=20 pf and impulse input.
Falltime (10-90%):	12nsec typical for C(in)=20 pf.
Shaping:	14ns +/- 2ns FWHM, impulse input. Trim program can be varied to obtain other than nominal shaping.
Input Noise:	Max eRMS for DC-100Mhz ,1300 @10pf, 1600 @20pf, 1900 @ 30 pf
Impulse Gain Tempco:	Nominally -0.12%/°C (25-65°C)
DC Output Tempco:	Nominally +2.5 mv/°C (25-65 °C).

Figure 1

FERMILAB SILICON STRIP AMPLIFIER

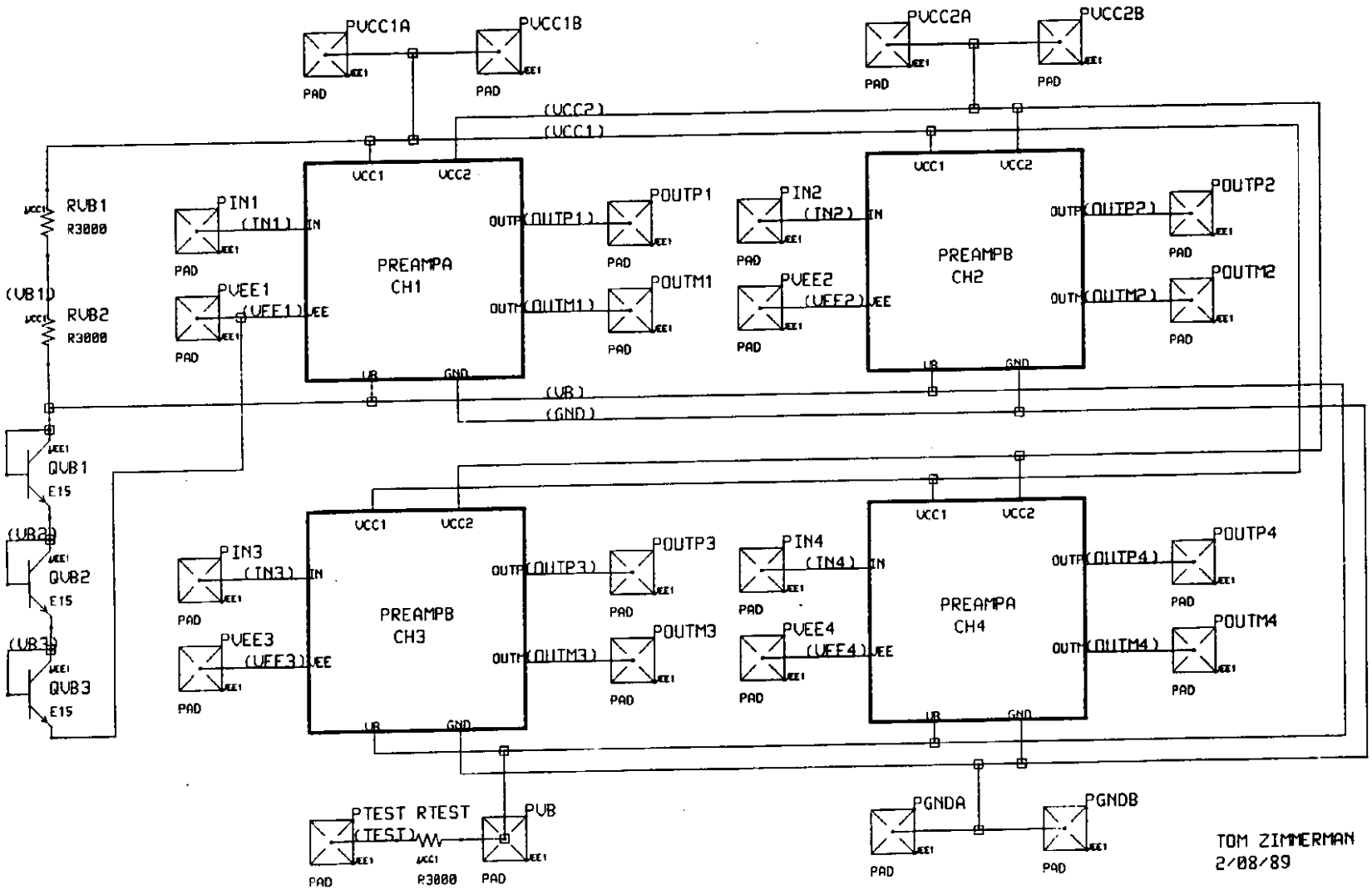

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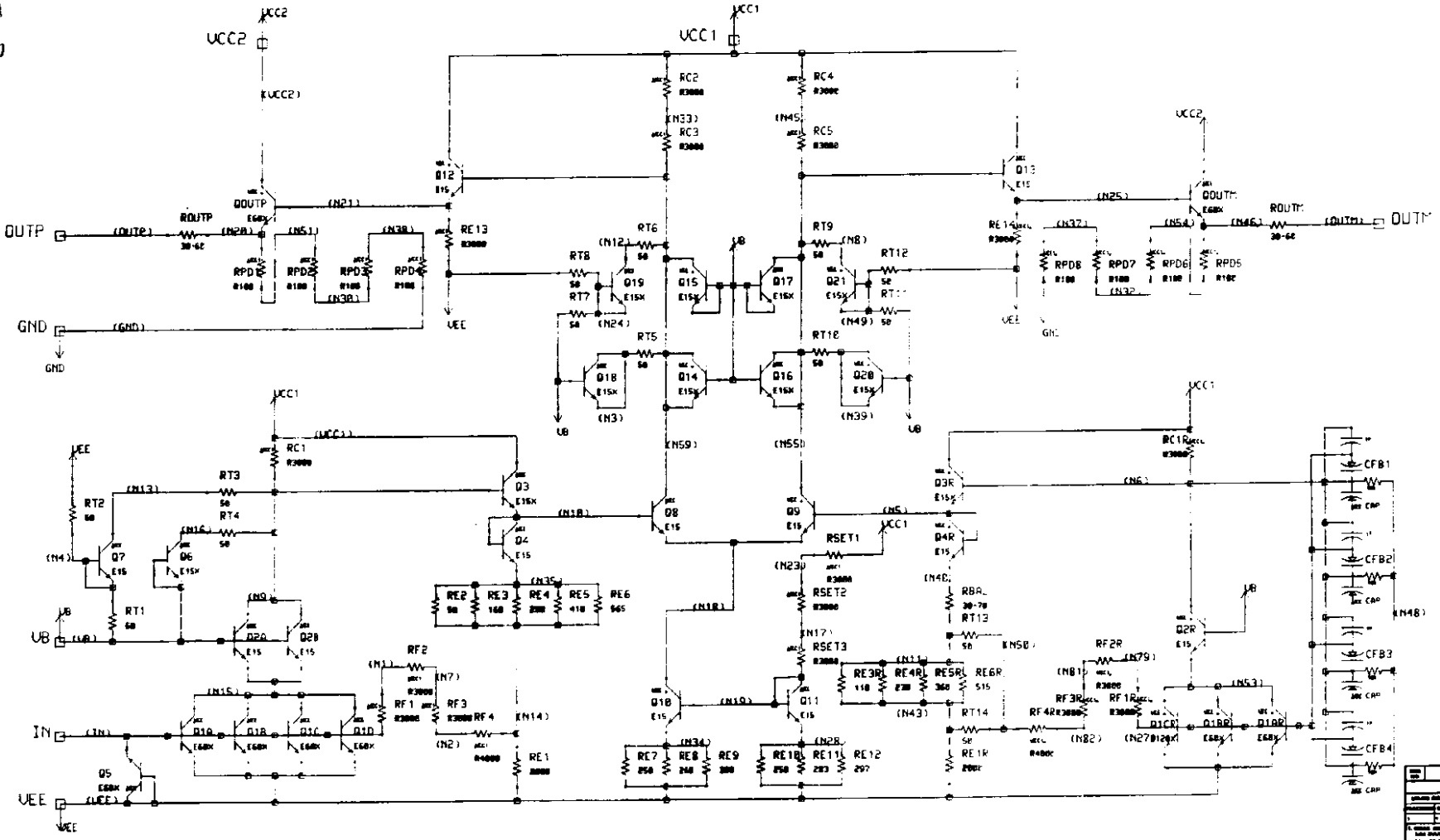
FIGURE 2

FERMILAB SILICON STRIP AMPLIFIER

PREAMPA



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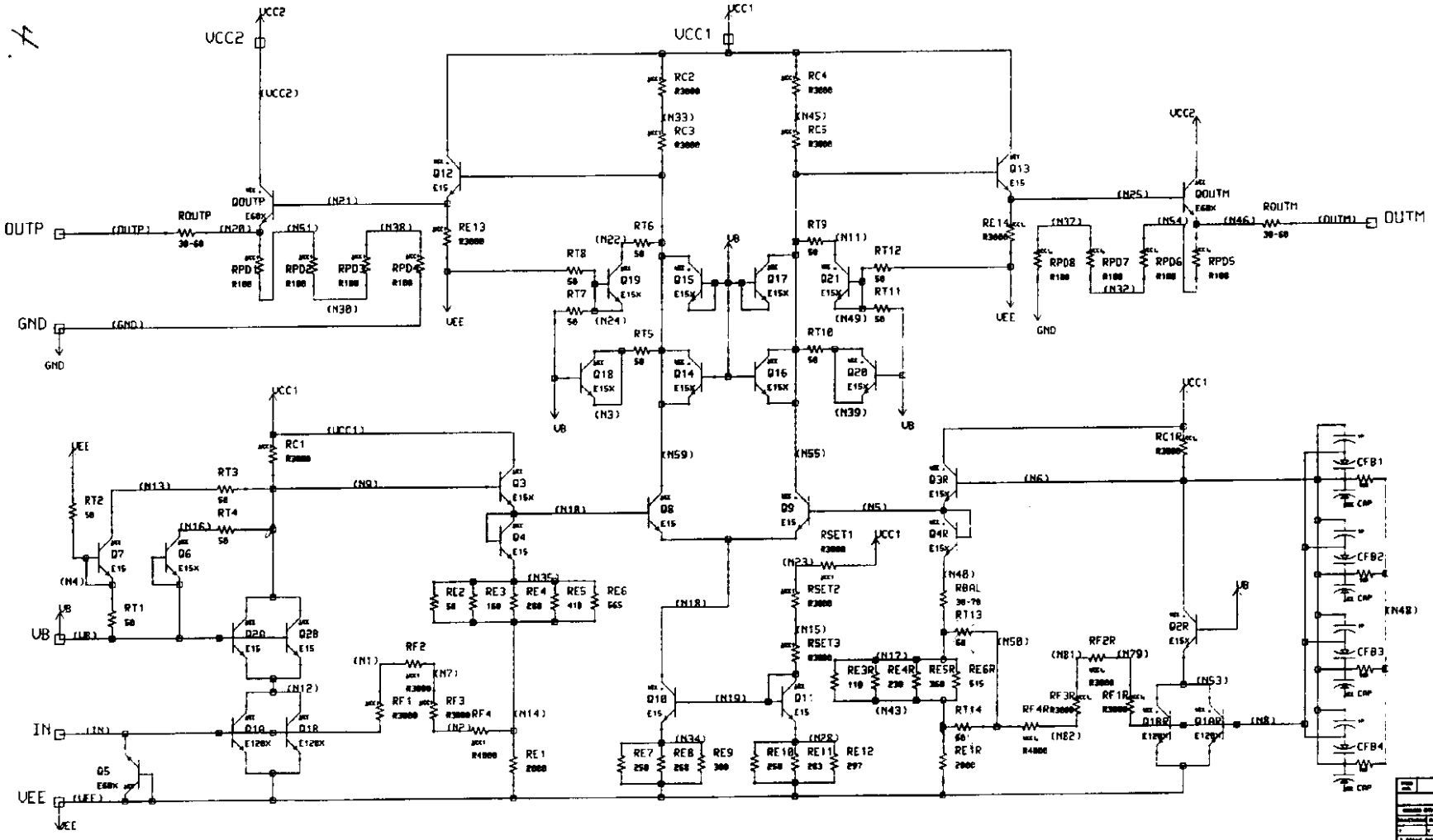
FERMILAB SILICON STRIP AMPLIFIER
PREAMPB



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QPA 02

BONDING DIAGRAM

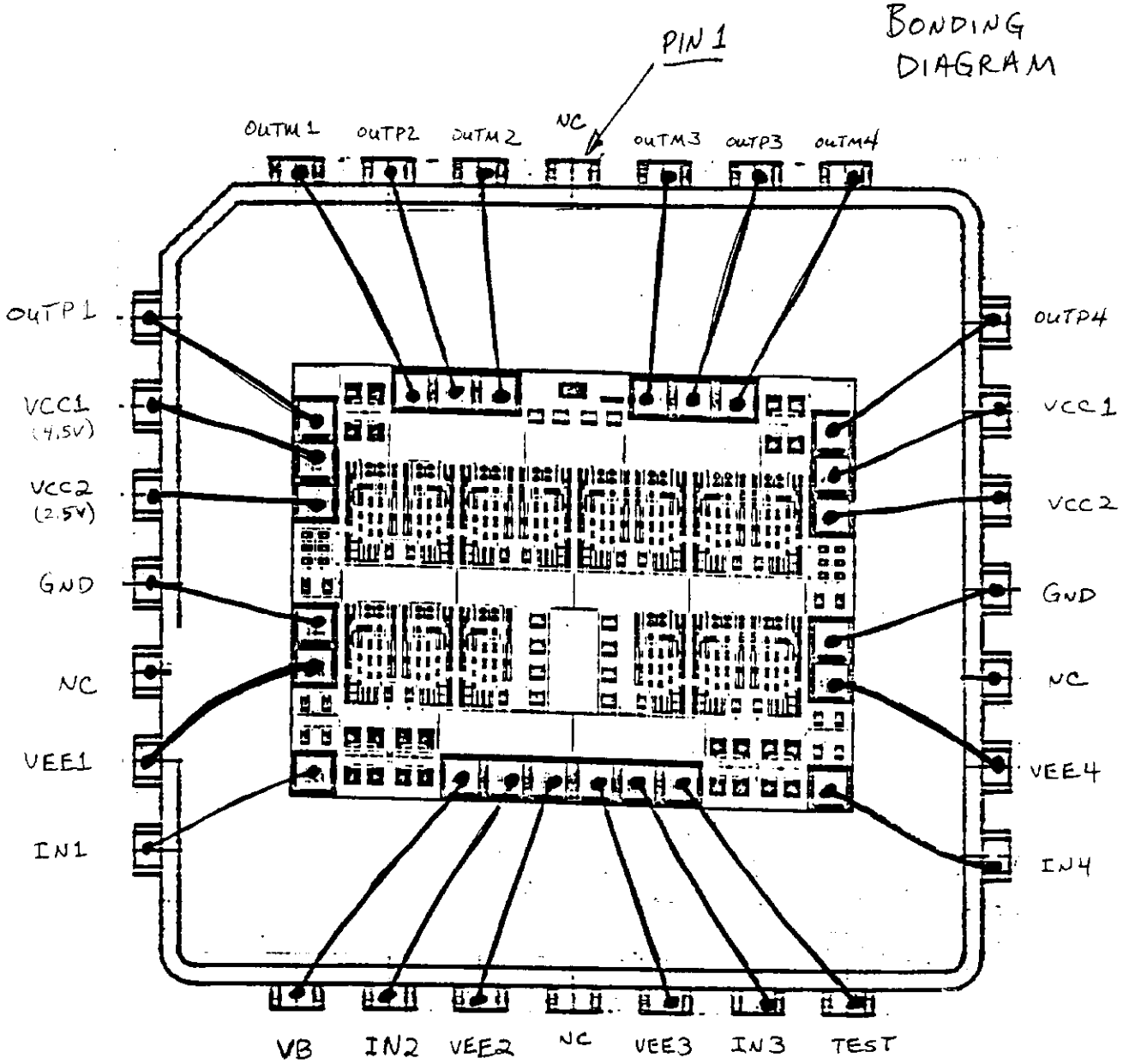


FIGURE 5.

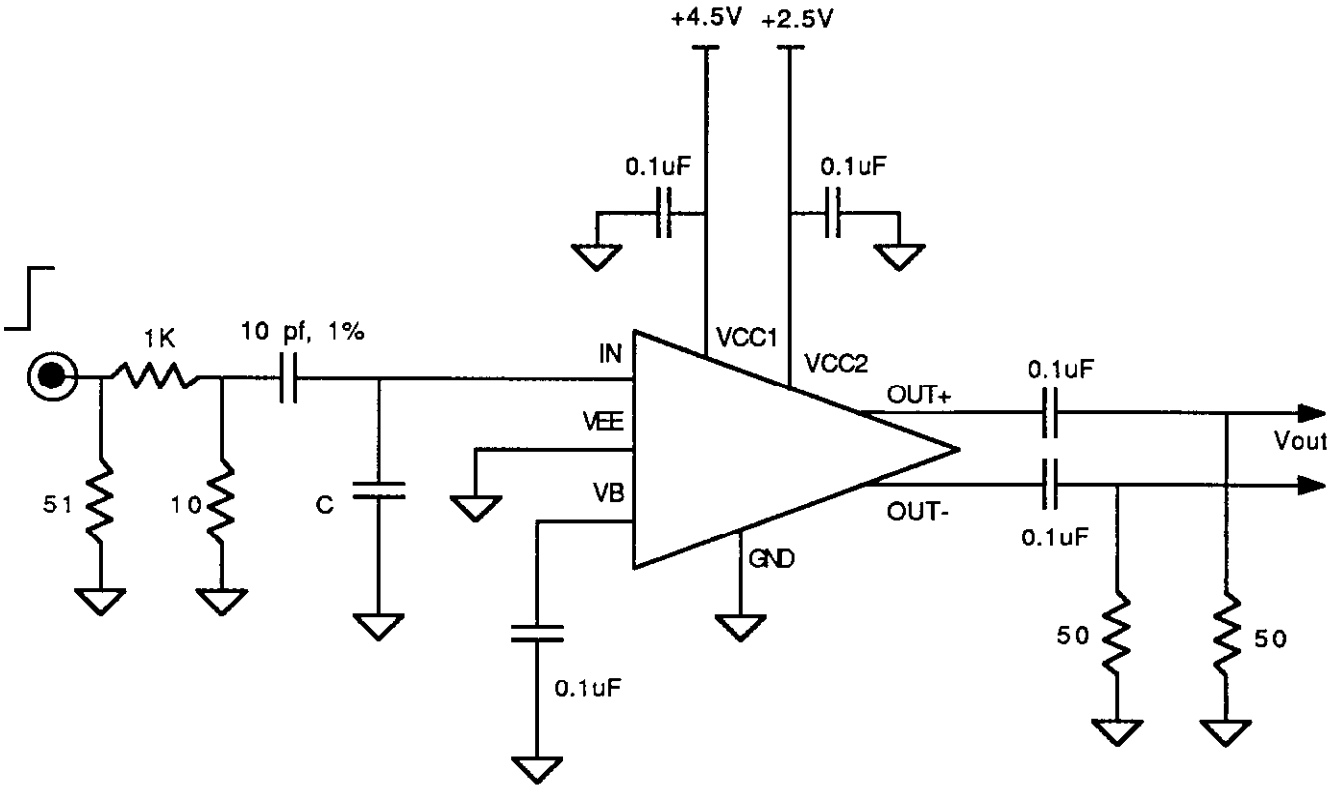
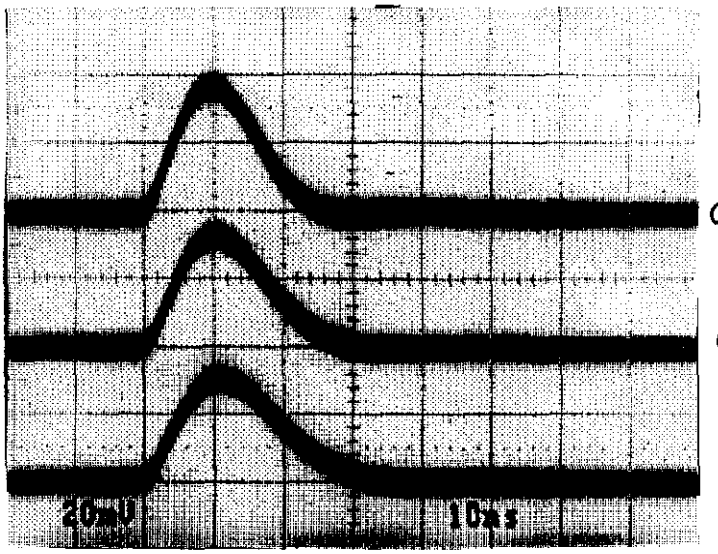
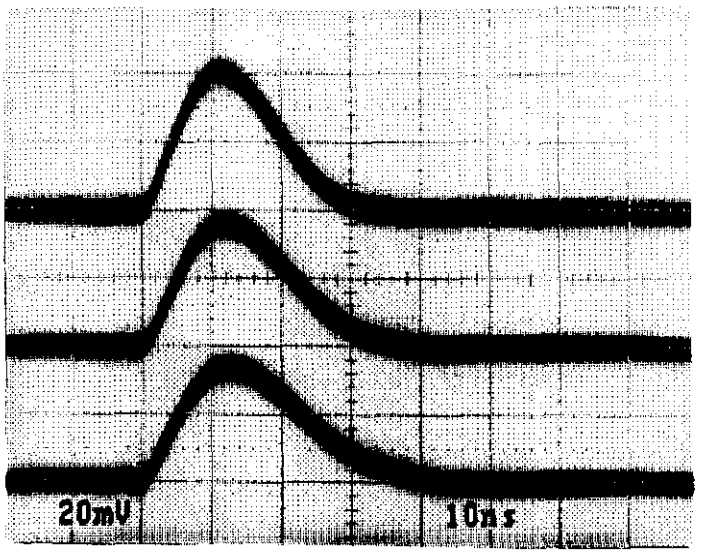

+4.5V
+2.5V
0.1uF
0.1uF
1K
10 pf, 1%
IN
VCC1
VCC2
OUT+
0.1uF
VEE
Vout
51
10
C
VB
OUT-
0.1uF
GND
50
50
0.1uF

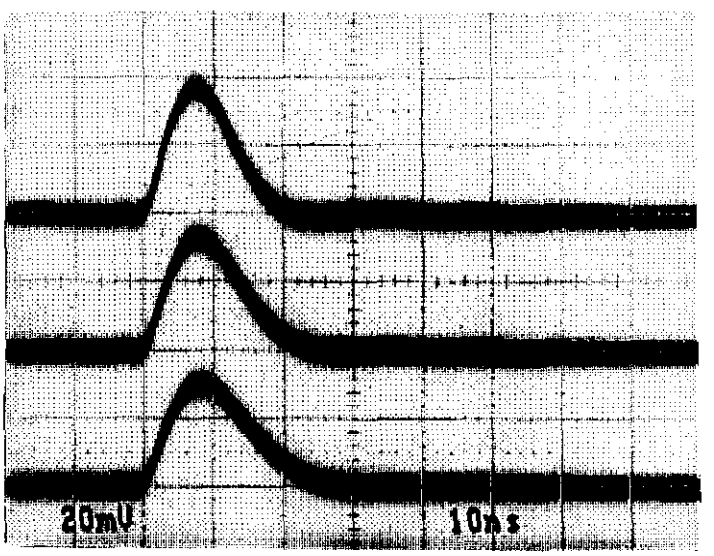
Figure 6



Trim Program #3

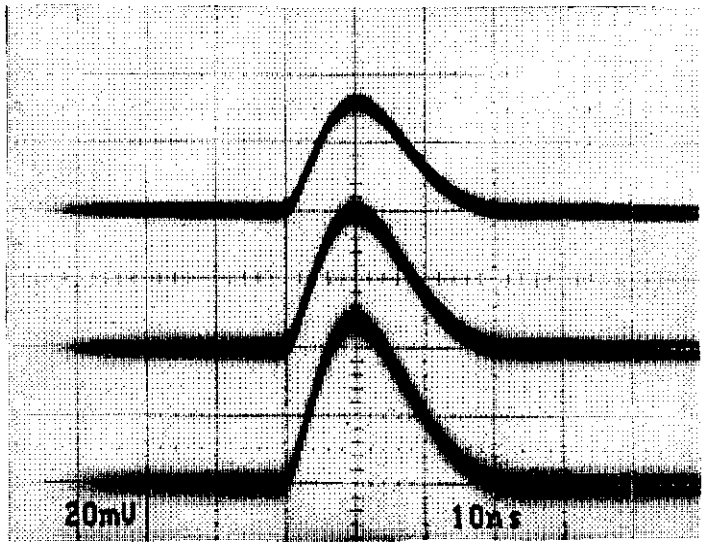


Trim Program #1



Trim Program #5

Figure 7 - Impulse Response



Cin = 10 pf, VCC1 = +3.77V

Cin = 20 pf, VCC1 = +4.5V

Cin = 30 pf, VCC1 = +5.15V

Figure 8

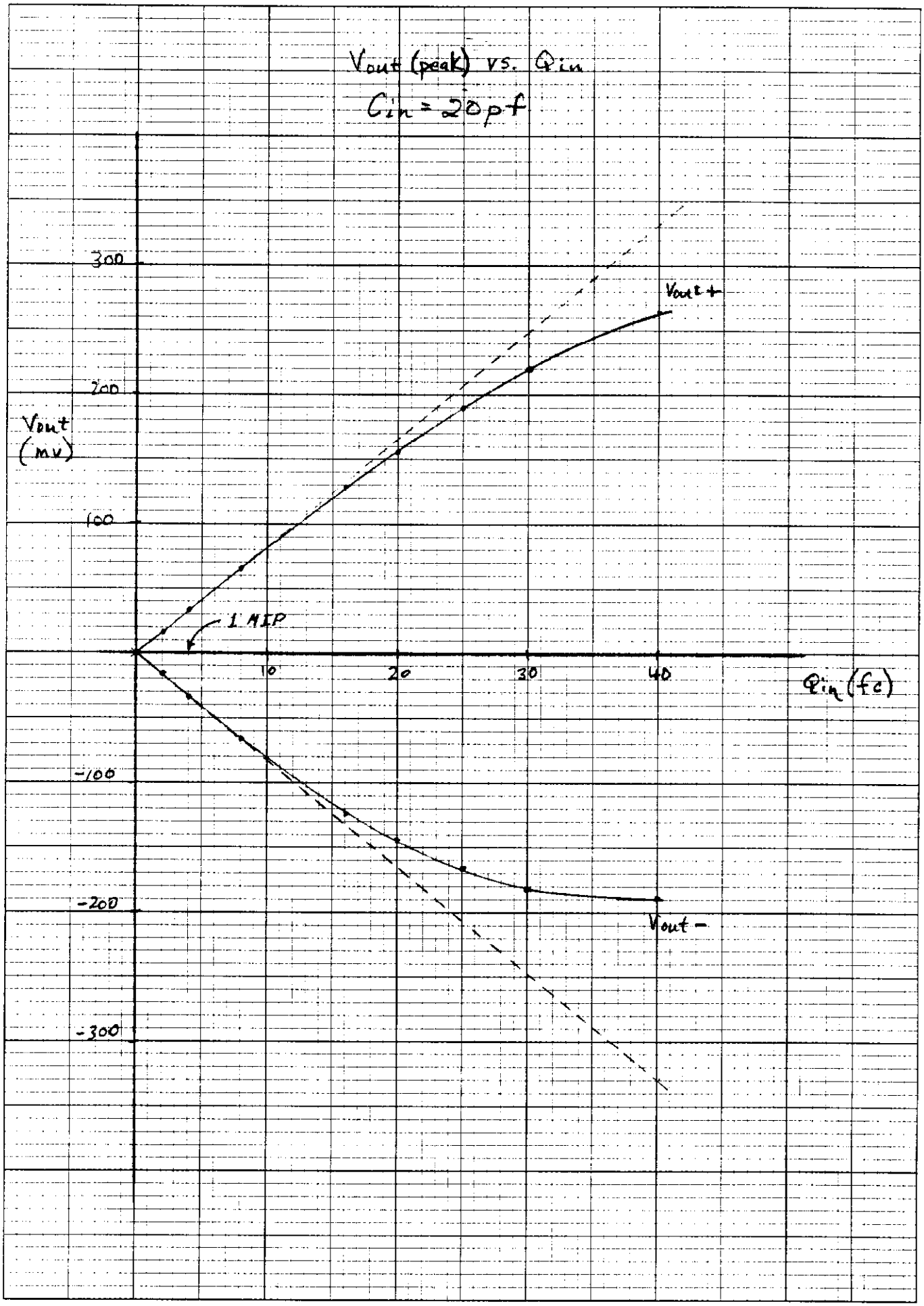
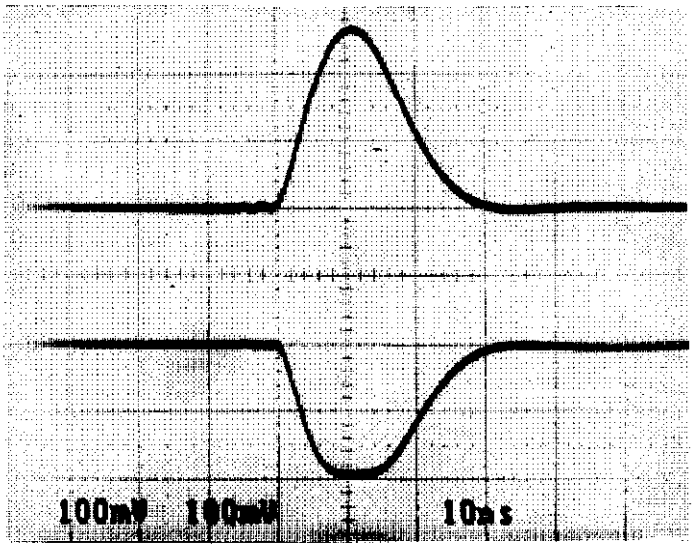
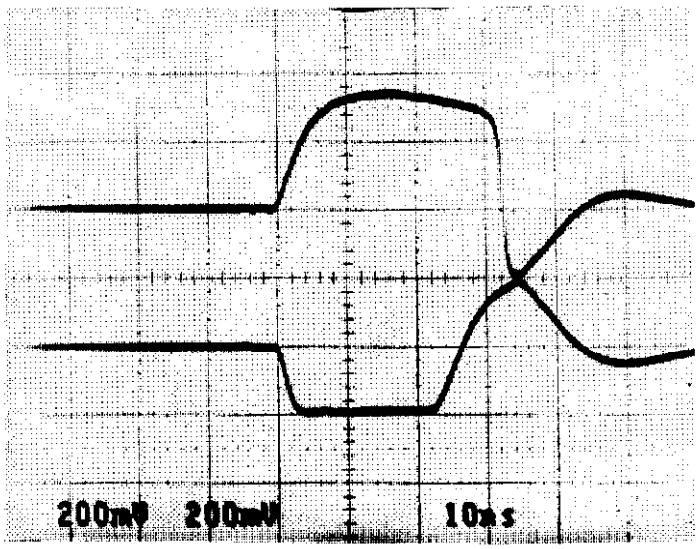


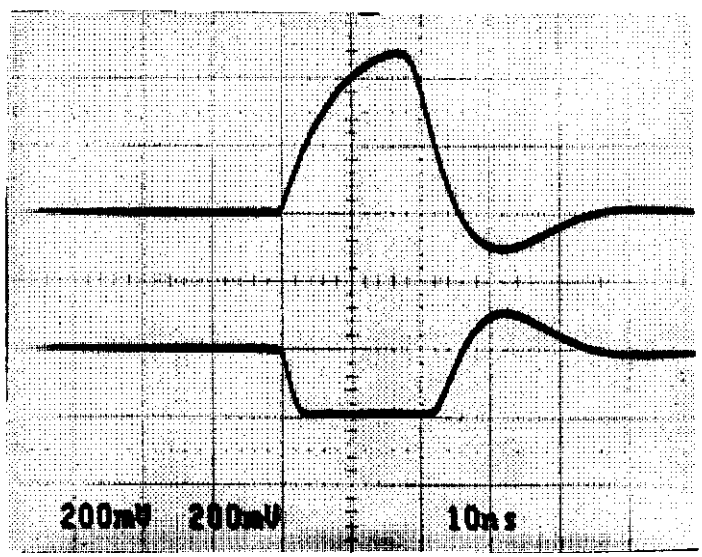
FIGURE 9



Input = 10 MIP



Input = 100 MIP, VCC2 = +2.5V



Input = 100 MIP, VCC2 = +3.0V

Figure 10 - Large Input Response

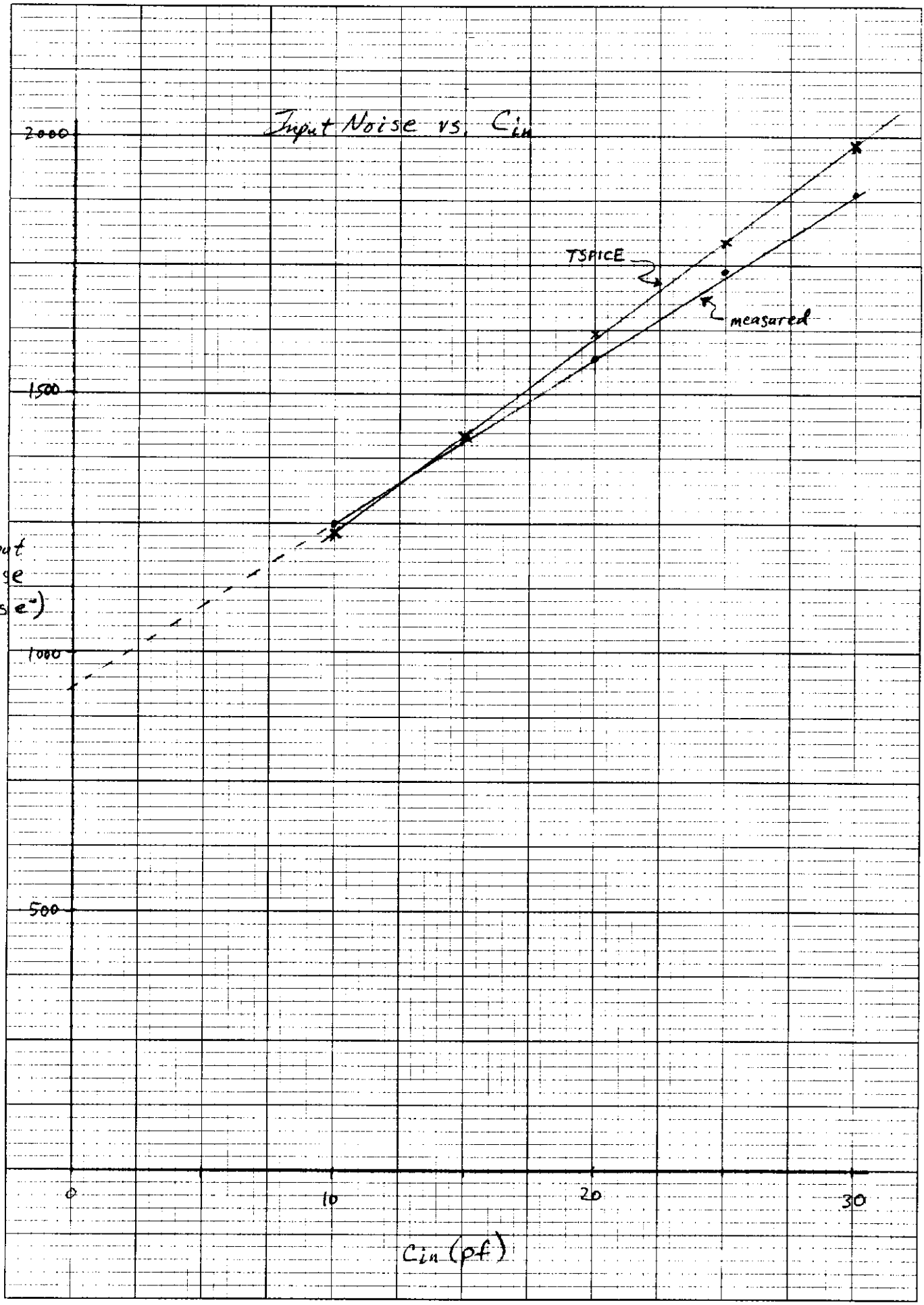


FIGURE 11.