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RADIATION EFFECTS ON JFETS, MOSFETS, AND BIPOLAR TRANSISTORS, AS RELATED TO SSC CIRCUIT DESIGN*

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Abstract

Some results of radiation effects on selected junction field-effect transistors, MOS field-effect transistors, and bipolar junction transistors are presented. The evaluations include dc parameters, as well as capacitive variations and noise evaluations. The tests are made at the low current and voltage levels (in particular, at currents ≤ 1 mA) that are essential for the low-power regimes required by SSC circuitry. Detailed noise data are presented both before and after 5-Mrad (gamma) total-dose exposure. SPICE radiation models for three high-frequency bipolar processes are compared for a typical charge-sensitive preamplifier.

Introduction

The operating environment anticipated for the Superconducting Super Collider (SSC) is a very harsh operating regime. The proposed event period of 16 ns demands very high frequency performance from electronic circuits, yet the need for thousands of circuits absolutely requires a low power operating budget. Additionally, an absolute limitation to circuit performance is the radiation due primarily to gamma and neutron bombardments that can exceed a total dose of 1 Mrad (gamma) and 10^{13} neutrons/cm^2 in a typical year of operation, dependent upon the distance from the beam [1]. This paper reports research conducted at the Oak Ridge National Laboratory (ORNL)† and The University of Tennessee, Knoxville, which was primarily concerned with gamma radiation total-dose effects on semiconductor devices and circuits. The source was a Gammacell 200 ^{60}Co irradiator. The circuits developed were primarily preamplifiers that could be used in large-volume calorimeters having detector capacitances in the range of 20-500 pF. The radiation properties of three high-frequency bipolar processes (from AT&T, Harris Semiconductor, and VTC, Inc.) were investigated, as well as several commercially available junction field-effect transistors (JFETs). Although it was understood that the use of MOSFETs should require a special radiation-hardened process, we nevertheless decided to investigate the properties of a MOSIS array to see just how deleterious radiation effects would be for a typically processed CMOS circuit. Although the restricted length of this paper prevents reporting all the data, the most essential radiation produced changes are stated.

Gamma Radiation Effects on JFETs

The JFET generally suffers the least damage in a radiation environment when compared with bipolar and MOS transistors. The reason is that a JFET is a majority carrier device and thus does not suffer from the minority carrier recombination problems that degrade a bipolar transistor. Although the MOS transistor is also a majority carrier device, the MOS transistor (unlike the JFET) is controlled by the electric field due to both the insulating gate oxide and the oxide-semiconductor interface states, and thus is quite sensitive to excess charge accumulation at the oxide and interface produced by ionizing radiation. The most significant radiation produced degradation in a JFET is the increase of reverse gate leakage current (I_G), which typically results in an increase from a few picoamps to a few nanoamps after several megarads of gamma dose.

When a JFET is used as the front-end device in a charge-sensitive (CS) preamplifier, the parameters of most interest are series noise, transconductance (g_m), capacitance, and output resistance [usually expressed as the ratio of the Early voltage (V_A) to the dc drain current (I_D)]. Generally, five samples of each device were characterized both before and after a 5-Mrad ^{60}Co irradiation. The devices were irradiated in a passive mode (all leads shorted together), and postirradiation testing was accomplished within typically 2-3 days after irradiation. All devices were kept at ~1 °C during storage to minimize annealing. The n-channel JFET units evaluated were the NJ3600, NJ1800, NJ903, 2N6451 and 2N4858 from InterFet, Inc.; the 2N5432 and IMF5912 from Intersil; the 2SK152 from Sony; and the 2N4416A from Siliconix. Since space is limited, only data for the largest area (NJ3600) and smallest area (2N4416A) devices are presented in this paper. All devices were characterized at

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three drain currents of 1 mA, 100 μA and 10 μA, and with a drain-source voltage of 2.5 V, which are operating regimes anticipated for the low power requirements of the SSC.

The equivalent noise voltage (ENV, or 'series' noise) of the NJ3600 and 2N4416A are shown in Figs. 1 and 2 for I_D of 1 mA and 100 μA, both before and after 5-Mrad gamma radiation. The noise is expressed as an equivalent noise resistance. The lower straight line on the graphs indicates the theoretical midband noise resistance anticipated [$R_n = 4kT\,(0.66/g_m)$]. The "error bars" indicate the range of measurements (min, max) for the 5 units of each device tested. As is apparent in Figs. 1 and 2, the region of midband noise is not achieved until >100 kHz after radiation. The low-frequency 'noise corner', f_c, at which the series noise resistance is twice that of the midband noise resistance is shifted from ~15 Hz (before radiation) to ~70 kHz after radiation in the NJ3600, versus ~2 kHz (prerad) to ~500 kHz (postrad) for the 2N4416A, when I_D = 1 mA. The multiple peaks in the postrad data are characteristic of recombination-generation noise due to trapping centers introduced by possible dislocations in the crystal lattice structure.

The measured input and output capacitance (C_{iss} and C_{rss}) for the JFETs generally indicated very slight changes in the postrad data relative to the initial values. Figure 3 illustrates data comparisons for the NJ3600, while Fig. 4 shows a slight (~0.2 pF) increase of capacitance for the 2N4416A device after radiation. The initial decrease of the C_{rss} values for $V_{reverse}$ < 1 V for the NJ3600 transistor after radiation is puzzling.

Several other parameters of the tested JFETs indicated very little change with radiation, with pinch-off voltages changing <1%, I_{DSS} values typically unchanged, and g_m values indicating perhaps a slight (<1.8%) decrease after radiation. The Early voltage values, however, increased from +18% for the NJ3600 to +160% for the 2N4416A devices. As anticipated, the gate leakage currents increased because of radiation from $<10^{-13}$A to 0.4 nA for the 2N4416A, and for the largest area device (NJ3600) the change was from 0.3 to 6 nA after 5 Mrads.

Gamma Radiation Effects on Bipolar Transistors

The most significant effect of ^{60}Co gamma radiation on the high-frequency bipolar transistors tested was a decrease in the dc current gain, Beta (ß) or h_{FE}. The Hewlett Packard Semiconductor Parameter Analyzer, Model 4145B, was used extensively for all dc measurements. Since radiation causes a decrease in minority carrier lifetime as well as a decrease in effective doping, the most radiation-resistant bipolar transistors will be those that have a relatively heavy base doping as well as a very narrow base width. Both of these criteria are present in high-frequency transistors having large gain-bandwidth products (f_T). The processes evaluated were those of the leading bipolar analog VHF semi-custom integrated circuit silicon foundries, namely AT&T, Harris Semiconductor, and VTC, Inc. The AT&T ALA200 array is typically a 4.5 GHz npn and 3.8 GHz pnp f_T family. The Harris analog FASTRACK VHF process utilizes 1.2 GHz npns and 1 GHz pnps, while the VTC VJ900 process provides a typical maximum f_T of 6 GHz (npn) and 1.5 GHz (pnp). All three manufacturers provide complete SPICE models for their transistors.

Figure 5 compares the prerad and postrad current gains (Beta) for the smallest area npn devices (an emitter size of 1 x 1, approximately 10 μm x 10 μm), while Fig. 6 compares ß for the small area (1 x 1) pnps, although the VTC unit tested was available in only a 1 x 9 area. It is apparent that the lower f_T pnp devices suffer the most degradation due to the ionizing gamma radiation. There were only slight changes (<5%) in the Cbc and Cbe depletion layer capacitances produced by the irradiations. The Early voltages for npn devices typically decreased because of irradiation, from 3% to 10%, while V_A increased by 15% for the Harris pnps, but decreased by 5% for the AT&T pnps and by 25% for the VTC pnps. The noise comparisons are shown in Table 2, comparing the series noise (i.e., the equivalent noise voltage or the equivalent noise resistance for the three processes, both before and after 5 megarad radiation. The low-frequency 'noise corner', f_c, for both a minimum size (1x1 emitter, or 1x device) and a large size (16x device) device are compared for both npn and pnp devices. Measurements of the equivalent noise currents (ENI) for the devices have not yet been made.

Using the HP4145B parameter analyzer, we were able to obtain an accurate SPICE model for each bipolar process, both before and after radiation. A comparison was made of each process to simulate a basic low-power, 20 mW, folded-cascode CS preamp [2] for use with a 2 cm x 2 cm silicon calorimeter detector (Cdet ~ 112 pF). The results for the rise-time, power dissipation, and anticipated equivalent noise charge (ENCe) for each preamplifier are compared in Table 1, both before and after radiation.

Table 1. SPICE simulation comparisons for a CS folded-cascode bipolar transistor preamplifier with a calorimeter detector capacitance of 112 pF. Shaping time-constant (CR-RC) of 50 ns.

	Process	Rise-Time (ns)	Pdiss (mW)	ENCe (rms electrons)
Preradiation				
	AT&T	4.9	19.1	4098
	Harris	5.5	20.0	5001
	VTC	4.9	19.3	4026
Postradiation (after 5 Mrad, ^{60}Co)				
	AT&T	7.0	18.3	4553
	Harris	8.0	17.7	7821
	VTC	7.0	18.5	5075

Table 2. Series Noise Comparisons for Bipolar Processes.

		Noise Corner Frequency (f_c - kHz)				Rn (midband) - ohms	
		(1x)		(16x)			
	Process	Pre-Rad	Post-Rad	Pre-Rad	Post-Rad	(1x)	(16x)
NPNs	AT&T	2.4	2.4	6.0	10.0	76	55
	Harris	0.6	2.4	2.0	2.8	550	62
	VTC	0.35	0.55	2.5	3.2	455	52
PNPs	AT&T	5.0	6.0	5.0	5.5	51	16
	Harris	6.0	10.0	1.7	2.4	148	26
	VTC	—	—	(8x) 1.0	(8x) 1.5	(8x) 78	(8x) 78

Gamma Radiation Effects on MOSFETS

Although a special radiation-hard CMOS process will be required for SSC circuits, we wanted to see how a typical MOSIS CMOS process would survive a gamma dose. Special NMOS and PMOS dual arrays having width/length ratios of 100 μm/10 μm and 1000 μm/10 μm were designed using the MAGIC layout program. The chips were fabricated under the standard 2 μm p-well Orbit Semiconductor process, using the MOSIS fabrication program. All transistors were fabricated in a 'quad' configuration, with diagonal transistors connected to obtain an overall well-matched dual transistor configuration, which is indicative of the construction required for low offset-voltage differential front-end devices. The dual transistors were biased in a normal conductive state (V_{DS} = 2.5 V, I_D = 1 mA, 100 μA and 10 μA) during the irradiation. The threshold voltage V_T was monitored, and devices were removed when the observed threshold voltage shift for the PMOS units had shifted to approximately 2 x V_T(pre-rad), which occurred at a total dose of 1.3 Mrad. It was found that the PMOS devices had an average shift in V_T from -0.7 to -1.5 V, while NMOS devices had V_T shifts from 0.9 to 0.6 V, although undoubtedly the worst-case negative shift from the initial 0.9-V value was much larger because the fixed oxide charge (N_{ot}) before the interface-trapped charge (N_{it}) effect produced a positive V_T trend. An example of the large increase (~5x) in the low-frequency noise due to radiation is shown in Fig. 7 for an NMOS device with W/L=100 μm/10 μm. Of most significance was the large increase in the offset voltage V_{OS} of the dual units, with pre-rad values of ≤ 1 mV for both n-and p-channel units observed for 1000 μm/10 μm devices, while in a post-rad measurement V_{OS} values of ≥ 100 mV were obtained. Further, the shift in g_m (at 1 mA) was significantly higher than that observed in JFETs, approximately -12% for PMOS and -19% for NMOS units after radiation. The Early voltages, similar to those for JFETs, increased after radiation from ~20 V to ~60 V for PMOS units, and from ~30 V to ~150 V for NMOS units.

Conclusions

Radiation using a ^{60}Co gamma source has shown a significant increase in the low-frequency noise for both JFETs and MOSFETs. JFETs are decidedly superior to MOSFETs where constancy of gm and threshold voltage are concerned. Although the Beta degradation is severe, particularly for pnp transistors, the high-frequency bipolar transistor offers very low series noise when compared with an FET and shows promise as a useful technology for the small shaping time-constants that will be required for the SSC.

Acknowledgements

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References

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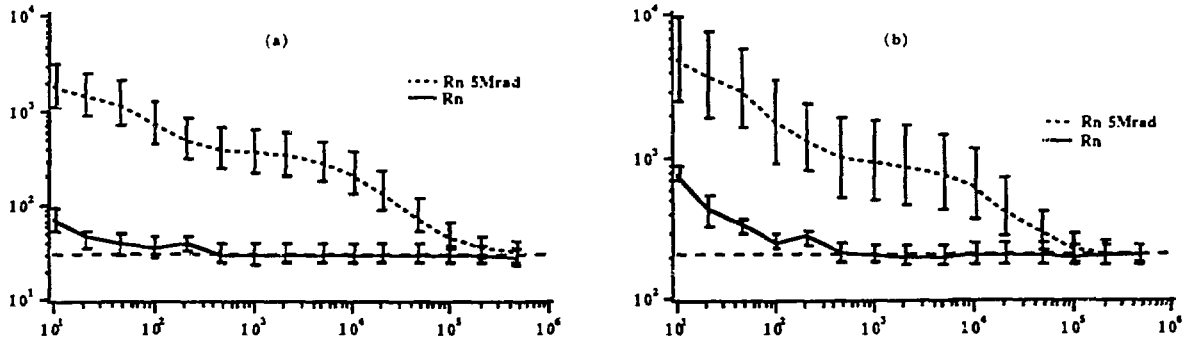

Fig. 1. Series noise resistance versus frequency for the InterFet NJ3600L at (a) I_D = 1 mA and (b) I_D = 100 μA [V_{DS} = 2.5 V].

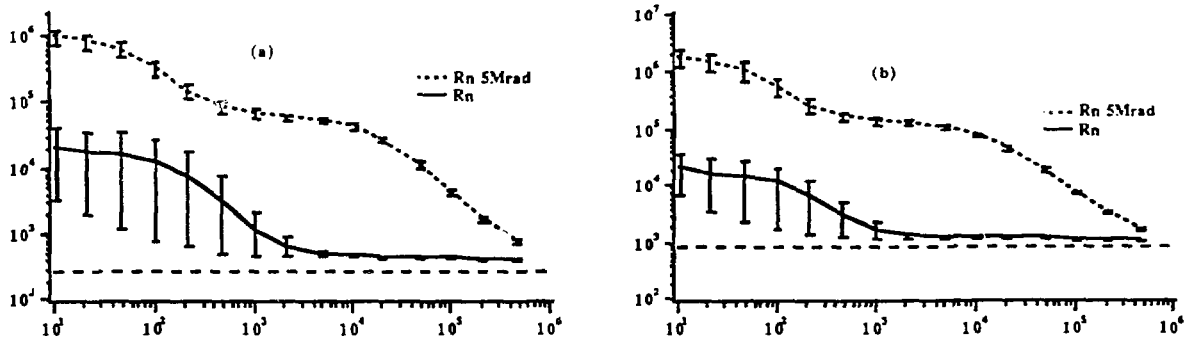

Fig. 2. Series noise resistance versus frequency for the Siliconix 2N4416A JFET at (a) I_D = 1 mA and (b) I_D = 100 μA [V_{DS} = 2.5 V]

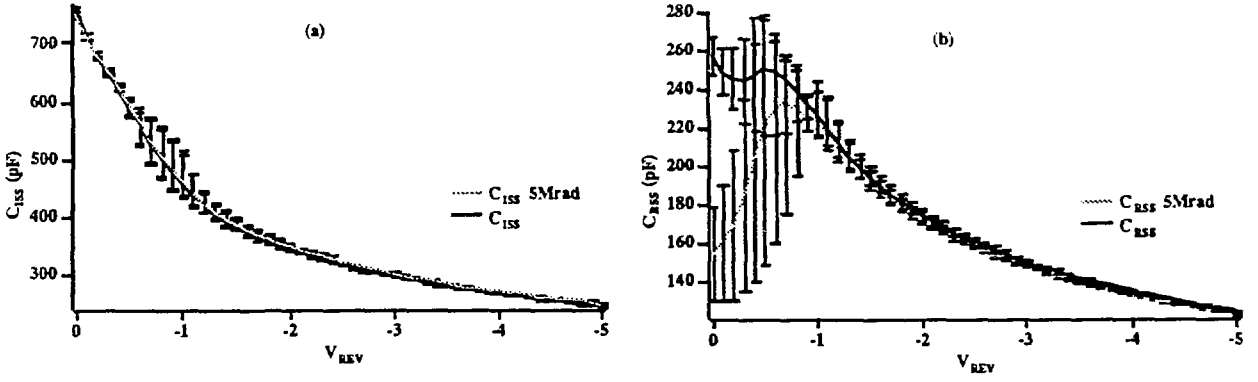

Fig. 3. Capacitance variations for the NJ3600L JFET, both before and after a 5-Mrad dose. (a) Input capacitance C_{iss} and (b) gate-to-drain capacitance C_{rss}.

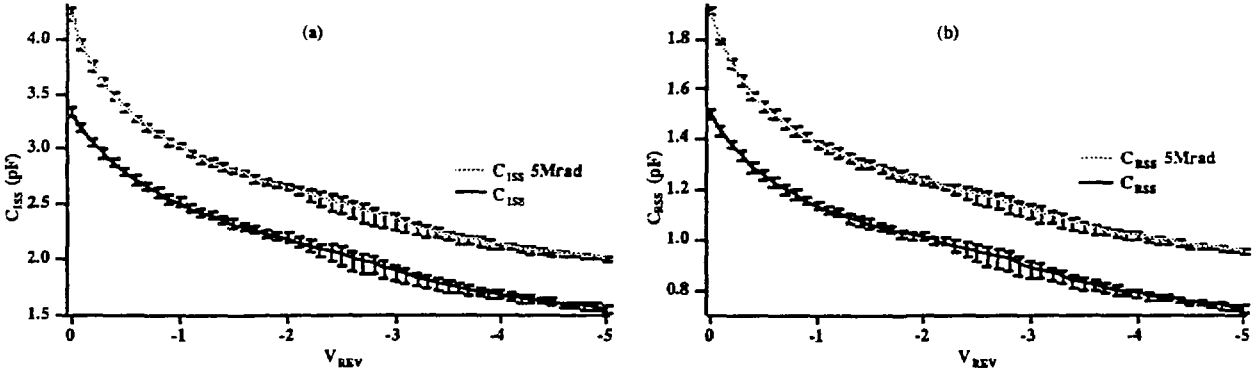

Fig. 4. Capacitance variations for the 2N4416A JFET.

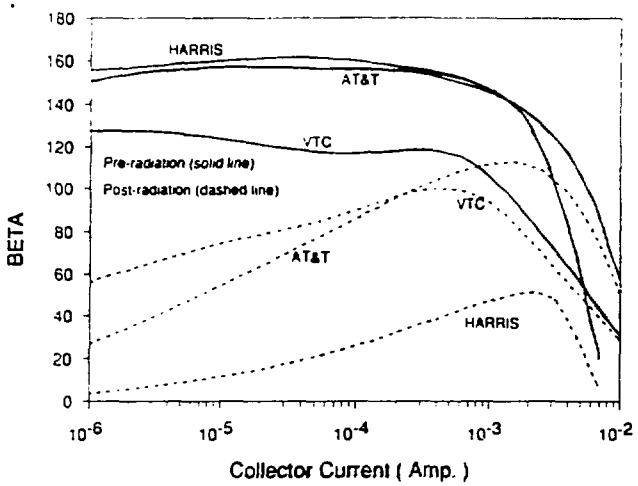

Fig. 5. Beta vs. I_C for npn high-frequency transistors. [V_{CE} = 2.5 V]

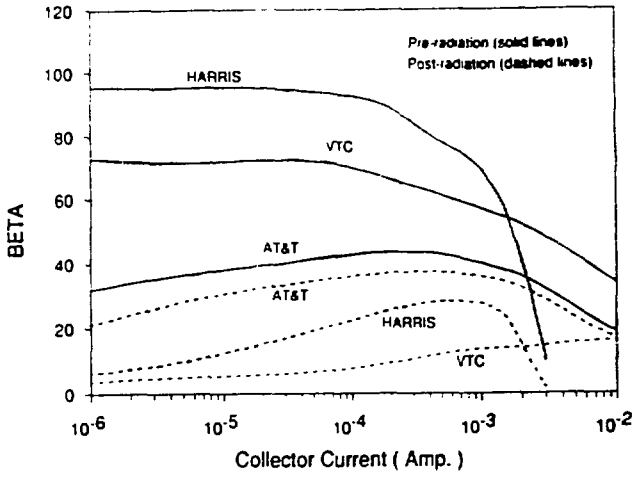

Fig. 6. Beta vs. I_C for pnp high-frequency transistors. [V_{CE} = -2.5 V]

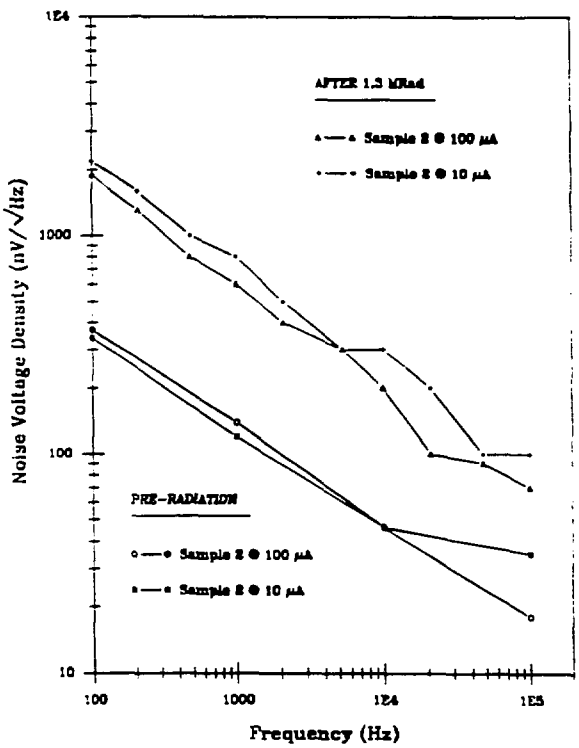

Fig. 7. Noise spectra for a MOSIS NMOS transistor with W/L = 100 µm/10 µm, both before and after a 1.3-Mrad (^{60}Co) total dose.