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CHERENKOV RING IMAGING DETECTOR FRONT-END ELECTRONICS*

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Abstract

The SLD Cherenkov Ring Imaging Detector uses a proportional wire detector for which a single channel hybrid has been developed. It consists of a preamplifier, gain selectable amplifier, load driver amplifier, power switching, and precision calibrator. For this hybrid, a bipolar, semicustom, integrated circuit has been designed which includes video operational amplifiers for two of the gain stages. This approach allows maximization of the detector volume, allows DC coupling, and enables gain selection. System tests show good noise performance, calibration precision, system linearity, and signal shape uniformity over the full dynamic range.

I. Introduction

This paper discusses the front-end electronics of the Cherenkov Ring Imaging Detector (CRID) [1] used in the SLD spectrometer [2] at the SLAC Linear Collider. As part of this system a semicustom analog IC was designed and produced, and so this paper will also discuss semicustom development and its applicability to detector front-end systems.

The CRID wire chamber detects single electrons created by ultraviolet Cherenkov photons, which photoionize in a gas containing 0.1% TMAE. The electrons drift at constant velocity within the drift box or TPC to a proportional sense-wire plane where they are detected. The detector plane has 10-cm-long wires on a 3 mm pitch. Typical gas gain is about 2×10^5 electrons or -32 fC/primary electron. Charge division, effected by means of an amplifier on each end of the wire, allows the calculation of the avalanche coordinate along the wire. A previous publication [3] describes the electronic system requirements of the CRID and the complete front-end system used on the CRID TPC prototype. The system considerations still apply with additional constraints, but the detailed circuitry has mostly changed to allow IC packaging.

II. Description of the System

Figure 1 shows the block diagram of the production front-end system. The hybrid, whose picture is shown in Fig. 2, is a single-channel, eleven-pin SIP, which plugs into a socketed motherboard that matches the 3 mm chamber pitch. Circuitry that biases the wire end to either plus or minus 200 V, allows the 39 kΩ carbon fiber sense wires to be heated, providing the option of burning off polymerized deposits [1]. In signal detection mode, the protection diodes are grounded. A detailed description of the system is presented in a companion paper submitted to this conference [4].

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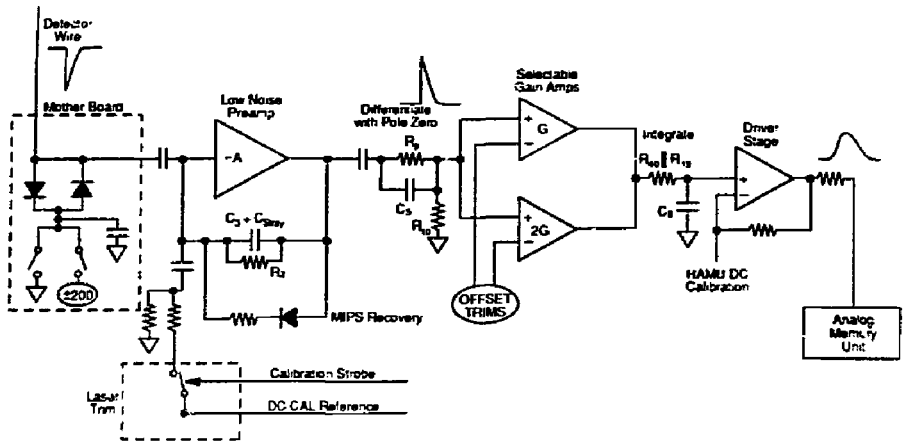

Fig. 1. Block diagram of the front-end system.

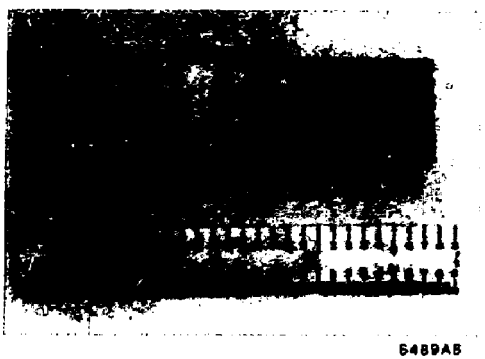

Fig. 2. Photograph of a single-channel hybrid.

Figure 3 is the circuit schematic of the hybrid with the semicustom IC treated as a block diagram. As shown in Fig. 1, there are three amplifier stages. The first stage is the low-noise preamp. It is implemented by using a discrete JFET input and a folded cascode pnp transistor on the hybrid supported by a voltage source, a transresistance amplifier, and a limiting diode on the Plessey 3703 IC [5]. The input impedance of the preamp is about 700 Ω, consistent with the requirements of charge division on a 39 kΩ fiber. The second stage is a video op-amp with digital gain select. The third stage is the driver video op-amp for the approximately 200 pF HAMU [6] load. Power is pulsed on the second and third stages to reduce consumption. The positive voltage to these two stages is switched, which enables a negative voltage switch in the IC. Most of the major hybrid functions are integrated, except for the calibration circuit and input transistors. Figure 4 is a schematic drawing of the semicustom IC with components from the hybrid, necessary for understanding the circuit added (within the dashed lines) for clarity. The design uses a Plessey MMB chip in a SO-16 package. The package height is 0.089 inches. The chip substrate is connected to V_{EE}.

III. The Semicustom Approach

In the CRID system, there are a number of areas in which analog IC arrays provide advantages that discrete designs cannot. The electronics are mounted very close to the detector. Circuitry volume is essentially subtracted from the TPC volume. Semicustom integration provides a reliable way to limit front-end system component volume. Earlier prototypes using a commercial multichannel hybrid preamplifier had shown unworkably large crosstalk; thus, the design now emphasizes a single-channel approach, with integration of the signal chain functions into a small package.

Semicustom IC processes are offered by vendors as partially fabricated integrated circuits with the metallization layers masked to customer specification. The unconfigured silicon chip can be viewed as a kit of parts

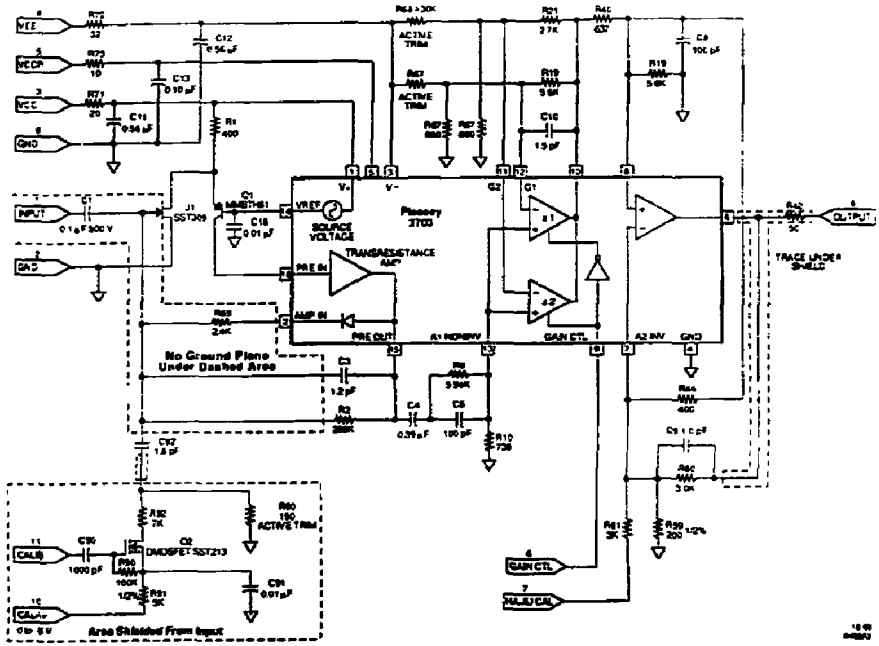

Fig. 3. Schematic of the single-channel hybrid, with the semicustom chip treated as a block diagram.

to which the customer provides the connections. There is a very broad offering of semicustom analog arrays available. The important considerations in selecting a process are as follows:

1. component qualities,
2. precision resistors and laser trimming,
3. two-layer metal,
4. packaging,
5. vendor engineering support and cost, and,
6. quantity and cost.

The bandwidth of amplifiers in front-end systems determines the IC processes that can be seriously considered. In the CRID case, the amplifiers need about 20 MHz bandwidth and a gain of about 20, resulting in a 400 MHz gain-bandwidth product. By selecting a video op-amp topology, the amplifier stages have close to the gain-bandwidth product of the individual transistors used. This permits the use of the Plessey MM series with npn transistors having f_T of 450 MHz, and also avoids the need for fast pnp transistors. Had ordinary, high open-loop gain op-amps been used, transistors in the GHz range of both polarities would have been needed. System frequency characteristics will limit the IC processes considered. High bandwidth will generally imply high cost. In a low-noise front-end system, the most important transistor is the first one. A process that provides an integrated low-noise transistor suitable for the detector would be ideal. In the CRID case, however, two discrete surface-mount transistors are used for good noise performance. Once a match between the system and the IC process is found, almost all of the remaining transistors should be locatable on the chip. In retrospect, an alternative strategy can be developed if one can find a process having excess bandwidth, then substantial savings in power can be achieved by the lowering of bias levels.

IC design usually has the limitation of small capacitor values, and these capacitors have large variations in value, as well. Resistors, too, have this broad variation in value. For instance, in our process they vary by ±25%. Tracking between resistors on a given device is ±3%, and in some processes can be as low as ±1%. Component variation sets the power variation, as well as, a large part of the bandwidth differences to be expected over a production run. Similar limitations in parameter control are dealt with by careful design in almost every IC product. Careful initial analysis must be made to show that designing with particular process specifications can result in a useful device. Later in the design process, statistical analysis of simulated circuits will indicate the viability of a particular design in production.

Some vendors offer thin-film resistors on their semicustom arrays, which can then be laser trimmed. The use of thin-film resistors avoids the large temperature and voltage coefficients of IC-process base-diffused resistors. Laser trimming can also eliminate absolute value variations. Thin-film components are offered by the

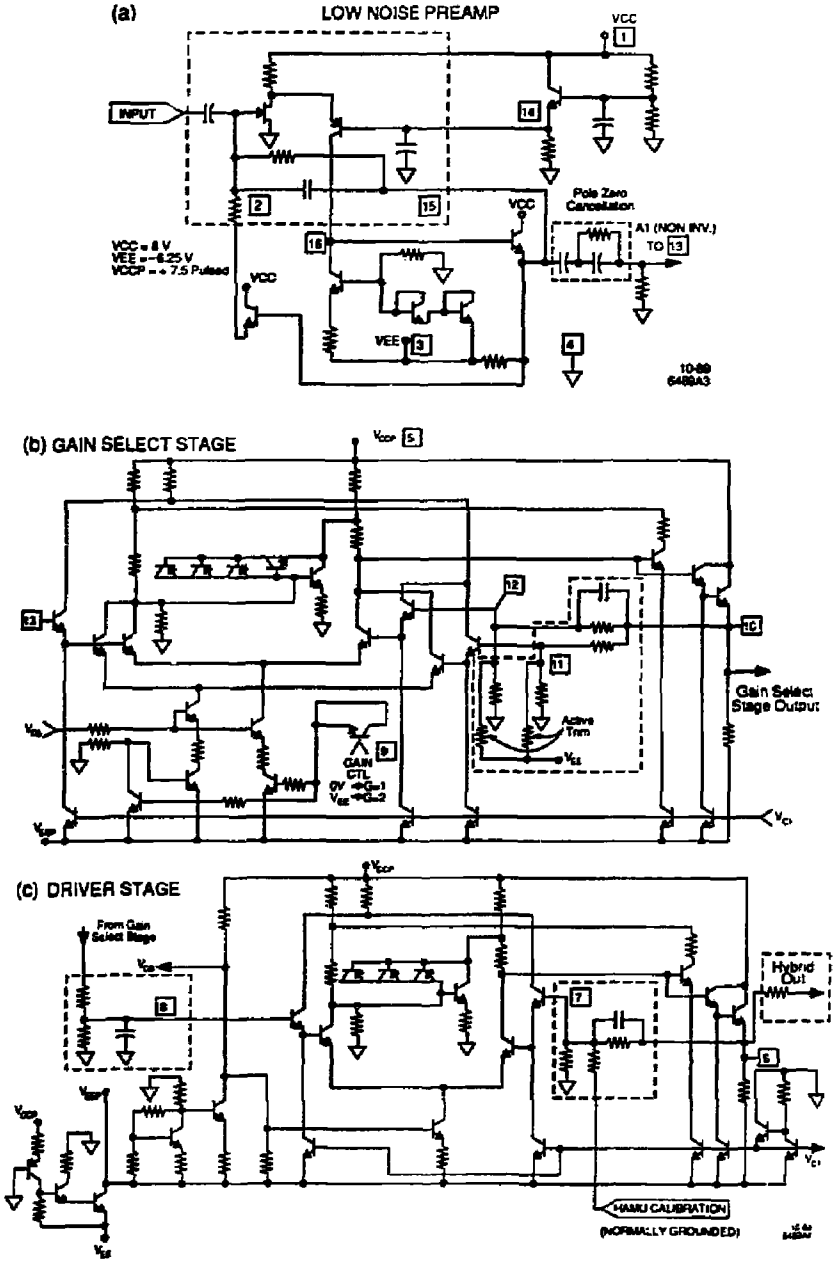

Fig. 4. Schematic of the semicustom IC, with components from the hybrid necessary for understanding the circuit added for clarity: (a) the low-noise preamp, (b) the gain-selectable amplifier stage, and (c) the driver stage.

more expensive processes; thus, this option implies not only higher processing cost, but higher engineering and overhead cost, as well. Where precise resistor values are needed in the miniaturized system, they can be placed on the servicing hybrid circuit, with a large increase in component volume offset by an increase in system versatility and by an increase in the ease with which changes can be made. In the CRID system, laser trimmed hybrid thick-film resistors are used for the two signal filters, preamp, calibration network, op-amp feedback, series output element, active DC trim, driver frequency compensation, and power filters. These 25 precision resistors are used for functions for which the IC process could not provide sufficient accuracy. With the gain resistors and filters, design changes are also very likely, and their integration would be risky.

Another option available on more sophisticated processes is two layers of metallization traces, instead of the one layer available on simpler arrays. More complex and compact circuitry is possible with two layers. Precision and low-noise designs are aided, since broad grounds, shielding, and more direct connections can be designed into such an IC.

After finding vendors with processes providing components that match the system requirements and topology, channel count and packaging must be determined. A system requirement for the CRID is the reduction of interchannel crosstalk. This specification derives from the existence of minimum ionizing particles (MIPS) which at times will produce as many as 900 primary electrons. This, when compared to the need to detect single electrons, underscores the need to keep crosstalk from these large signals from saturating nearby amplifiers.

The single-channel hybrid using surface-mount packages chosen for the CRID system allows extensive interchannel shielding. The back of the hybrid is conductive and grounded, and the motherboard has 5-mm-high metal guards between hybrid pin rows. Interchannel crosstalk within a multiple-channel chip is quite small, since the back of the chip is conductive and the substrate couples closely to it. However, in running traces and bond wires on and off the chip, coupling is substantial. Newer bonding schemes, such as TAB and chip-on-board using bump bonds, will be useful in creating low-crosstalk multichannel chips in the future.

Prototyping is greatly simplified using surface mount epoxy packages over chip and wire. Wire bonds imply hybrid modifications with probe and bonding stations. The CRID hybrid needed extensive modifications as the hybrid was matched to the prototype IC and the system requirements. Printed resistor modifications were made with a diamond hand scribe and a microscope. This allowed many circuit variations to be created and evaluated, including changes in the groundplane configuration. Chip and wire, on the other hand, implies at least four times less circuit area per function, but has higher prototyping costs and longer intervals between prototypes.

Design of a front-end system with an IC requires a circuit simulator such as SPICE. Some vendors offer analog engineering design to a given specification. However, detector front-end systems often fit into a very constrained environment, such as space, allowable crosstalk, small signal shielding, power consumption, and/or filtering precision. Designing only a specification and having the circuit engineering done by contract is difficult to do successfully, since the front-end electronics are so closely linked to the detector grounds and geometry. Vendors also offer SPICE component parameters, software packages, and functional cell examples to assist the customer in setting up a simulator. This approach is usually much less costly, and was chosen by the CRID group, with Plessey doing the chip layout of the supplied circuit. If the design of the front-end electronics of a detector system is contracted, then extensive resources must be allocated for specification development and prototype verification. Chip engineering, layout, and testing design are a large part of final circuit costs, particularly when the chip count is below 100,000 parts. The CRID needs 8,000 channels for its barrel detector, with another 8,000 for the endcaps needed in the future. For this low IC volume, vendors with low prototyping and engineering costs are essential. When the component requirement analysis was begun, two classes of processes were available. The first was the low cost, low speed, mature npn arras—such as that offered by Plessey Semiconductor, from whom a prototype IC cycle could cost as little as $4,000. The second involved the more recent technologies, having high frequency pnp transistors and npn transistors in the multiple GHz range. These exotic arrays have typical prototyping costs in the $40,000 range. The choice for the CRID group was clear.

IV. Signal Shape

The function of the front-end electronic system under discussion is to measure the time-of-arrival of the drifting electron, and to measure the location of the avalanche along the resistive anode wire of the proportional chamber by the use of charge division. Thus, amplifiers are placed at both ends of the anode wires with the expectation of comparing the measured pulse heights. The requirement for a common digitizing system throughout SLD electronics mandates the use of the HAMU and a fixed number of time samples. Each of the analog signals therefore will be digitally sampled only a few times, and one must develop an algorithm to characterize it by its time-of-arrival and its pulse height, based on these data. A simple and efficient algorithm for determining these parameters is available if the output

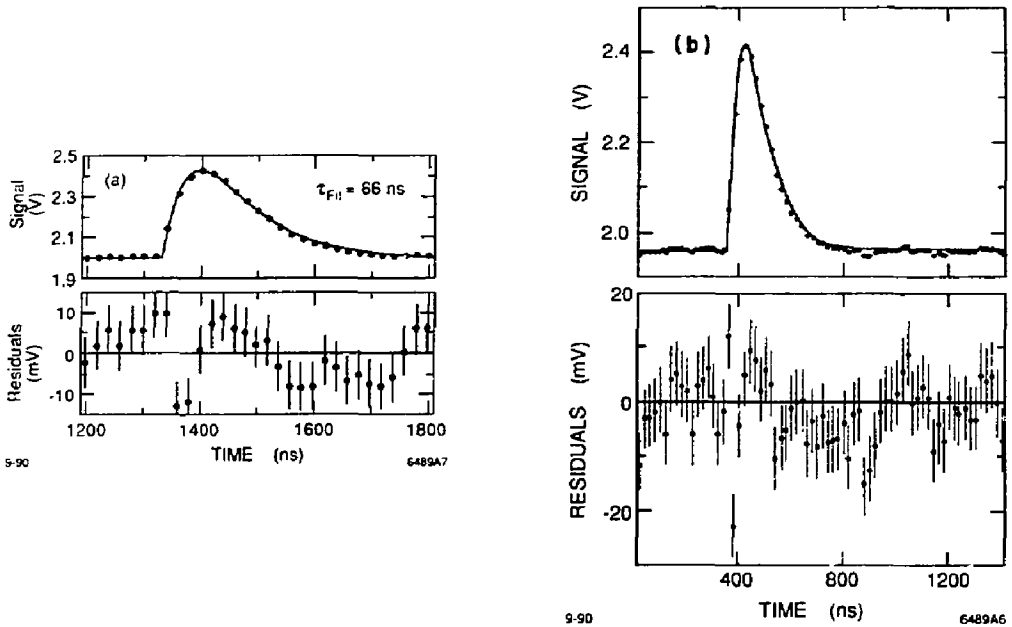

Fig. 5. Comparison of the theoretical and the actual pulse shape response of the hybrid to input signals. A LeCroy Research ICA was used for the measurement, with the time bins set to 20 ns. The lower plot shows the residuals of the fit: (a) an impulse input into a properly configured amplifier; (b) a simulated chamber input signal into an amplifier whose pole-zero time constants have been tuned to cancel the long tail from an actual chamber. In both cases, the solid line is the resultant fit.

signal shape is RC-CR or $(1/t)e^{-t/\tau}$. This, therefore, became one of the system specifications.

The output signal is digitized every 67.2 ns by the HAMU hybrid, and digitally filtered by a deconvolution algorithm yielding the amplitude and time-of-arrival of the input signal. At this time, the sampled analog signal may be discarded. The filter assumes the RC-CR shape. In simulations, only three samples are needed for a pulse determination, and double pulses are resolved very well. The RC-CR shape requires a low-noise preamp, followed by differentiation with pole-zero cancellation. This is then buffered by the gain selectable amplifier, followed by an integrator. The driver stage must accommodate the 200 pF load of the HAMU.

To avoid errors in the digital filtering, the signal must fit the algorithm well, over the entire signal range. Wide bandwidth amplifiers with moderate open loop gain and feedback provide linear gain stages. Discrete capacitors and resistors provide precision shaping, as long as the amplifiers are of much greater bandwidth (20 MHz) than the 67 ns τ shaping. As Fig. 5(a) shows, the calculated and actual signal shape fit closely. In the fitting procedure, all of the variables (amplitude, τ, and start time of the pulse) remain free. In this fit, τ was fit to 66 ns. Simulations show that τ will not vary more than ± 1 ns over production due to transistor bandwidth spread. In Fig. 5(b), the pole-zero time constants of the amplifier have been adjusted to cancel the long tail of a signal from an actual chamber, as discussed in the section on MIPS recovery. An input signal emulating that of a chamber has been used, rather than an impulse charge. The fit in this case is seen also to be quite good.

Another requirement is dynamic linearity. The feedback amplifier topology gives excellent linearity. Figure 6 shows the signal peak amplitude versus calibration input. The amplitude obtained by fitting the data to a theoretical RC-CR pulse shape over the same dynamic range shows identical linearity performance, indicating that the filters are not affected by signal size.

The use of amplifiers which possess low noise and approximately RC-CR pulse shape to deconvolve primary chamber signals has been discussed previously. [7–10] Our hybrid production amplifiers possess the necessary characteristics to maintain the physics goal of better than 1% position resolution, achievable by charge division, in the wire dimension.

V. MIPs Recovery

In the detector, primary minimum ionizing particles (MIPS) that originally produced the cone of ultraviolet radiation of interest, create signals as large as 900 times typical. To protect adjacent channels, a heavily

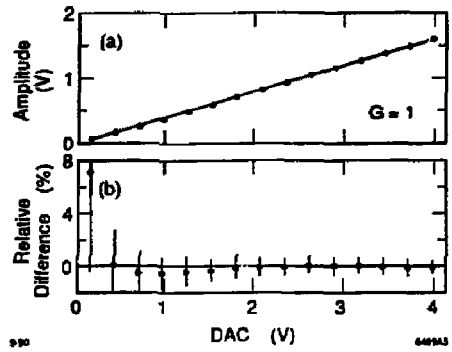

Fig. 6. Linearity plot for the amplifier hybrid, using the calibration input.

shielded packaging approach is used. With extensive simulation and prototyping, a front-end with fast recovery from these large signals has been developed. The input charge is limited by a transistor in the IC, which acts as a diode that shorts the integrating capacitor C_3 shown in Fig. 3. Its collector is tied to V_{ee} in order to limit feedback capacitance. The series resistor in the emitter circuit was chosen by trial and error during hybrid prototyping. The diode junction is a nonlinear capacitance for small signals, but the 0.5 pF emitter-base capacity of the IC npn is small enough to limit this to an almost undetectable level.

The best MIPS recovery for the subsequent amplifier stages was found in single stage differential amplifiers, which are inherently self-limiting when driven to the rail by the one-diode drop output, 800 mV, of the preamp stage. The gain control stage is DC coupled to the driver, and the driver DC coupled to the HAMU, to limit the baseline shift caused by the MIPS. Initially, the first stage was to have pulsed power, but large input and output coupling caps were needed to minimize DC shifts and, therefore, the preamp required DC power. Each gain control amplifier is skewed in its bias to the negative side, so that a trim resistor on each inverting input to V_{EE} allows laser trimming to 1.3 V nominal for the HAMU input. Single-stage differential DC coupled gain stages give good MIPS recovery.

Laboratory results for MIPS recovery are good. Figure 7 shows MIPS recovery for a number of input charge and duration combinations. In this figure, the left-hand curser is placed at the end of the input ramp charge stimulus. The right-hand curser marks the return of the output to within 1 V of the baseline, where it is possible to extract a single electron signal within the amplifier's 2 V dynamic range. In these tests, the input charge is created by a voltage step appearing across a small capacitor. Theoretically, the pole-zero filter should be set to match the preamp time constant $R_2(C_3 + C_{stray})$. However, as the signal from an actual detector has a large tail in time, this long tail is approximately cancelled by empirically adjusting the pole-zero filter. MIPS recovery testing of the amplifier on the chamber remains to be done.

VI. Power Pulsing

Pulsed power is used to limit power consumption to approximately 60 mW per channel. As mentioned above, the low-noise preamp has large AC coupling capacitors at its input and output, and must remain on. The two secondary stages have a quiescent DC bias of about −5 mV at their input. The input time constant from turn-on is about 2 ms, which is much larger than the data acquisition time of 100 μs; and the sloped baseline is slowly varying and is corrected digitally. The gain stages settle to their operating values at power-up in 7 μs, as indicated in Fig. 8. During normal operation, the amplifiers will be pulsed on for a period of about 200 μs. The accelerator will provide beam 120 times per second so the duty cycle is about 2.4%. Figure 4 shows the power switch internal to the IC that switches V_{EE} on, in response to a pulsed V_{CCP}.

VII. Noise

An earlier paper [3] discussed noise considerations in some detail. Noise must be as low as possible in order that the charge division measurement yields the spatial resolution required. Of the two input geometries discussed, the JFET Siliconix SST309 in a canonical preamp configuration was selected. A total capacitance of 19 pF was measured from input to ground at the motherboard socket for the amplifier, with the amplifier removed. The channel resistance of the JFET with 8 mA drain current is about 50 Ω, and thus it will be less sensitive to input capacitance. The detector sense wires

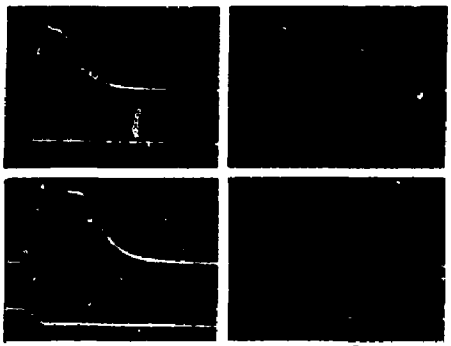

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Fig. 7. Plot of MIPS recovery for various combinations of duration and input charge. The time shown is the time to recover to within 1 V of the baseline, as measured at the output of the amplifier.

a) 200 electrons arriving over a 100 ns time
b) 200 electrons arriving over a 500 ns time
c) 500 electrons arriving over a 500 ns time
d) 1000 electrons arriving over a 500 ns time

are 7 μm-diameter carbon wires that offer a resistance of 39 kΩ, creating Johnson noise of about 800 e^- in our frequency range. The hybrid prototype demonstrated that the preamp functions included on the IC work quite well. An improvement in noise is made by bypassing the source V_{REF} with the discrete capacitor C_{16} (Fig. 3).

Noise simulation of the secondary amplifiers was not done. The noise contribution of these stages was found to be significant too late in the prototyping process to change the IC design. Noise measurements begin by measuring charge gain, and then digitizing at 20 ns intervals with no input signal. The standard deviation of ten adjacent samples is taken as a measure of the rms noise, and normalized using the charge gain. An rms noise of about 1600 e^- rms, with the detector connected was measued. This increases the coordinate measurement error from 0.7% [3.8] measured with the first prototype amplifier, to its present value of 1.2% of the wire length [8], a value acceptable for the physics measurement.

VIII. Calibration

Channel calibration must be done to an accuracy of 0.5%. On each hybrid is a DMOS FET transistor that switches from high impedance to about 50 Ω when driven by an 8 V positive step. Its source is connected to a negative reference voltage; and when switched generates an analog reference step that settles in less than 10 ns. This step is divided by about 35 using an active laser-trimmed divider. The circuit is shown in Fig. 3.

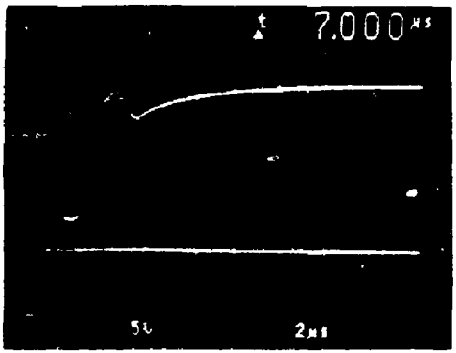

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Fig. 8. Timing diagram showing the relationship between turn on of the pulsed power and amplifier readiness.

Capacitor C_{92} can be an inexpensive one, since the resistor R_{90} is trimmed by dynamic measurement

For maximum accuracy, the digital-to-analog step conversion is performed close to each input on each amplifier substrate, so that untrimmed effects from amplifier bus location and circuit trace stray capacitance are eliminated. This introduces the problem of shielding the step generation and switching network from the inputs. The first design goal in this shielding exercise is to place the calibration strobe (pin 11) as far away as possible from the input signal (pin 1) on the hybrid. The second design goal is to properly configure the motherboard, which services 93 wires and holds 186 amplifier hybrids in two rows. Eight layers are used, many being power and ground planes. The CMOS shift registers for holding the digital calibration pattern and the digital step generators are both placed on the side of the motherboard opposite to that of the amplifiers, using the power and ground planes within the motherboard as additional shielding. The voltage step is gated with dual HCMOS analog switches. When a gate is off, the gate output is switched to ground. Switch feedthrough of the digital step is about 20 mV at the output of the amplifier at gain one. Motherboard power planes successfully shield the amplifier inputs at this point. The amplifier inputs are all on the outer edges of the motherboard, and the inner pins receive the step, CALIB. Low, grounded shields are placed between each row of hybrid pins. The CALIB signal on the hybrid is on the deepest conductive layer, with a ground plane over it. In addition, the back of the hybrid is a ground plane. Crosstalk to the input, for a zero volt step, produces an acceptable 50 mV pulse, as measured at the output. Adjacent channels have very low response to the CALIB signal.

Figure 6 shows that a linearity plot for an amplifier using the calibration input has a nonlinearity for very small signals, as shown by the residuals. This is probably due to the measuring software, however, these smallest signals will not be used in generating calibration coefficients. Actual channel-to-channel calibration accuracy depends on the dynamic laser trim accuracy and component stability, which will be discussed in greater detail in Ref. 4.

IX. Gain Select

The amplifier gains must be chosen to place the CRID's single electron signal appropriately within the HAMU operating range of 1 to 3 V. The inclusion of a gain selection specification reflects a situation of incomplete information, both about the chamber operating gas gain and the resolution of the HAMU. The nominal gain setting, g=1, is characterized by a voltage-to-charge ratio of 17 mV/fC. In initial hybrid prototypes [3], the two gains were g=1 and g=4, but g=4 had to be reduced to g=2 when system ground feedback sensitivity was discovered. The mechanism for this problem centers on driving the 200 pF HAMU load through a 15 cm trace. The resonance and impedance minimum of this network is around 30 MHz, where it looks like about 10 Ω. Because the driver is on the same substrate as the preamp input, the large currents needed for the highest frequencies cause ground shifts to appear as signal at the input, since the input is referenced to grounds off the hybrid. There is ample phase shift available through three stages of amplification on the hybrid to cause positive feedback and, therefore, oscillation. Absolute stability is achieved by attentive ground optimization and the above reduction in system gain. The combination of both of these techniques lowers the feedback ground signal to a system gain of less than one, with resulting stability.

The gain control circuit on the IC is shown in Fig. 4, and Fig. 3 shows the digital gain control hybrid pin, for which 0 V gives the low gain setting and V_{EE} gives a gain of two. The two amplifiers shown in Fig. 4b have separate input differential pairs with their collectors joined to use the common top end. The independent current sink tails are switched, which allows the feedback path to either inverting input to be selected. This gain-control scheme works well, with few hybrid components required. It should be noted that the output driver amplifier has a circuit similar to the gain control stage, but has a larger output transistor.

X. Conclusion

Designing the CRID front-end system using a semicustom IC simplifies a number of difficult design requirements. The Plessey process provides a straightforward and low-cost path toward system miniaturization. The performance of the front-end amplifier system has met all of the design specifications, while permitting the CRID TPC volume to be maximized.

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