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ANALYSIS AND SIMULATION OF THE SLD WIC PADS HYBRID PREAMPLIFIER CIRCUITRY*

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Abstract

The SLD PADS electronics consist of over 9000 channels of charge-sensitive preamplifiers followed by integrated sample/hold data storage, digitizing, and readout circuitry. This paper uses computer simulation techniques to analyze critical performance parameters of the preamplifier hybrid including its interactions with the detector system. Simulation results are presented and verified with measured performance.

I. Introduction

The SLD is a large detector for high-energy colliding beam experiments, scheduled to go into place at SLAC at the end of 1990. The WIC (Warm Iron Calorimeter) is one of many detector subsystems; it is used for muon identification and calorimetry based on charge measurement of signals from limited streamer discharge tubes. The signals are derived from "pads" coupled to the discharge tubes in a complex tower structure which has been described in the literature [1].

The WIC pads electronics subsystem consists of 9216 channels of charge-sensitive hybridized preamplifiers followed by analog data storage, digitization and serial readout [2]. The energy resolution of the calorimeter requires an overall charge measurement accuracy of about±10%. The completed system has achieved an accuracy of about±5%.

The purpose of this paper is to demonstrate the use of computer simulation techniques in analyzing and characterizing the performance of the linear front-end circuits of the preamplifier. This work permits us to better understand, and hence control, the qualitative and quantitative performance of the overall system.

II. The Preamplifier Circuit

The preamplifier circuit (Fig. 1), designed by B. Wadsworth at MIT, consists of a conventional op-amp integrator with a discharge-time constant of 100 μs (well within the minimum 8 ms beam crossing at SLC), followed by an AC coupled op-amp differentiator that produces a shaped output pulse peaking at 5–7 μs. The output sampled at the peak is therefore proportional to the signal charge at the input to the preamp. In the actual system the output pulse is strobed into a sample-and-hold circuit at a programmable time (nominally 6 μs) after beam crossing. The nominal charge gain of the circuit is 1.48 V/nC, and the full-scale charge is 3.4 nC, giving a full-scale peak signal output of about 5 V. Special features of this circuit important for this paper are:

- The 13 Ω series input resistor added to present a nominal 50 Ω input impedance for line termination over the frequency of interest.
- The 680 pF capacitor for charge gain calibration of the overall system using the external voltage ramp, VCAL. It is connected to the circuit input with a FET switch during calibration.
- The VTEST input that is used for test purposes, and which can be used to measure the equivalent shunt detector capacitance, CPAD.
- The voltage divider at the output, which generates a pedestal of 0.6 V to match to the CDU sample-and-hold circuit [3].

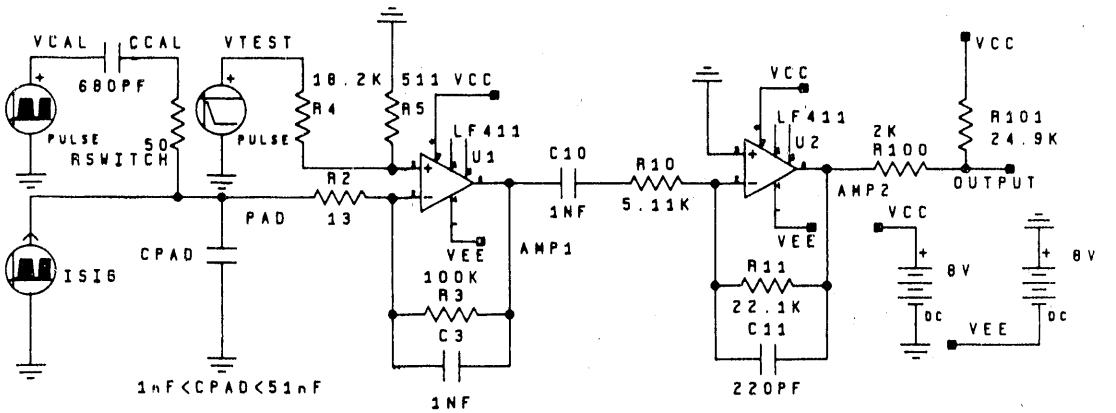

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Fig. 1 Simulation schematic of the preamplifier. The input current source represents the input charge, while the two voltage sources are used for calibration and VTEST modes. The operational amplifiers are modeled using a Boyle-type subcircuit model. CPAD represents the detector capacitance, which can vary from 1 to 51 nF.

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The preamplifier circuit as shown was produced in large quantity, almost 5000 units, as a dual-channel thick-film hybrid in a 15-pin SIP by the Tong Hsing Company in Taipei, Taiwan, based on a design and layout done at SLAC. All resistors were trimmed to ±1%, but there was no overall active trimming of gain or peaking time. The acceptance limit for uncalibrated charge gain was ±13% to allow for component variation. Acceptance limit of the 680 pF calibration capacitor was ±2%. The op-amp as originally specified was the National LF351, although it is likely that the actual chips used in manufacture are of improved performance, namely the LF411. The LF411 will be used thoughout all simulations that follow.

III. Circuit Simulation and Models

The operational amplifiers (type LF411) in the circuit are modeled as subcircuits using a Boyle-type operational amplifier macromodel [4]. This model represents the behavior of the amplifier for both linear and nonlinear operation, and includes effects from the amplifier open-loop gain and phase characteristics, output slew rate limiting, finite output resistance, differential and common mode voltage gain, input impedance, input bias current, and output voltage and current limiting. The detector system is modeled by a current source (representing the ionization charge generated in the limited streamer discharge tube) in parallel with a capacitance CPAD (representing the physical capacitance of the detector streamer tube and electrode structure). The measured range of this capacitance in the detector is 1 nF to 50 nF, and varies due to detector geometry. A rectangular charge versus time distribution is used for the input signal. The physical signal from the ionization process has a more complex time structure than this simple model, but results will show that the exact form of the input charge distribution is not critical. The two voltage sources shown are for the calibration and VTEST function simulations. The calibration voltage ramp is used to inject a known charge (Q=CCAL*VCAL) into the amplifier to calibrate the amplifier, as well as all the subsequent linear processing stages. The "on" resistance of the FET calibration switch is assumed to be 50 Ω in our model. The rise time for the calibration voltage VCAL (300 ns) is the same as that used in the physical system. This rise time controls the duration of the input calibration current pulse and limits the instantaneous input current to avoid saturation. Similarly, the negative VTEST voltage source has a 300 ns rise time to correspond to the physical system.

This system has been analyzed using commercial electronic CAE tools and a commercial Spice-derivative analog simulation package [5]. The Boyle op-amp macromodel parameters for the LF411 are also from commercial vendors [6].

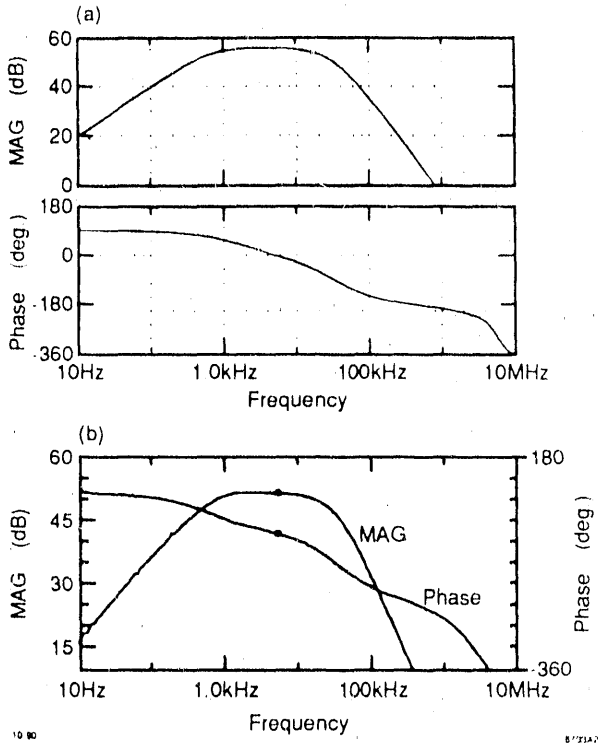

Fig. 2 Simulated (a) and measured (b) small signal frequency responses of the preamplifier.

IV. Simulation Results and Laboratory Measurements of the Preamplifier

To test the validity of the circuit model, we have compared the simulation results with laboratory measurements of the preamplifier. Figures 2(a) and 2(b) present the simulation and measured complex frequency response, while Figs. 3(a) and 3(b) show the simulation and laboratory measurements of the preamplifier complex input impedance. There are three regions of interest in these curves. In the low-frequency range (below 1 kHz) the agreement between simulation and measurement is excellent. In this region the input impedance is dominated by the 13 Ω input resistor, while the gain characteristic is dominated by the differentiator formed by C10 and the second stage. Similarly, in the midband region (between 1 kHz and 2 MHz) there is good agreement in the simulated and measured curves. The midband gain of the simulation is a little high (55 dB vs. 52 dB measured) but the overall complex gain characteristic is in general agreement. The higher op-amp model gain also explains the difference in input impedance (34 Ω vs. 46 Ω), as it can be shown analytically that the input impedance of the first stage in this midband regime is approximately:

$$Z_{in} \approx \frac{1}{2\pi C3\ GBW},$$

where GBW is the gain-bandwidth product of the amplifier.

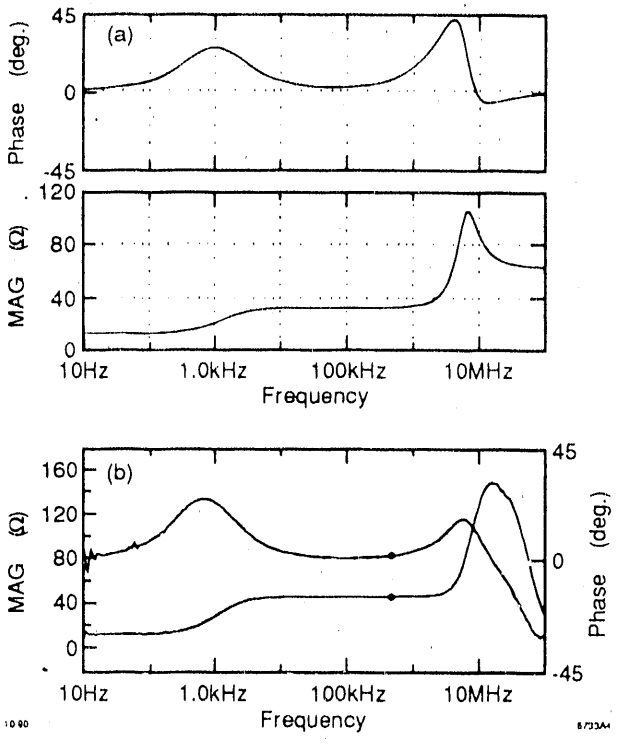

Fig. 3 Simulated (a) and measured (b) input impedances of the hybrid preamplifier.

The third region in the curves (2 MHz to 100 MHz) also shows general agreement between the model and the measurements. The amplifier shows a parallel low Q resonance which raises the input impedance to a maximum. The model and lab results both show the resonance (simulation resonance at 7 MHz, lab measurement at 15 MHz), and the model predicts a lower maximum impedance of 105 Ω versus the measured 150 Ω. This discrepancy is largely due to the simplified representation of the output impedance and the absence of parasitic elements in the Boyle model (such as lead inductance and parasitic capacitance) that would be significant in this 10–100 MHz range. The unity gain frequency of the preamplifier is 600 kHz, so that the major effect of these high-frequency resonances involves the interaction of the physical detector with the input integrator. In our system the capacitance of the detector system is in parallel with the input impedance, so that the input detector capacitance dominates the input impedance at this resonance. For the frequencies where the system has gain, there is very good agreement between the simulation and laboratory measurements.

Figs. 4(a) and 4(b) show the simulated and measured transient responses of the amplifier without any input capacitance CPAD. Note the 5 μs peaking time in both figures and the excellent agreement for the overall pulse shape. Table I shows the sensitivity of the system to variations in sampling time relative to the maximum. The required time stability for 1% accuracy is easy to achieve.

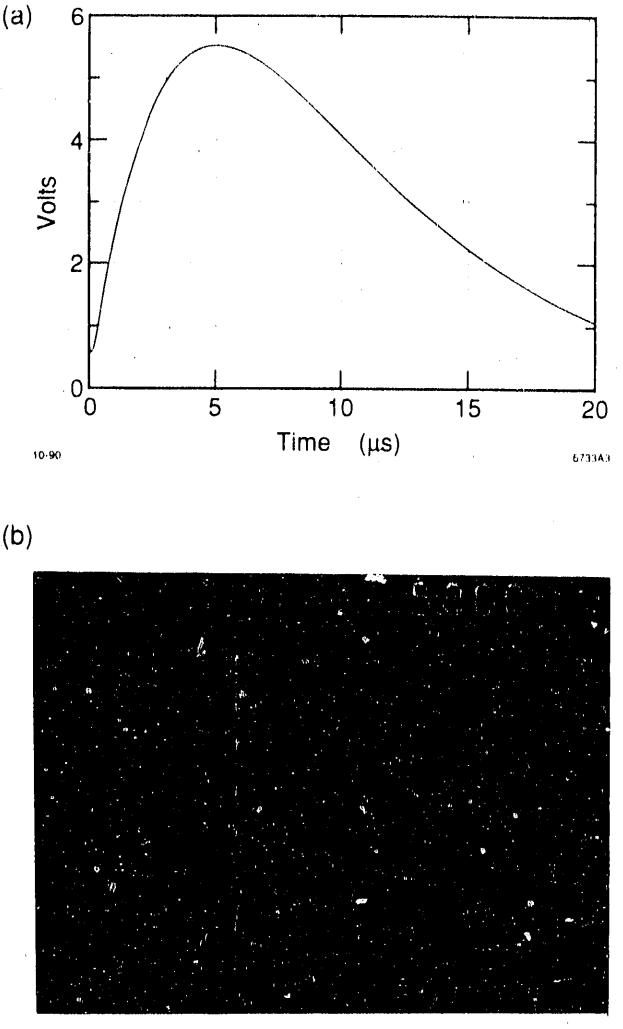

Fig. 4 Simulated (a) and measured (b) transient responses for full-scale (3400 pC) input charge and zero pad capacitance.

Table I
Time Shift of Sampling Edge Relative to 5 μs for Specified Errors

ERROR	− Shift (μs)	+ Shift (μs)
1%	−0.63	0.71
5%	−1.36	1.68

V. Input Charge Distribution Effects

Figure 5(a) shows the response of the system (with a nominal 10 nF pad capacitance) to 3400 pC input charges with 50, 100, 200 and 300 ns total duration. Note that the variation in output amplitude at the 6 μs sampling time is less than 0.2%. Figures 5(b) and 5(c) show the waveforms at the input node and at the first stage integrator output during these short intervals. The dominant effect of the charge duration is to change the amplitude of the transient voltage developed at the input node, and to change slightly the voltage ramp waveform at the first stage output. Thus the overall shape of the input charge

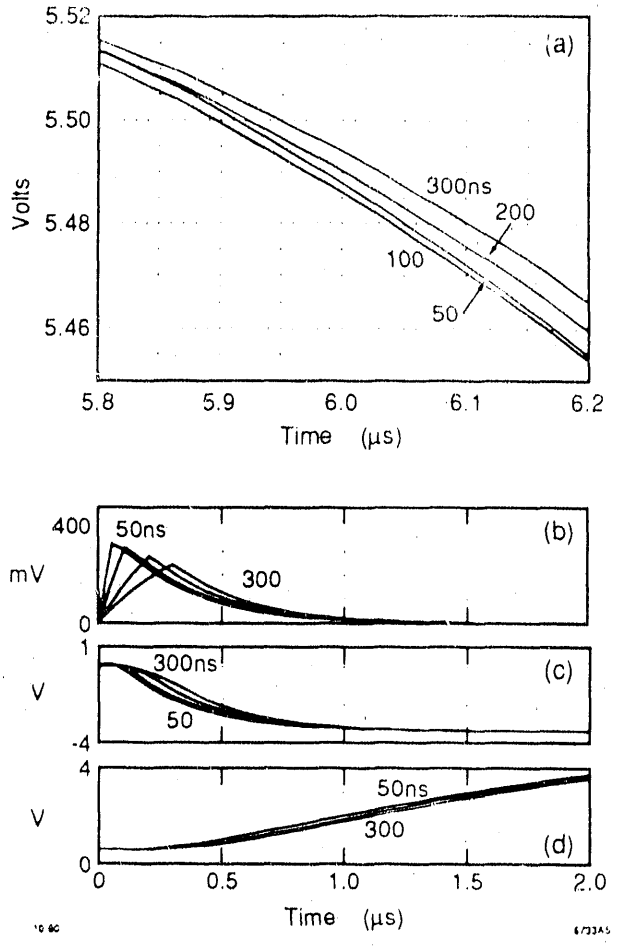

Fig. 5 Simulation study of input charge duration effects. (a) Output pulses for the system with a 10 nF detector capacitance and 3400 pC input charge, for durations of 50, 100, 200 and 300 ns. At the 6 μs sampling time, the variations in amplitude are less than 0.2%. (b) The waveforms at the detector node, (c) the waveforms at the first-stage integrator output, and (d) the waveforms at the preamplifier output.

distribution is not significant for durations of less than 300 ns, as is the case for signals from the streamer tubes. Similarly, note the importance of the capacitance at the input node. This detector capacitance keeps the transient voltage developed at the amplifier input from exceeding the differential voltage range of the op-amp inputs, which could occur for high instantaneous currents.

VI. Effects of Variation of Detector Capacitance

Figure 6 presents a family of output waveforms for the system with a fixed 3400 pC input signal, with a pad capacitance of 1, 11, 21, 31, 41 and 51 nF. The simulation results show a variation in peaking time as well as total amplitude. For the 1 nF to 51 nF range example, a time shift of nearly 2 μs is observed. If a fixed 6 μs sampling time were used without any correction, errors in the range

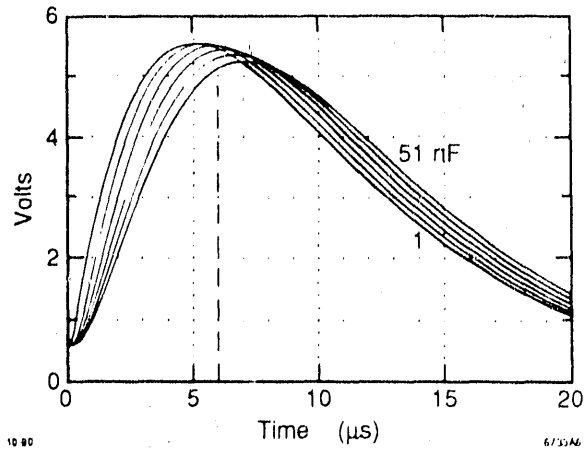

Fig. 6 Simulation study of detector capacitance effects. Preamp output pulses are shown for a 300 ns 3400 pC input and 1, 11, 21, 31, 41, and 51 nF pad capacitances. A 2 μs shift in peaking time is evident. This shift can be calibrated out to first order in the gain calibration process.

of 8% would be introduced. Because the peaking time varies from 5 to 7 μs, 6 μs has been selected as an optimum since it minimizes sensitivity to timing variations.

VII. Calibration Performance

The preamplifier incorporates a calibration capacitor which is used to inject a known charge into the system. This calibration system also largely compensates for the peaking time shift demonstrated in the previous section. The calibration capacitor is switched under logic control via a FET switch. Thus in the calibration mode, this capacitance appears in parallel with the detector capacitance, while it is switched out (FET off) during the normal operation of the system. There is therefore a residual error. The magnitude of this effect is shown in Figure 7, which shows the residual calibration error as a function of sampling time over the 1 nF to 51 nF range of detector capacitance. This effect is greatest for small detector capacitance. The error introduced at the 6 μs sampling time is seen to be less than 0.4%.

VIII. Effects of Detector Capacitance on the VTEST Function

The preamplifier includes a VTEST function to measure the attached detector capacitance CPAD and to verify the connections between the preamplifiers and the detector. It can be shown analytically that the peak voltage developed at the preamplifier output is approximately:

$$V \approx -0.041\ VTEST\left(1 + \frac{CPAD}{C3}\right).$$

Figure 8 shows a family of preamplifier output pulses over the range of detector capacitance for VTEST = −2.5 V. Figure 9 presents a comparison of the analytic expression with the simulation output sampled at 6 μs. Note that for large capacitances the measurement via VTEST may be as much as 12% lower than the approximation. Faults such as shorts or opens in the cables are easily detected.

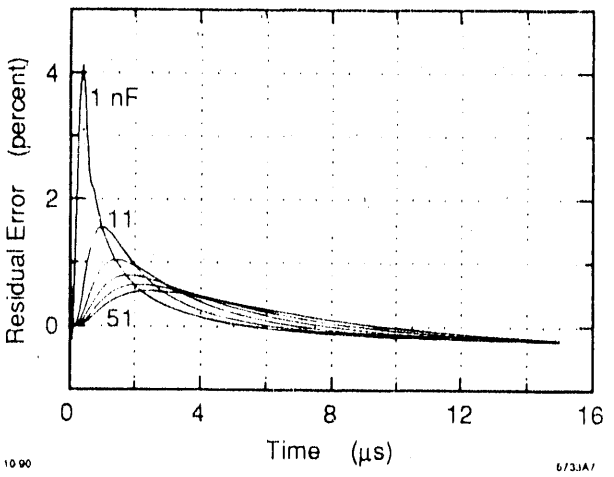

Fig. 7 The Calibration Residual Error is shown for 1, 11, 21, 31, 41, and 51 nF CPAD. At the 6 μs sampling time, the residual is seen to be less than 0.4%.

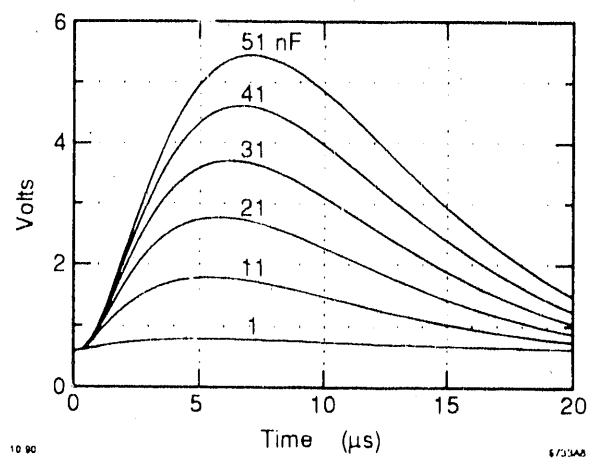

Fig. 8 Simulation study of the VTEST function for -2.5 V VTEST and 1, 11, 21, 31, 41 and 51 nF CPAD. This function is used to measure the detector capacitance *in situ* and as a connection check.

IX. Summary and Conclusions

The use of the computer simulation of the detector/preamplifier combination has been shown to be a reasonably accurate predictor of preamplifier performance, but more importantly has allowed us to demonstrate, analyze and quantify selected aspects of its behavior in the system. In particular, this analysis has confirmed wide tolerances on system timing, and has clearly shown that self-calibration can compensate for the effects of large variation in detector capacitance. The selection of 6 μs for fixed time sampling has been shown to be entirely reasonable for this system.

Two discrepancies are to be noted. First, the input impedance determined by the simulation has been shown to be 25% lower in the midband region than measured. This difference is known to be related to the first stage

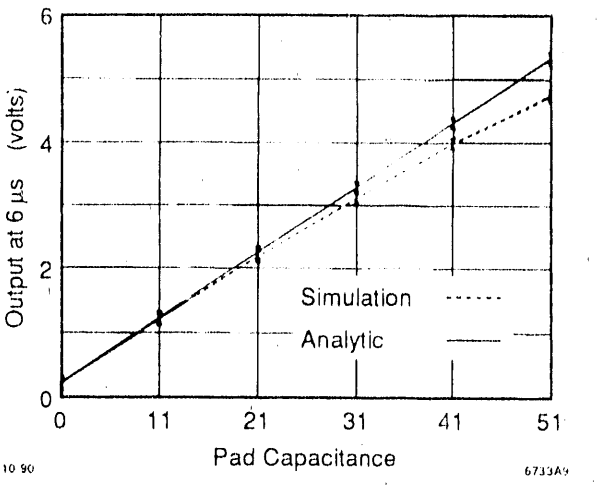

Fig. 9 Comparison of Simulation VTEST function (sampled at 6 μs) with the analytical approximation for 1, 11, 21, 31, 41, and 51 nF CPAD. The difference increases to -12% at the maximum capacitance of 51 nF.

op-amp model parameters. This effect is not critical to the charge measurement and only affects line termination and total charge collection time. Second, the capacitance CPAD, as determined by the VTEST function in the actual system, typically indicates a detector capacitance considerably lower by some 25–35% than that measured by a conventional hand-held digital capacitance meter. Although this discrepancy is not completely understood, it seems quite likely that channel-to-channel capacitive coupling not included in our model is responsible, as VTEST is pulsed for the detector as a whole. Evidence obtained by isolating channels on the detector supports this theory. The simulation model could be extended to include cross-coupling of multiple channels to study this effect.

Acknowledgements

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[5] The CAE software used is from Viewlogic Systems (Marlboro, Massachusetts) and the analog simulation software is the PSpice package from Microsim Corporation (Irvine, California). The hardware platform used is a Sparcstation from Sun Microsystems (Mountain View, California).

[6] The LF411 Macromodel parameters are provided by Microsim Corporation and Texas Instruments, Inc.

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