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MONOLITHIC JFET PREAMPLIFIER FOR IONIZATION CHAMBER CALORIMETER*

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Abstract

A monolithic charge sensitive preamplifier using exclusively n-channel diffused JFETs has been designed and is now being fabricated by INTERFET Corp. by means of a dielectrically isolated process which allows preserving as much as possible the technology upon which discrete JFETs are based. A first prototype built by means of junction isolated process has been delivered. The characteristics of monolithically integrated JFETs compare favorably with discrete devices. First results of tests of a preamplifier which uses these devices are reported.

Characteristics and Noise Behavior of N-Channel Diffused JFETs

N-channel JFETs obtained by a p^+ gate diffusion into an n-doped epitaxial layer which constitutes the channel are widely used in high energy physics (HEP) and still provide the best noise performance as input devices in charge sensitive preamplifiers at processing times down to approximately 50–100 nsec. JFETs, unlike bipolar transistors, lend themselves to cryogenic operation. JFETs are superior to MOSFETs in ionizing radiation resistance and less sensitive than bipolar transistors to neutron damage, which makes them suitable for operation in the strong radiation field around the interaction region of hadron colliders. They are also less prone to damage due to electrostatic discharge (ESD) into the gate, a feature which dramatically increases the reliability of front-end circuits in applications where carrier drift is achieved by means of an applied high voltage. The amplification factor $g_m r_{ds}$ defined as the product of the transconductance and the differential source to drain resistance is quite large, from several hundreds to about one thousand, making it possible to achieve high dc open loop gains in charge sensitive preamplifier. Diffused JFETs have a predictable noise and gain behavior, with minimal variations from different production batches, a proof of how well established the production technology is. Among the class of field effect devices they have the smallest amount of $1/f$ noise in the channel current. The spectral power density of the thermal noise is remarkably close to the theoretical dependence on the transconductance g_m [1].

Silicon Processing

The monolithic integrated preamplifier is going to be fabricated by INTERFET Corp., by means of an innovative process meant to solve a difficult problem of gate to gate isolation [2].

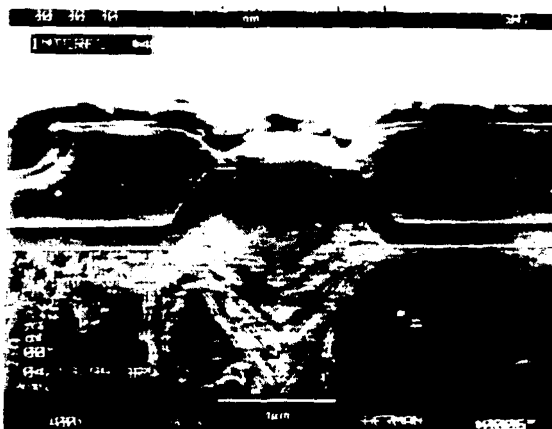

Figure 1: Cross section of a Dielectrically Isolated Wafer. The SEM picture (at ×2400 magnification) shows the region between two adjacent tubs. The n-epitaxial layer grows as polysilicon over the silicon oxide separating adjacent tubs.

The new technique will still allow the use of an epitaxially formed channel and a diffused gate, as in standard JFET processing. The epitaxially grown lattice is free of defects created by ion implantation which only in part can be annealed. Also, each doping polarity reversal requires greater and greater concentrations of compensating dopant element. Two or three such reversals are required for the ion implantation method while only one is necessary if an epitaxially grown channel is used.

A. Dielectric Isolation Method

A standard slice of the needed resistivity is first oxidized and then patterned through a photoresist process. The slice is then etched by means of an orientation dependent etching process to form "V" grooves which will achieve electrical insulation. Another layer of oxide is then applied followed by a polysilicon grow to fill the grooves and to build up a thickness comparable to the original wafer. The slice is then turned over and most of

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Table 1: Comparison of Discrete and Monolithic Diffused JFETs

	Short Channel		Long Channel	
W	11400 μm		400 μm	
L	5 μm		7 μm	
	Monolithic	**Discrete**	**Monolithic**	**Discrete**
I_{DSS} ($V_{DS}=5$ V)	54 mA	37 mA	1.7 mA	1.1 mA
V_T	−1.3 V	−1 V	−1.25 V	−1 V
g_m ($I_D=2$ mA, $V_{DS}=3$ V)	20.1 mS	21 mS	2.1 mS	1.6 mS
I_G	1 pA	1 pA	0.4 pA	0.2 pA
R_{ds} ($I_D=2$ mA, $V_{DS}=3$ V)	12 kΩ	60 kΩ	57 kΩ	65 kΩ
μ ($I_D=2$ mA, $V_{DS}=3$,V)	240	1260	120	105

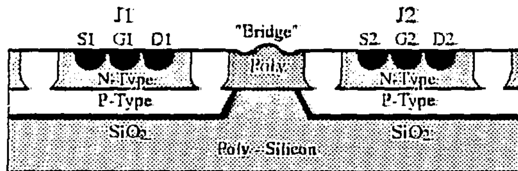

Figure 2: Dielectric Isolation Process.
Devices built in adjacent "tubs" are connected by back-to-back diodes in series with a high value resistor due to the polysilicon bridge shown in Fig. 1. If true isolation is needed, anisotropic etching can be employed to leave free standing "mesa" of silicon on a silicon dioxide floor. In this case only a single large tub is necessary.

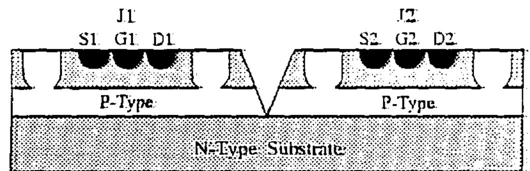

Figure 3: Double-epi, V-groove Process.
Two successive epitaxial layers of p and n type silicon are grown on top of an n-type substrate. Anisotropic etching is used to reach into the substrate, thereby separating the backside gates. Adjacent devices are connected by back-to-back diodes through the substrate.

the original silicon is lapped away until the tips of the V-grooves are exposed. This results in single crystal silicon islands ("tubs") isolated by silicon oxide and supported by a thick polysilicon substrate.

A single layer of n-type epitaxial silicon is grown over the dielectric isolation substrate and provides a uniform channel of controlled thickness for the JFET.

Figure 1 shows a cross section of a dielectrically isolated wafer in the region between two adjacent tubs. The epitaxial layer grows as doped polysilicon over the silicon oxide separating the tubs, thus connecting adjacent tubs. At this point several process options are possible.

i. *Planar Process*

If a standard planar process is used with multiple tubs, adjacent JFETs will be connected by back-to-back diodes and a high value resistor due to the polysilicon bridge like in Fig. 2. This should not cause isolation problems except perhaps increased noise in the input device.

ii. *"Mesa" Isolation*

If true isolation is needed, V-grooves can be etched to leave a free standing "mesa" of silicon on a silicon dioxide base. Metallization across this groove to connect devices on adjacent "mesas" degrades the yield, so it is better to use whenever it is possible the simpler planar process.

If grooves or mesas are necessary or if metallization over the grooves turns out to be a high yield step then there is no need to produce multiple dielectric isolation tubs. Multiple silicon mesas over a flat, large single tub can be used.

B. Double Epitaxy and V-Groove Isolation Method

This method utilizes an n-type silicon substrate on top of which a p-type layer for the back gate and an n-type layer for the channel are epitaxially grown. Next

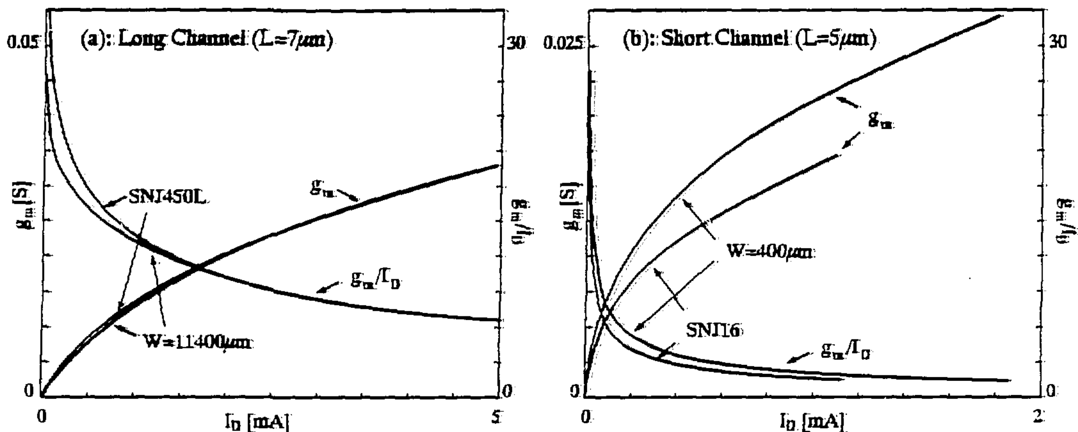

Figure 4: Comparison of Discrete and Monolithic JFETs. (a) Short channel devices, $L = 5\,\mu m$, $W = 11400\,\mu m$. (b) Long channel devices, $L = 7\,\mu m$, $W = 400\,\mu m$.

V-shaped grooves are etched deep enough to reach into the n-substrate thereby separating the backside gates, Fig. 3.

A true isolation is not achieved with this method since adjacent devices are connected by back-to-back diodes through the common substrate. Moreover, parasitic n–p–n transistors and p–n–p–n SCRs may cause latch-up problems under adverse conditions.

First Experimental Results

Up to the present only a preliminary silicon lot using the double epitaxial method has been manufactured, packaged and delivered. This first lot was manufactured on available material, which has a higher p-epi resistivity (about $1\,\Omega$cm, instead of the design value of about $0.01\,\Omega$cm). This increases the gate spreading resistance in series with the back gate, thus degrading the noise performance, a problem which will be corrected in the future production runs.

Figure 4(a) compares the g_m and g_m/I_D characteristics for a monolithic and discrete JFET of $W = 11400\,\mu m$ and drain to source spacing of $16\,\mu m$ (corresponding to an effective gate length of about $5\,\mu m$). At higher currents ($I_D > 1.5\,$mA) they are almost identical.

Figure 4(b) shows the same traces for long channel cycle device ($25\,\mu m$) corresponding to a gate length $L \simeq 7\,\mu m$) and for a gate width $W \simeq 400\,\mu m$. Also in this case they are very similar, with a slight superiority of the monolithic one.

Table 1 compares important dc parameters of monolithic and discrete devices. The only parameter which is somehow degraded is the output impedance, especially for short channel devices. This is a consequence of the low back gate doping and will be corrected in future runs.

Another parameter of key importance is the local matching of pinch-off voltage, V_T, over an area equivalent to the one of the preamplifier.

The median value of V_T is about $-1.3\,$V, within specification but higher than the nominal value of $-1\,$V, with an outstanding narrow spread of only $\pm 25\,$mV. The yield of this first lot, which uses V-groove trenches, is very high, so that tighter specifications can be set in the future.

Preamplifier Circuit and First Experimental Results

The charge sensitive preamplifier schematic is shown in Fig. 5 along with the channel widths W and is discussed in depth in Ref. [3].

The preamplifier consists of a cascode stage (J1 – J2) driving an active load made of J3 and J4. J7 serves the double purpose of bootstrapping the gate of J4 in order to allow the operation of J3 in the saturation region (V_{DS} for J3 is the sum of the V_{GS} of J4 and J7) and of buffering the high impedance point on the drain of J2. J9 is a large transistor and acts as an output driver. The signal feedback path includes J9 in order to improve the circuit non-linearity. The dc feedback is resistive through a voltage shifter made of eight series connected diodes to adjust properly the voltage level. A matched resistors voltage shifter will be explored in the future. In this first prototype both the feedback resistor and capacitor will be external components even though integrated high value resistors and capacitors have been built on a test portion of the chip. On the preliminary version, on double epi material the diode voltage shifter is not working properly, which prevents the operation of the preamplifier. An amplifier was nevertheless wired using test devices and an external diode voltage shifter.

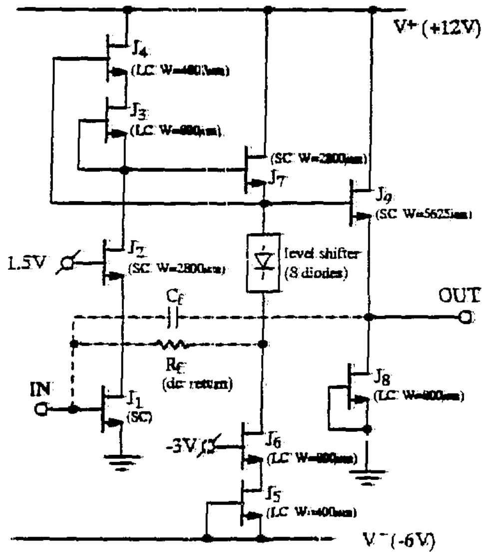

Figure 5: Circuit Schematic of the JFET Charge Sensitive Preamplifier. SC: devices with short channel, $L = 5\,\mu m$; LC: devices with long channel, $L = 7\,\mu m$. The input device J1 has a channel width $W = 11400\,\mu m$. The feedback resistor and capacitor (R_f and C_f) are shown connected with dotted lines since they are outside the monolithic chip.

Figure 6 shows the impulse response, normalized to the same displayed amplitude, for a 150 mV and a 1.5 V output pulse. A different rise time (40 nsec and 44 nsec, respectively) is evident, as predicted by the computer simulations and breadboard tests [3]. The noise performance has been evaluated and is consistent with the additional gate spreading resistance in series with the back gate due to the low *p*-epi doping.

Future Improvements

Test structures for the integration of high value feedback resistors ($R_F > 1\,M\Omega$) according to a scheme pioneered for the integration of front-end electronics on high resistivity silicon [4] and of the feedback capacitor have been included and will be evaluated.

As soon as a working version of the preamplifier is ready, it will undergo low temperature testing and evaluation of its resistance to neutron and ionizing radiation as well to electrostatic discharge. Test structures have been included to study the technology limits to achieve shorter channel lengths, which should improve the noise and speed performance of the circuit.

A systematic study of the optimum doping levels in the channel region is necessary for the development of a JFET with optimum noise performance near liquid argon temperature (90 K). In all alternative development,

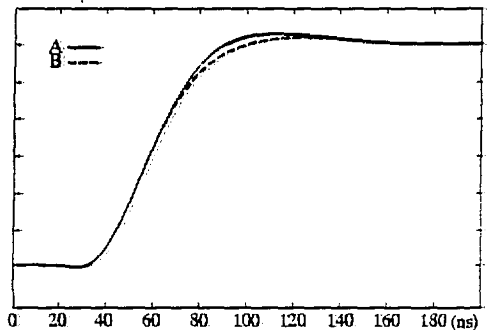

Figure 6: δ response of the charge sensitive preamplifier. Trace A: 25 mV/div; Trace B: 250 mV/div.

low thermal conductivity packages can improve the noise performance of the integrated circuit by raising its temperature by self heating.

A version of the circuit for transformer coupled systems will also be designed.

Conclusions

A preliminary run of a process capable of monolithic integration of JFETs has been evaluated. Performance, tolerances and matching of the devices are remarkably good, and the excess noise can be reduced in future runs. A preamplifier has been wired using monolithic JFETs and is working according to predictions. Full characterization of the different process options is being carried out. The preamplifier is intended for applications with ionization chamber calorimeters in the SSC environment at processing times of about 50 nsec.

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