Presented at the Sixth European Symposium on Semiconductor Detectors, Milan, Italy, Feb. 24-26, 1992

BNL--47525

DE92 015842

A NOVEL CHARGE SENSITIVE PREAMPLIFIER WITHOUT THE FEEDBACK RESISTOR(*)

Giuseppe BERTUCCIO[1], Pavel REHAK[2], Deming XI[2](o)

1) Politecnico di Milano, Dipartimento di Elettronica e Informazione, P.za Leonardo da Vinci 32, 20133 Milano, Italy (**)

2) Brookhaven National Laboratory, Upton, NY 11973, USA

Abstract

A novel charge sensitive preamplifier[3] which has no resistor in parallel with the feedback capacitor is presented. No external device or circuit is required to discharge the feedback capacitor. The detector leakage and signal current flows away through the gate of the first JFET which works with its gate to source junction slightly forward biased. The DC stabilization of the preamplifier is accomplished by an additional feedback loop, which permits to equalize the current flowing through the forward biased gate to source junction and the current coming from the detector. An equivalent noise charge of less than 20 electrons r.m.s. has been measured at room temperature by using an input JFET with a transconductance to gate capacitance ratio of 4 mS/5.4 pF .

INTRODUCTION

The charge sensitive preamplifier is generally used to amplify signals delivered by radiation and particle detectors. In the most simple configuration (figure 1) a resistor R_f is placed in parallel to the feedback capacitor C_f to continuously discharge it. The

---

(*) This manuscript has been autorized under contract number DE-AC02-76CH00016 with the U.S. Department of Energy. Accordingly, the U.S. Government retains a non exclusive, royalty-free licence to publish or reproduce the published form of this contribution, or allow others to do so, for U.S. Government purposes.

(o) Permanent Address: Institute of High Energy Physics, Beijing, China

(**) This research is also supported by Italian MPI, INFN and CNR.

(3) U.S. patent pending

feedback resistor also establishes a well-defined dc operating point to the amplifier itself. The detector's leakage current flows through R_f.

As far as the noise is concerned the feedback resistor introduces its thermal noise, which can be negligible in principle, compared with the shot noise of the leakage currents of the detector (I_d) and of the input JFET (I_F), if R_f is chosen to be:

$$R_f > \frac{2kT}{q(I_d + I_F)} \tag{1}$$

in which k, T and q are respectively the Boltzman constant, the temperature in Kelvin and the electron charge.

In some application, like the high resolution X-ray spectroscopy , the detector and the JFET are cooled in order to reduce the total leakage current down to $10^{-14}\ A$; the condition (1) would require a huge resistance value for R_f. But very high value physical resistor, in the range of several GΩ, present excess noise [1,2]. So, in this situation, R_f constitutes the main noise source limiting the maximum signal to noise ratio of the system. Another case where the feedback resistor presents difficulties is that one related to the Silicon Drift Detectors [3,5]. These detectors can operate also at room temperature with high energy resolution because of their extremely low output capacitance $(60\ fF)$ and low leakage current $(\approx 1\ nA/cm^2)$. These detectors need the integration of the first transistor of the preamplifier near their output electrode in order to avoid added stray capacitances. A feedback resistor of relatively high value (200 MΩ) is required to be integrated in a small silicon area, without introducing stray capacitances and excess leakage current. All these requirements are presently difficult to satisfy.

In both these cases removing R_f from the feedback loop is strictly necessary to achieve the lowest noise. But if R_f is taken away, a conventional CSP cannot work permanently because of the lack of a dc feedback path and the lack of a discharging path for the feedback capacitor C_f: the leakage current from the detector and the input JFET, together with the signal current from the detector, would charge C_f till the preamplifier reaches the saturation. In the past various solutions have been proposed in

order to have a CSP working without R_f: the optoelectronics feedback, the charge pump through the detector capacitance, the transistor pulsed feedback are some examples [6]. In all these solutions a comparator senses the preamplifier output voltage and when it exceeds a threshold value, a certain amount of charge is injected, with different methods, at the preamplifier input to discharge the feedback capacitor.

In this paper we present a charge sensitive preamplifier dc stabilized without the feedback resistor, this new configuration doesn't need any additional device and circuit for resetting.

PRINCIPLES OF OPERATION AND CIRCUIT ANALYSIS

The basic idea of the novel configuration of the CSP is to use the gate to channel junction of the input JFET as a path for the detector leakage current and for the discharge of the feedback capacitor.

Let's consider the charge sensitive preamplifier represented in figure 2. An n-channel JFET is employed and the detector is connected in such a way that its leakage current can flow through the gate to channel junction at the source end of the gate. A similar approach can be done by considering the detector connected in the reverse way and the preamplifier employing a p-channel input JFET.

In figure 3 the output characteristics of a commercial n-channel JFET are reported both when the gate to source junction is reverse or forward biased, showing the possibility for a JFET to work well also in that we can call the "forward bias mode".

Let's consider, figure 4, a conventional schematic configuration for a charge sensitive preamplifier in which the feedback resistor has been removed. T1, T2 and R constitute a cascode voltage amplifier, T3 is the voltage follower output stage. In this circuit the input JFET is forced to work in forward bias mode by the current coming from the detector and from that part of the gate-channel junction which is reverse biased. The voltage at the preamplifier input is a function of the current flowing through the gate to source diode: for current ranging from 1 pA to 1 nA the dc gate voltage of the tested

JFET varies approximately from 0.25 V to 0.45 V. The dc voltage gain of this amplifier is, in first approximation:

$$G_0 = \frac{v_o}{v_i} \cong -g_m R \tag{2}$$

where v_0 and v_i are the voltage signals at the output and the input respectively and g_m is the transconductance of T1. For typical values: $g_m = 4\ mS$ and $R = 1\ M\Omega$, it results $G_0 = -4000$, therefore, if the dc output voltage has a dynamic range of some volts, the input voltage dynamic range is limited to few millivolts. Even when no signal is present, this configuration without R_f is very critical to every variation of the detector leakage current, which can vary with the bias voltage, temperature, aging and radiation damage of the detector itself.

In order to employ the input JFET operating in the forward bias mode, the dc and low frequency gain of the preamplifier has to be lowered in order to increase the dynamic range of the dc input voltage up to some hundreds of millivolts.

The modificated configuration in figure 5 makes this effective. A second negative feedback loop has been introduced between the preamplifier output and the base of T2. This feedback increases the input resistance at the emitter of T2 to the value:

$$R_e \cong R\left(\frac{R_2}{R_2 + R_3}\right) \tag{3}$$

From a simple analysis it can be derived that the dc voltage gain of this preamplifier is reduced to:

$$G_0 \cong -g_m R_1 \left(1 + \frac{R_3}{R_2}\right) \tag{4}$$

with $g_m = 4\ mS$, $R_1 = 2.5\ K\Omega$, and $R_2 = R_3$ it results $G_0 = -20$, and the dynamic range of the input dc voltage is increased by two orders of magnitude.

In the frequency range of the signal charge delivered by detectors this preamplifier is similar to the conventional one. In fact the feedback loop in the second stage is not effective, due to C, so that the T2 transistor behaves as in the common base configuration, the main loop gain is high and all the charge will accumulate on C_f. The

discharge of C_f occurs through the gate-source junction of the input JFET. A detailed analysis of the circuit brings to the following transfer function:

$$\frac{v_0}{i} = \left(-\frac{1}{C_f}\right)\left\{\frac{s+\frac{1}{\tau}}{s^2 + s\left[\frac{1}{\tau}\left(\frac{\tau_2}{G_0\tau_1}+1\right)\right]+\frac{1}{G_0\,\tau\,\tau_1}}\right\} \tag{5}$$

where "i" is the input current, $\tau = \left(\frac{R_2 R_3}{R_2+R_3}\right)C$; $\tau_1 = R_g C_f$; $\tau_2 = R_g\left(C_f + C_T\right)$;

with R_g being the dynamic resistance of the gate to source junction and C_T is the total capacitance between the input and ground, which includes the detector and JFET capacitances.

Simple expressions of the time constant associated with the two poles can be derived assuming that these are strongly separated ($\tau_s << \tau_1$):

$$\tau_s = \tau\frac{G_0'}{G_0'-1} \qquad \textit{and} \qquad \tau_1 = R_g\left(C_f + C_T\right)\left(1-G_0'\right) \tag{6}$$

where $G_0' = G_0\,\frac{C_f}{C_f + C_T}$ is the dc loop gain when R_g tends to infinity.

The response to an input δ-current $i = Q\,\delta(t)$ is therefore:

$$v_0(t) = \left(-\frac{Q}{C_f}\right)\left(\frac{\tau_s\,\tau_1}{\tau_1-\tau_s}\right)\left[\frac{\tau-\tau_s}{\tau\,\tau_s}\,e^{-\frac{t}{\tau_s}} + \left(\frac{\tau_1-\tau}{\tau\,\tau_1}\right)e^{-\frac{t}{\tau_1}}\right] \tag{7}$$

so $v_0(0) = -\frac{Q}{C_f}$ and the output voltage decays exponentially with two time constant.

The shorter time constant τ_s can be chosen by the R_2, R_3 and C values, while the longer time constant τ_1 depends on the total capacitance at the input and on the value of R_g, which can be written as:

$$R_g = \frac{kT}{q\left(I_L + \bar{i}_s\right)} \tag{8}$$

where I_L is the leakage current of the detector and JFET and $\bar{i}_s$ is the mean value of the signal current from the detector, which can be expresses as:

$$\bar{i}_s = q\left(\frac{E}{\varepsilon}\right) f_s \tag{9}$$

where E is the energy deposited in the detector by the photon, ε is the mean energy to create a single signal charge in the detector and f_s is the photons rate.

As far as the noise is concerned the detector's current and the gate to source current (which have equal mean value) can be considered as two statistically independent components because of the capacitance C_T, so that the parallel current noise at the preamplifier input is due to the current $I_n = 2 I_L + \bar{i}_s$.

PREAMPLIFIER PERFORMANCE

The schematic of the preamplifier used for experimentation is shown in figure 6. It is a modified standard CSP with the resistor in the feedback loop [1]. With respect to the circuit of figure 5, an npn emitter follower output stage T4 is added in order to have a lower output impedance. A bootstrap of the load resistor of the cascode is performed by means of the capacitor C2. The current source T5 supplies all the circuit and guarantees an high load resistance at the emitter of T4. The input JFET is an INTERFET NJ 26 die glued on a teflon pc board, together with the feedback capacitor of 0.3 pF realized by two parallel metal strips.

With no detector connected, the input JFET works with the gate to source junction forward biased at a current equal to the reverse current of the gate-drain junction.

The gate voltage was measured by means of an electrometer resulting in V_{GS}=+105 mV confirming the forward bias mode condition.

A calibrated capacitor was used to inject a positive δ-like charge at the input. The response of the preamplifier is shown in figure 7, the risetime is less than 30 nS, the decay with two time constant is clearly visible. It has to be pointed out that the longer time constant decreases with the rate of unipolar injected charge, that is with the increasing of the mean signal current $\bar{i}_s$ as expresses by the (6) (8) and (9).

The equivalent noise charge (E.N.C.) was measured at room temperature by using a semi-gaussian shaper with shaping time ranging from 0.25 μs to 10 μs. The experimental E.N.C. as a function of the shaping time is shown in figure 8. The E.N.C. is a decreasing function of the shaping time because the parallel noise contribution does not dominate with respect to the other noise components. The minimum E.N.C. was measured to be 19.5 electrons r.m.s. at the maximum shaping time available of 10 μs. By means of a multiparameters minimum least square interpolation of the experimental data with the theoretical expression of E.N.C. [7], it's possible to separate the three component of the noise, as shown in the figure 8. The parallel white noise, in the present case with no detector connected at the preamplifier input, corresponds to the shot noise of a current of 1.5 pA, this is equivalent to the white thermal noise of a resistor of 30 GΩ with no excess noise. By knowing the transconductance $g_m = 4\ mS$ of the input FET, the total capacitance at the input was derived by the interpolating equation, resulting in $C_T = 5.7\ pF$. The coefficient of the $1/f$ noise [1] is $A_f = 1.1 \times 10^{-14}\ V^2$, this includes the contribution of the series $1/f$ noise of the input JFET and the contribution due to the dielectric losses at the preamplifier input. The E.N.C slope with respect to C_T is derived being 3 electrons r.m.s/pF at the fixed shaping time of 5 μs.

CONCLUSIONS

A novel configuration for the charge sensitive preamplifier, which is dc stabilized without the feedback resistor, has been presented. It has been shown that a junction field effect transistor can be drived by the detector leakage current, operating well with the gate-channel junction slightly forward biased at the source end of the gate. In the CSP this biasing mode for the input JFET can be exploited to remove the feedback resistor with a simple modification to the conventional configuration of the preamplifier itself. JFETs operating in the "forward bias mode" can be used also as source follower amplifying stage for integrated electronics on detectors.

Acknowledgements

We thank prof. E.Gatti for his helpful advises and for reviewing the analysis of the circuit, V.Radeka, H.Kraner, S.Rescia for stimulating discussions and for their support during the experiments, D.A.Pinelli for his careful collaboration in preparing the test structures, that greatly contributed to the success of the experiments, A.Pullia for the help in the analysis of the noise measurements. G.Bertuccio wants to thank V.Radeka for the hospitality at the Brookhaven National Laboratory during the performance of this work.

REFERENCES

[1] V. Radeka, *Proc. International Symposium on Nuclear Electronics*, Versailles, France (1968).

[2] F.S. Goulding, J. Walton and D.F. Malone, NIM 71 (1969), 273-279.

[3] P.Rehak, J.Walton, E.Gatti, A.Longoni, M.Sampietro, J.Kemmer, H.Dietl, P.Holl, R.Klanner, G.Lutz, A.Wylie, H.Becker, NIM A248 (1986), 367-378.

[4] V.Radeka, P.Rehak, S.Rescia, E.Gatti, A.Longoni, M.Sampietro, G.Bertuccio, P.Holl, L.Strueder and J.Kemmer, IEEE Electron Device Letters, Vol.10, No.2, (1989).

[5] G.Bertuccio, M.Sampietro, A.Fazzi, *Proc. 7th Inter. Workshop on Room Temperature Semiconductor X- and γ-Ray Detectors and Associated Electronics*, September 1991, Ravello (Italy). To be published on NIM.

[6] D.A. Lansing et al., IEEE Trans. Nucl. Sci., NS-18, No.1, 115-124, (1971).

[7] E.Gatti, P.F.Manfredi,M.Sampietro and V.Speziali, NIM A297 (1990), 467-478.

APPENDIX

In the circuit of figure 9 the block G represents the whole preamplifier of figure 5. C_d is the detector output capacitance. The gate impedance of the input JFET has been taken into account as the capacitance C_{in} in parallel with the resistance R_g. The currents balance at the input node brings to:

$$\frac{v_o}{i} = \frac{G}{1 + s R_g \left[C_T + C_f (1 - G)\right]} \tag{1a}$$

in which $C_T = C_d + C_{in}$ and $G = G(s) = v_o / v_i$ is the voltage gain of the preamplifier as function of the Laplace complex variable 's'.

In order to derive $G(s)$, in a first approximation, some assumptions has been accepted for the circuit of figure 5: 1) the capacitance existing in parallel to R is negletted, 2) the current gain β of T2 and T3 are high enough to neglect their base current, 3) $R >> R_1$.

Let's indicate with v_2 and i_2 the signal voltage and current at the T2 emitter, respectively. The voltage gain v_o / v_2 from the T2 emitter to the output is easily derived:

$$G_2 = \frac{v_o}{v_2} = \left(1 + \frac{R_3}{R_2}\right)\left(\frac{1 + s\tau}{1 + s\tau^*}\right) \tag{2}$$

in which $\tau = \frac{R_2 R_3}{R_2 + R_3} C$ and $\tau^* = \frac{\tau}{g_{m2} R}\left(1 + \frac{R_3}{R_2}\right)$, g_{m2} being the T2 transconductance.

the T2 emitter input impedance results $Z_2 = \frac{v_2}{i_2} = \frac{R}{G_2}$. So, the voltage gain of the whole preamplifier is:

$$G(s) = \frac{v_o}{v_i} = - g_m \left(\frac{R_1 Z_2}{R_1 + Z_2}\right) G_2 \tag{3a}$$

in which g_m is the transconductance of the input JFET and the factor multipling G_2 is the voltage gain v_2 / v_i. From the eq. (1a) (2a) and (3a) it follows the transfer function of the charge preamplifier as espressed by equation (5).

FIGURE CAPTIONS

Figure 1: Schematic of a conventional charge sensitive preamplifier with the high value resistor in the feedback loop. 'A' is a transresistance amplifier. The equivalent circuit of a detector connected to the preamplifier input is represented.

Figure 2: Charge sensitive preamplifier without the feedback resistor. The input JFET is forced to operate with the gate to channel junction forward biased at the source end of the gate. The leakage current,coming from the detector and from that part of the gate junction which is reverse biased, flows toward the source.

Figure 3: $I_D - V_{DS}$ characteristics of a commercial JFET. The gate-source voltage ranges from the forward bias of +0.4V to the reverse bias of -1.2V in 0.2V step. In the forward bias mode the gate current is indicated.

Figure 4: Circuital configuration of a conventional CSP. The feedback resistor has been removed. The detector is connected in such a way to permit its leakage current to flow into the gate-source junction of T1. This preamplifier cannot work permanently.

Figure 5: Circuital configuration of the novel CSP without the feedback resistor. A second feedback loop has been introduced between T3 and T2 transistors.

Figure 6: Schematics of the novel charge sensitive preamplifier without the feedback resistor.

Figure 7: Time response of the novel CSP to a δ-like charge injected at the input. The shorter time constant, emphasized in the insert, is due to the charge of C (figure 5) while the longer one is related to the discharge of the total input capacitance $C_T + C_f$ through the gate-source junction of the input JFET.

Figure 8: The equivalent noise charge of the novel CSP measured at room temperature with respect to the shaping time of a quasi-gaussian filter. The three components of the noise have been separated by means of a fitting of the experimental points with the theoretical ENC expression.

Figure 9: Schematic for the determination of the transfer function v_o/i of the preamplifier. The block G represent the circuit of figure 5.

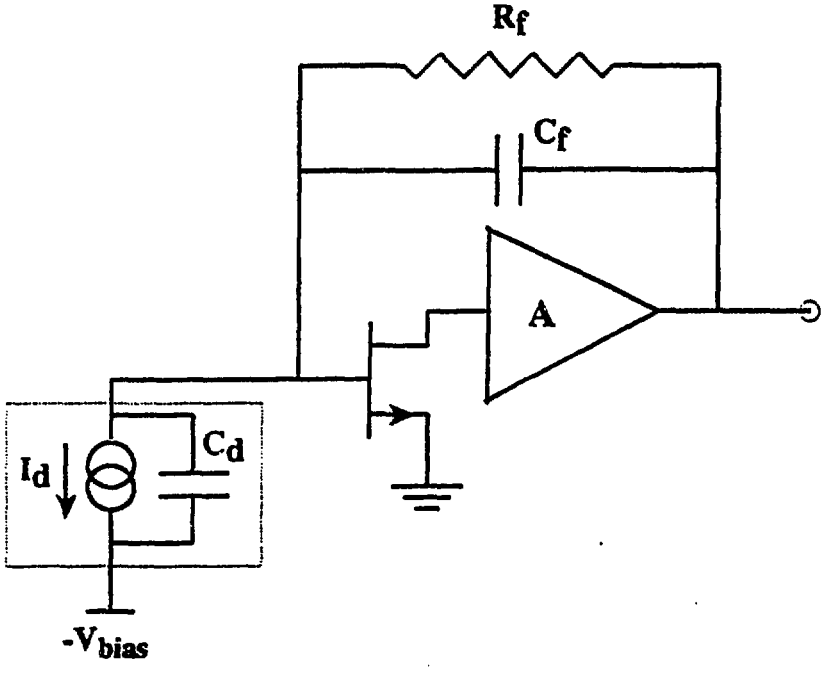

Figure 1

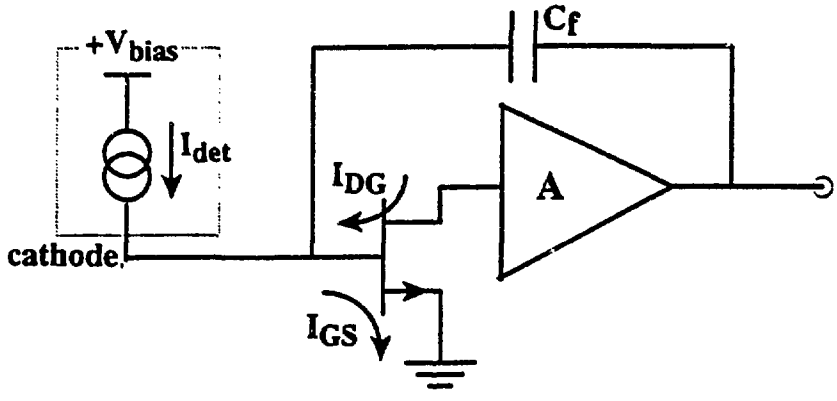

Figure 2

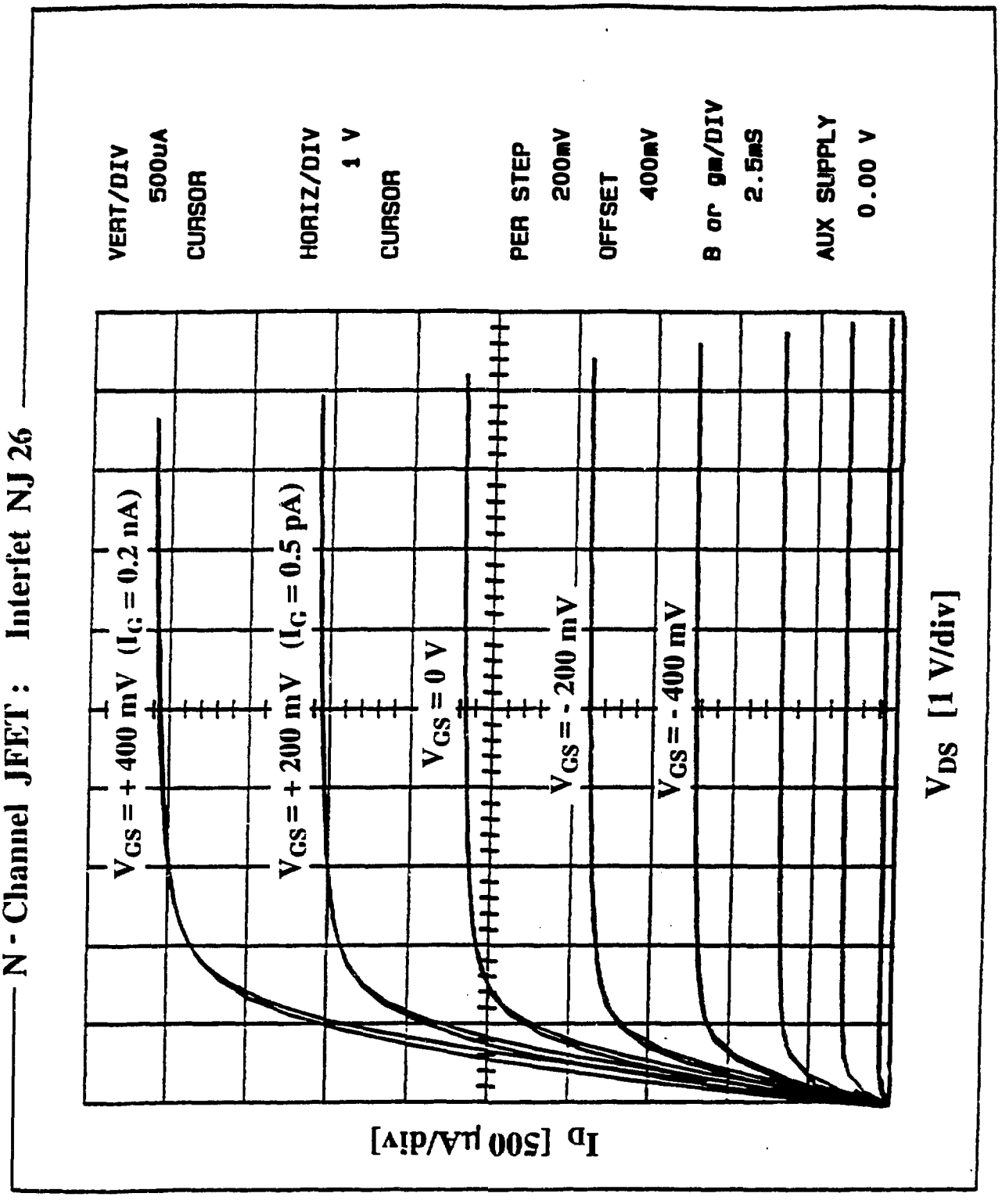
N - Channel JFET : Interfet NJ 26
VERT/DIV
500uA
CURSOR
HORIZ/DIV
1 V
CURSOR
PER STEP
200mV
OFFSET
400mV
B or gm/DIV
2.5mS
AUX SUPPLY
0.00 V
V_{GS} = + 400 mV (I_G = 0.2 nA)
V_{GS} = + 200 mV (I_G = 0.5 pA)
V_{GS} = 0 V
V_{GS} = - 200 mV
V_{GS} = - 400 mV
I_D [500 µA/div]
V_{DS} [1 V/div]

Figure 3

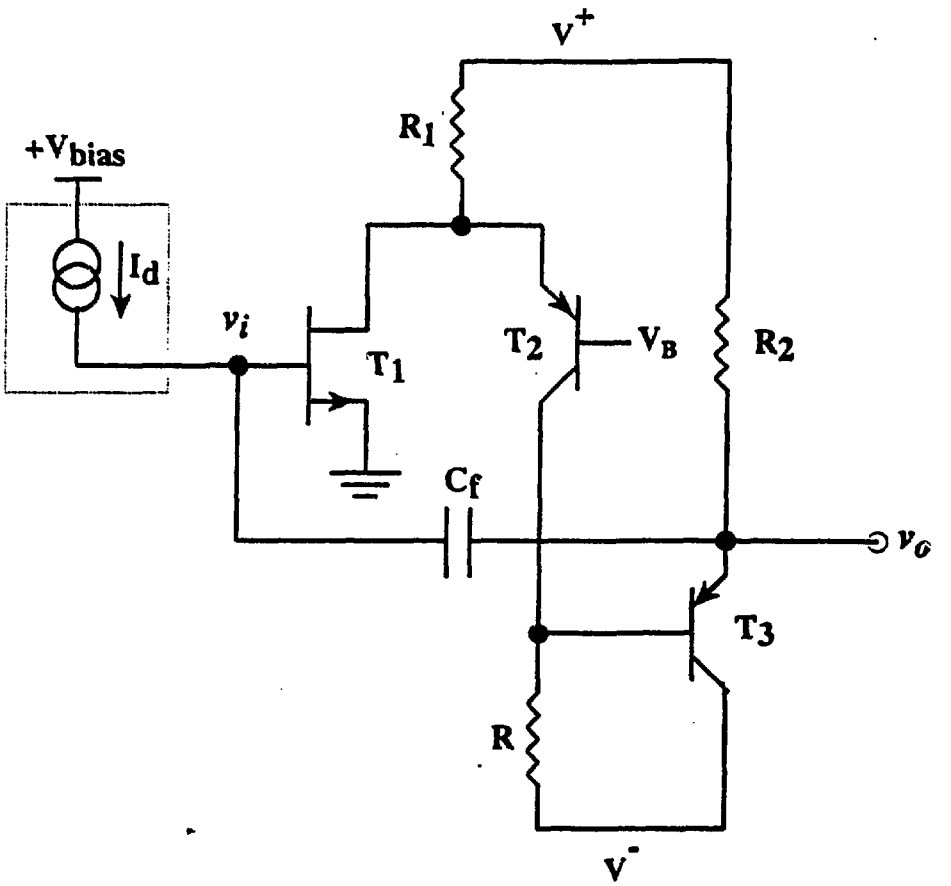

Figure 4

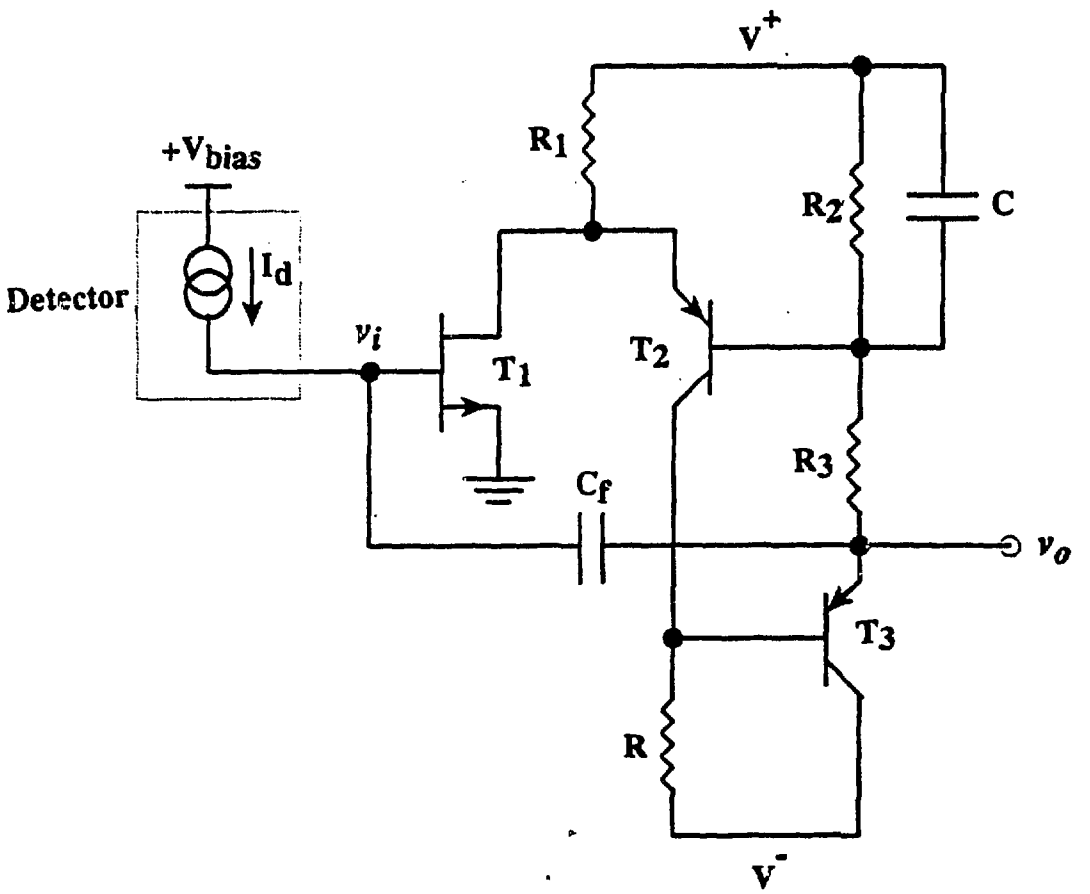

Figure 5

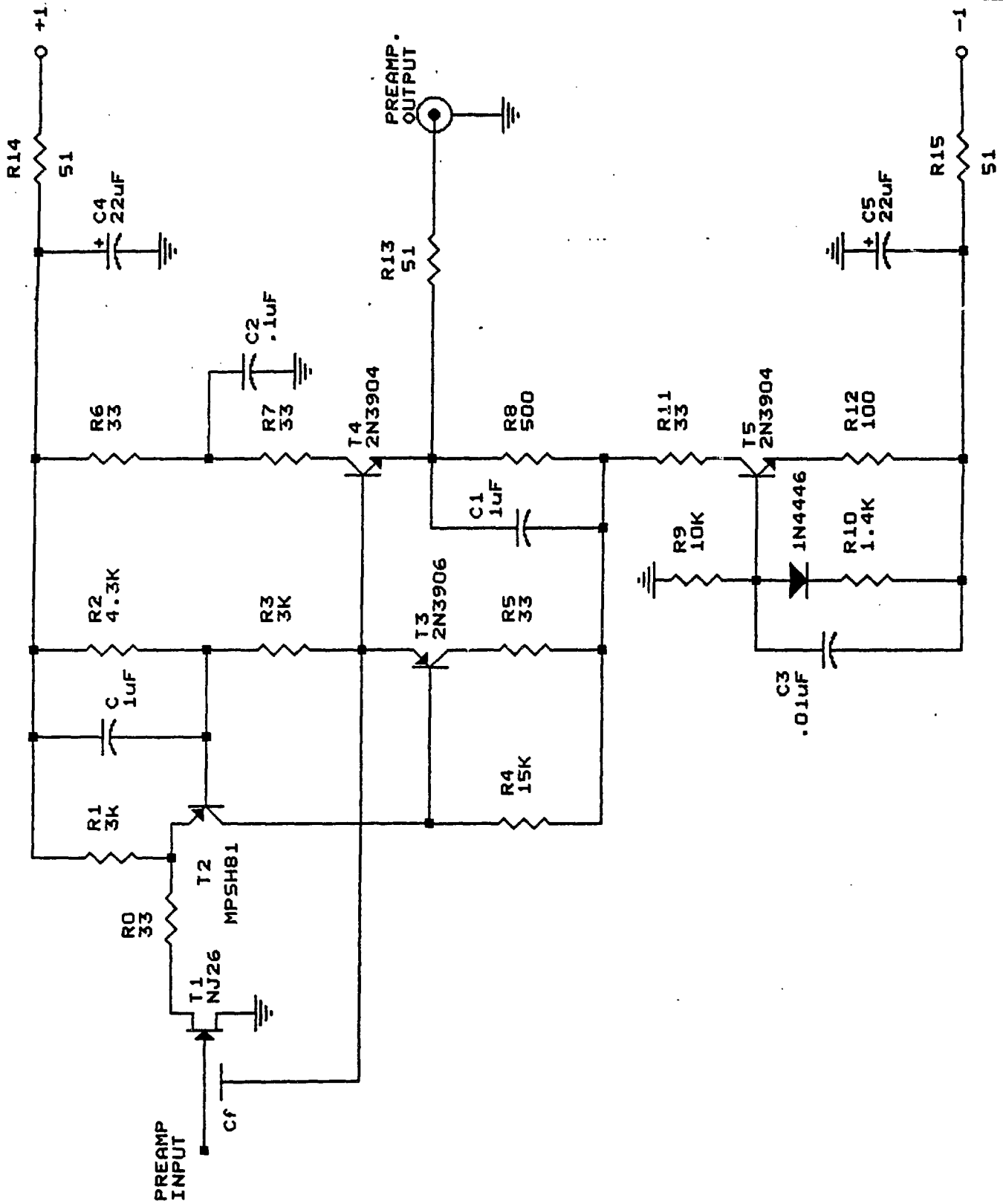
+1
-1
PREAMP. OUTPUT
R14 51
C4 22uF
R15 51
C5 22uF
R13 51
C2 .1uF
R6 33
R7 33
T4 2N3904
R8 500
R11 33
T5 2N3904
R12 100
C1 1uF
R9 10K
1N4446
R10 1.4K
R2 4.3K
R3 3K
T3 2N3906
R5 33
C 1uF
C3 .01uF
R4 15K
R1 3K
T2 MPSH81
R0 33
T1 NJ26
Cf
PREAMP INPUT

Figure 6

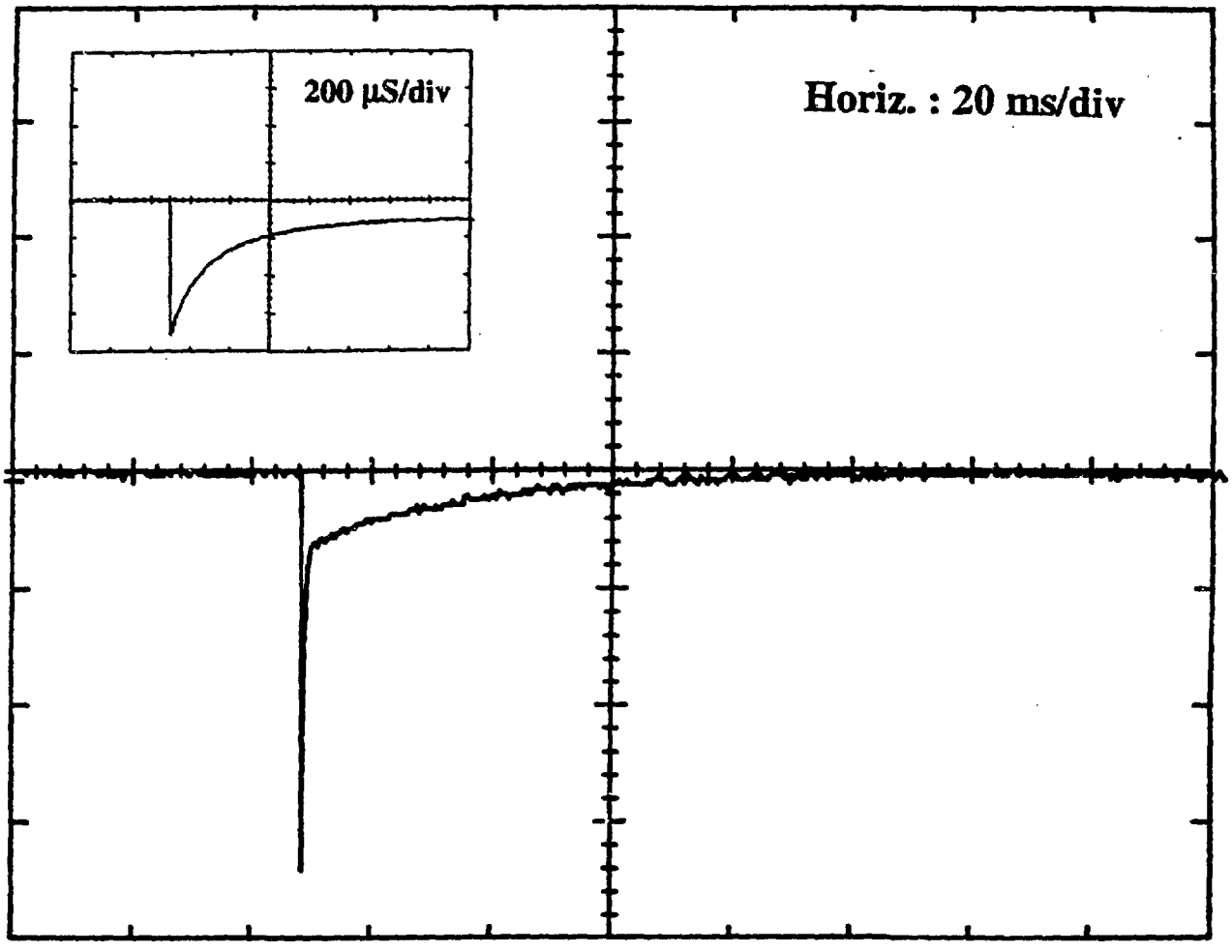

Figure 7

90
80
70
60
50
40
30
20
10
0
0
2
4
6
8
10
* : Experimental point
Fitting curve
JFET : NJ 26
C_T = 5.7 pF
T = 292 K
Series white noise
1/f noise components
Parallel white noise
E.N.C. [electrons r.m.s.]
Shaping Time [µs]

Figure 8

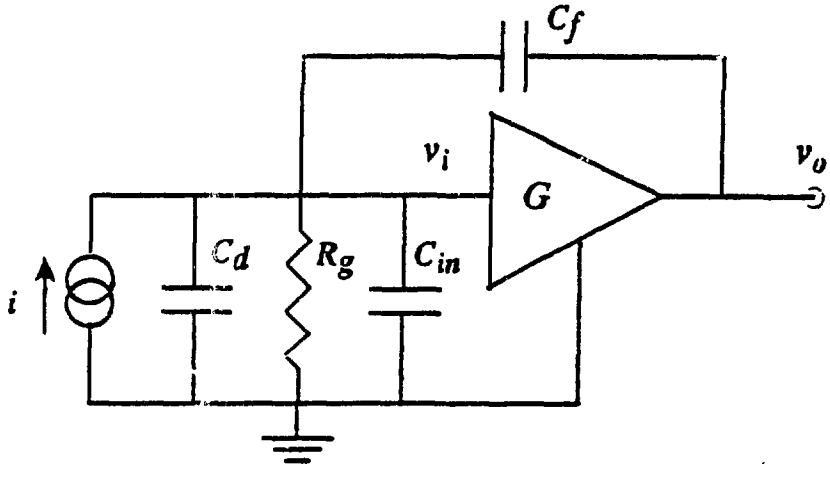

Figure 9