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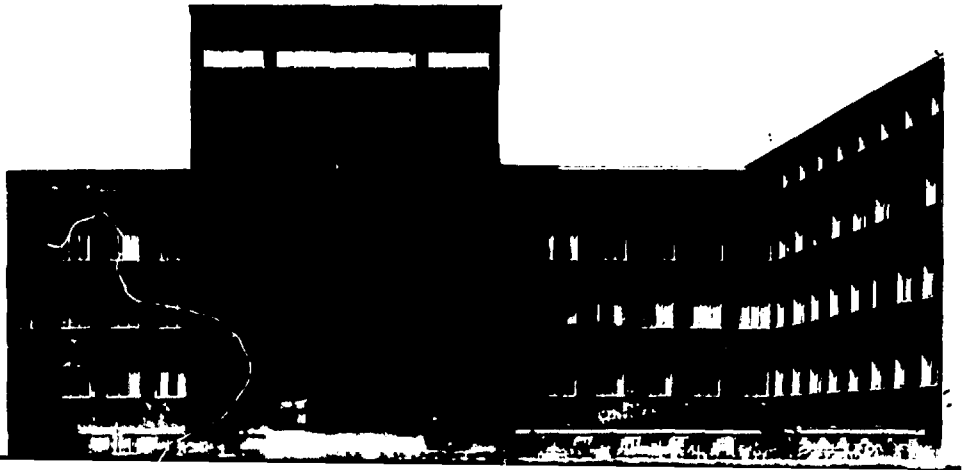

Electronic Ground Support Equipment for the Cluster Electric Field and Wave Experiment

Torleif A. Sten

Department of Physics
University of Oslo, P.O.Box 1048 Blindern
N-0316 Oslo 3, Norway

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Torleif A. Sten

Department of Physics

University of Oslo

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Introduction

The Cluster mission consists of a fleet of four identical spacecraft with the aim to study plasma structures in three dimensions. Cluster, together with SOHO, is a collaborative mission between the European Space Agency (ESA) and the U. S. National Aeronautical and Space Administration (NASA).
The launch is scheduled to take place at Kourou, French Guiana, in 1995.

The Electric Field and Wave (EFW) experiment, which is part of the Cluster Wave Experiment Consortium (WEC) is designed to measure the DC and AC electric field and density fluctuations by means of four spherical sensors, each deployed on a fifty meter wire boom.
This experiment is a result of collaboration between several research laboratories in Europe and in U.S.A., with the principal investigator at the Swedish Institute of Space Physics, Uppsala, (IRFU).

In order to perform comprehensive and time consuming tests and calibrations of the EFW experiment, a computer controlled electronic ground support equipment (EGSE) has been developed at the University of Oslo, Department of Physics, (UiO).
The basic design principles were outlined in cooperation with IRFU and the Space Science Laboratory, University of California, Berkeley, (UCB).

UiO is responsible for the production of three EGSE's and the control software development. This report deals with the hardware produced and assembled at UiO.

Contents

1. The EFW EGSE Overview.

The EFW EGSE mainly consists of three sub-systems as sketched in Fig.1 :
- The EFW stimuli rack.
- Four EFW plasma simulators.
- Associated computer and experiment interfaces for fully automatic control of the rack instrumentation and the plasma simulators. The description of this part of the system is limited to the general purpose interface bus (GPIB).

1.1. The EFW Stimuli Rack.

A Vero Imrak 1400 (116x68x60 cm) contains the following Hewlett Packard instrumentation:

- HP 37204 B, HP-IB Multibus Extender for connection of the internal rack bus to an external GPIB controller card via fiber-optical cables of 100 meters. The WEC stimuli PC and the EFW experiment PC will have GPIB-AT controller cards from National Instruments installed. A second HP 37204 B is normally located at the WEC stimuli PC.

- HP 3325 B, Synthesizer and Function Generator providing signals for most of the EFW test sequences.

- HP 8904 A, Multifunction Synthesizer with options 001 and 002, providing amplitude and phase modulated signals.

- HP 3478 A, Digital Multimeter to monitor the EFW stimuli box outputs.

The rest of the instrumentation, manufactured within the EFW team, consits of:

- The EFW Stimuli Box, a GPIB controlled link between the HP instruments and the EFW plasma simulators. Signals from a selected source are routed as inverted or non-inverted at unity gain, or at a gain of ten, to each plasma simulator.

- A +28 volts power supply to be used at the EFW bench test level.

- A Wideband Receiver attenuator driver for the WBD experiment (Univ. of Iowa) is driven from the GPIB and located in the EFW rack for practical reasons.

- The AC power section contains fixed installation. such as a mains isolation and noise suppression transformer of 690 watts, a dual automatic fuse/switch and two AC power outlets for connection of diagnostic equipment.

1.2. The EFW Plasma Simulators.

During some of the EFW test and calibration sequences, the spherical sensors will be partially deployed, and placed in the plasma simulator boxes.

The simulator box, basically a Faraday cage made of aluminium with a cladding of PVC, meassures 68 x 50 x 50 cm when fully mounted. It is formed by four hinged plates and two side walls, beeing folded when packed for transport.

A sphere support board, holds the EFW sensor in the center of the simulator box, and two wire drums are used to wind and hold the inner and outer stubs and guards.

One of the 1 mm holes in the EFW sphere connector assembly is used for connection of stimuli. A gold plated contact is pressed together, inserted in one of the holes, and released.

Stimuli is applied via a thin flying wire from the R/C network in the electronics box connected to the EFW stimuli box for remote selection of the following functions :

- Plasma simulator (Faraday cage) driven by the stimuli source, or connected to signal ground.
- One of the impedances: 100 M ohm, 5 M ohm with 11 pF in parallell, 10 K ohm or 5.6 pF.

2. The EFW Stimuli Box.

A main task of the stimuli box is to let a software program run fully automatic test sequences by:
- Selecting a signal source via the input module.
- Routing the signals via the output module to each of the plasma simulators.

The stimuli box is a listen only device, in accordance with the IEEE-488 protocol, running on a General Purpose Interface Bus, (GPIB). The GPIB address is fixed to 13 (decimal).

For information on the stimuli box performance see the U_O internal reports:
- Noise and frequency spectra of the CLUSTER EFW stimuli box and plasma simulators. (T. A. Sten, May 1992).
- Calibration of the CLUSTER EFW stimuli box. (T. A. Sten, March 1992).

2.1. The Stimuli Box Overview. Fig.2.

The GPIB interface and control logic has three functions:
- The GPIB interface with handshake and listen functions.
- The relay control logic, decoding the GPIB data for setting of the relay states throughout the system.
- A programmable timer to set up the duty cyle and frequency of an internal square wave stimuli source.

The input module is used for selection of an external signal source, HP generators, or the internal:
- Precision sine referenc of 500 Hz with amplitudes of 1 or 10 volts.
- Square wave of 100, 10 or 1 Hz, with symmetrical outputs of 5, 1 and 0.01 volts peak to peak.

The signals are passed on to the output module non-inverted (Ax1) and inverted (Bx1).

The output module is used for routing of stimuli to each of the plasma simulators, at unity gain (Ax1, Bx1) or at a gain of ten (Ax10, Bx10). It has two BNC connectors, one for monitoring of the stimuli outputs with a digital multimeter (DMM). The other one (Phase Inp.) may be used to connect a phase controlled signal from option 002 in HP 8904A.

A function panel is depicting, by means of graphic symbols, the main functions of the stimuli box, and indicating by light emitting diodes, the current mode of operation.

The power section has one tri-volt supply with isolated outputs for all the digital circiuts, and the analog circuitry in the input module.
Two power supplies (+/- 115 volts) are used for the high voltage amplifiers in the output module. These supplies are turned on by a solid state relay (SSR) whenever the Ax10 or Bx10 mode is requested during a test sequence.

2.2. The Power Section (Fig.3)

In general, none of the output return lines are conneted to the card frame. It is quite essential to connect the external ground reference to the stimuli box signal ground, one of the BNC connectors before starting any measurements.
Coax cables, marked with yellow tape and with the center pin removed, are provided for this purpose.

Two 20 mm fuses, 2A/250 slow, are located on a rear panel close to the mains connector and filter, Belling Lee L2133C/L.

A lineary regulated tri-volt supply (Vero LK 35) was selected to save volume in the card frame. It has galvanic isolated outputs of:

5 V / 3 A, floating with respect to any other output lines, driving the digital circuits and the relays.

+/- 15 V / 0,65 A for the analog circuits in the input module.

Note: This unit has one internal 20 mm fuse, 1.25A/250V.
To access the fuse:
- Remove left side cover, four screws.
- Remove lower left screw near the connector.
- Carefully bend the bottom plate to access the fuse holder.

Two identical switch-mode supplies (Schafer C297 H), working at 30 KHz, are used to power the high voltage amplifiers in the output module. The output voltages are preset to 115 volts.
Viewed from the rear of the card frame, the right connector is wired to provide the positive voltage.

Each output is filtered with one toroid choke of 2 x 27 mH (Siemens), a 10 uF/ 160V electrolyttic and a 0.33 uF/ 500V ceramic capacitor. The ripple is 100 mV peak to peak at normal load. Both filters are located close to the power connectors.

Note: Each unit has one 20 mm. fuse, 2A/250V slow blow, located near the connector.

The AC input to the 115 V supplies is switched, either by a software controlled solid state AC relay (SSR), Teledyne type 601-2, or a rocker switch "100 /" at the function panel.

Note that this switch overrides the SSR and should normally be left in OFF position. The SSR is conducting whenever K5 or K7 in the output module are energized, i.e. when any of the two amplifiers (Ax10, Bx10) is requested. Driver logic for control of the SSR is implemented in U1 (EP310) at the function panel.

Two switches for the AC line seem redundant. The idea is, however, to enable a check of the noise contribution from the high voltage supplies in the unity gain mode (Ax1, Bx1).

2.3. GPIB Interface and Control Logic.

A description of the circuitry falls naturally into three parts, namely the GPIB interface, the programmable timer and the relay control logic. The schematic drawing is given in Fig.4 and the component layout in Fig.5.

Most of the logic functions have been implemented in Altera's erasable programmable logic devices (EPLD), see section 5 for the design files describing the logic equations in question.

2.3.1. The GPIB Interface is connected to the IEEE-488 bus via inverting Schmitt Triggers U1 and U2 (HCT14) providing positive logic levels at the internal bus and handshake lines. A TTL driver U4 (SN75160A) is used for the Not Ready For Data (NRFD) and No Data ACcepted (NDAC) lines, being negative true.
The eight data lines D0-D7 are terminated with 3,2 k pull up resistors to +5 volts and with 6,8 k pull down resistors to the digital (GPIB) ground. For each of the control lines, the 6,8 k pull down resistors are connected to the dedicated GPIB return lines.

Communication on the GPIB is established through a handshake function and a listen function. In the following, a "message" will affect the GPIB interface only, whilst "data" affect the "device", in this case the timer and relay control logic.
The "controller" is assumed to be a GPIB interface card located in a PC. The clock frequency is 4.160 MHz.

The Acceptor Handshake (AH) Function implemented in U6 (EPS 448) ensures that:
- The Listener in U5 is ready to accept a message.
- Message on the bus is valid.
- A message has been accepted by the Listener.
- Data on bus is valid and then provides a strobe pulse RXSTR for one periode of the clock (CP).
- The controller is informed, by setting the NRFD and NDAC lines. Note that these outputs are true at LOW levels.

An Inte.Face Clear (IFC) must be received at the NRESR input of U6 (EPS448) to initiate the programmable sequencer.
The "stimuli box ready" input (RXRDY), is sensed by the AH-function and the Listen-function. RXRDY is, however, wired to VCC because the data will be safely transfered within one CP.

The Listener (L) Function implemented in U5 (EP610) will decode controller messages such as:
- MLA, my listen address.
- UNL, unlisten all current listeners.
- DCL, device clear for all connected devices.
- MTA, my talk address unlisten the stimulibox only.
- SDC, selected device clear the stimulibox only.
- IFC, interface clear.

The L-function is basically a clocked (CP) Set'Reset flip-flop with a clear- input, and the output (LAC) is set high when the Listener is in an ACtive state.

It operates as follows:

- Controller sends IFC, and the f-f is cleared if power on (pon) is true.
- When the controller wants to address the stimuli box; it places the address on GPIB and sends attention (ATN) true, communicates with AH, and send a data valid (DAV) true. The f-f Set-input is simply controlled by the product term:

ATN & DAV & MLA.

- When the controller wants to unlisten the stimuli box; it will send ATN and DAV as above, followed by UNL or a MTA code.
  The f-f Reset- input is controlled by:

ATN & DAV & UNL + (or) ATN & DVA & MTA.

The Device Clear Function affects the stimuli box electronics only, and no other interface functions, being cleared by IFC.

- Controller may clear, or reset to a pre-defined state, the stimuli box electronics by sending *DCL* or *SDC*. Both codes will cause a high level at the output buffer DCL of U5, which has two product terms at the input:

ATN & ACD & SDC & LAC + ATN & ACD & DCLR

Where: SDC and DCLR are product terms being true when the GPIB command codes SDC and DCL are detected respectively.
LAC is true when the Listener is in an Active State.
ACD is true when the AH function is in Active Data State.

2.3.2. The Relay Control Logic

Some types of GPIB interface cards do not quite distinguish between data and messages. Bytes such as 0A (line feed) and 0D (carriage return) tend to be misinterpreted. For that reason, all bytes with a leading zero, the "0" nibble (SEL0) has been omitted in this design.

When the stimuli box is addressed, and a valid data byte (D7-D0) is present on the internal bus:

D7-D5: Form an address for the 3-to-8 line decoder functions in U5 and U7 (EP 610) with the SEL3 and SEL2,1,0 outputs connected to the latch enable inputs of U11 to U13 (HCT 259, 8-bit addressable latches)

D4: Is used for GPIB addressing only.

D3: Holds the data bit to be latched.

D2-D0: Is used to select one of the latches within a HCT 259.

All the HCT 259 outputs remain unchanged until the positive going pulse (RXSTR) from the AH-function in U6 (EPS 448) will:

- Take one of the SEL outputs low.
- Enable the the selected HCT 259.
- Set the selected latch-output to the level of D3.

The relay control lines for the plasma simulators are buffered by U16-U18 (HCT 4050). Most of the relay control lines from U13 are decoded in U15 (EP 310) to drive function panel LED's.

2.3.3. The Timer Control Logic essentially consists of the programmable timer U8 (82C54) and six clocked D-type latches implemented in U7 (EP 610). It is used to set up the frequency and duty cycle of a pulse train (PULSE) to the programmable attenuator in the input module.
When a valid data-byte (D7-D0) is present on the bus:

D3-D0: Form a data nibble; representing the least significant nibble when written directly to U8, and the most significant nibble when latched into U7.

D7-D5: Form an address for the "3-to-8 line" functions in U7 where the output SEL6 is a write command for U8. SEL4 and SEL5 are used inside U7 to latch the most significant nibble D7-D5, and the address bits A0, A1.

A sequence for setting up the timer may look like:

- Latch the address bits A0 = 1, A1 = 1 to state that a control word will follow.
- For each counter, latch the most significant nibble of the control word into U7.
- Place the least significant nibble of it on the bus, and write a full control word to U8.
- For each counter, latch the appropriate address A0, A1 to state that data-bytes follow.
- For each counter latch data, least significant byte first.

If necessary, see the software commands in section 3.3 for a more complete description of the timer.

The time. output from U8 is buffered by U14 (HC4049) driving an optocoupler at the input module. A serial resistor of 3.3K is used to reduce radiation of noise from the PULSE wiring.

K15 and K16 from U13, controlling the pulse attenuator, are buffered by U17 (HC4050) to drive the optocouplers at the input module.

2.4. The Function Panel.

The main functions of the stimuli box is depicted on this panel by means of graphic symbols and text. Light emitting diodes in different colours show the current state of the stimuli box such as:

- Listener addressed.
- Selected stimuli source at the input module.
- Gain setting of the high voltage amplifiers.
- Connection of input to the digital multimeter.
- Phase input or GND selected at the output module.
- Routing of stimuli to each plasma simulator.
- Indicating if a plasma simulator is driven or grounded.

One of the grapich symbols, the A amplifier, is somewhat misleading. In the Ax1 mode, there is no buffer amplifier between the external signal sources and the loads. See K5 in Fig.10.

The circuitry is straight forward and need no comments exept for U3 (EP310) which is described in section 5.5. A schematic drawing is given in Fig. 6 and the component layout in Fig. 7.

2.5. The Input Module.

A schematic drawing is given in Fig.8 and the component layout in Fig.9. This unit is described in three blocks:
- The inverting buffer (Bx1).
- The sine reference generator.
- The pulse attenuator.

The inverting buffer Bx1 U1 (AD846BQ)is a transimpedance amplifier, capable of driving a rather heavy load, represented by the four 15 m plasma simulator cables. A combination of the feedback resistor value of R2 = 1,5 K, and the compensation capacitor C5 = 22 pF, preserve stablity and bandwidth.

The non-inverting buffer U8 (AD846 BQ) is used to unload the outputs from the pulse attenuator and the sine reference.
An +Input bias current in the order of 20 uA restricts the non-inverting applications to low impedance signal sources. An operational amplifier U9 (OP27) is used to buffer the voltage dividers in front of K14.

The sine reference generator U10 (ThC SWR 200, Thaler) is set to a frequency of 500 Hz by C21 = C22 = 20 nF. K14 is used to select the "Sine Ref." 10V or 1V peak amplitudes.

The pulse attenuator.

Briefly, this circuitry consists of a digital to analog converter U7 (DAC80Z-CBI-V) with groups of the input bits connected to U6 (EP310), an EPLD which is driven by the GPIB relay control logic.
The optocouplers U3,4 and 5 (HCPL 2201) provide the following digital inputs:

PULSE: For frequency and polarity of a square wave, with output symmetrically to ground.

K15, K16: For setting one of the fixed output voltages:

A = K15' & K16' 5 V.
B = K15' & K16 1 V.
C = K15 & K16' 10 mV.

In the following, please note carefully that:

- Bit 1 is the most significant bit (MSB), the sign bit.
- Bit 12 is the least significant bit, 1,22 mV.

Actual bit patterns for U7 is given by:

Bit: 1	2	3	4	5	6	7	8	9	10	11	12	Amplitude:
0	0	0	0	0	0	0	0	0	0	0	0	+ 2,4988 V
1	1	1	1	1	1	1	1	1	1	1	0	- 2,4988 V
0	1	1	0	0	1	1	0	1	0	0	0	+ 0,496 V
1	0	0	1	1	0	0	1	0	1	1	1	- 0,496 V
0	1	1	1	1	1	1	1	1	0	1	1	+ 4,89 m'
1	0	0	0	0	0	0	0	0	1	0	0	- 4,88 mV

where bit 1 is driven by PULSE.

Some of the identical, vertical bit patterns are grouped as:

B2 = bit 2 and 3.
B3 = bit 4, 5 and 8.
B4 = bit 6 and 7.

The other patterns, even if identical, are treated bit-wise to preserve some flexibility.
For information on the logic implemented in U6, please see the Boolean equations in section 5.6.

Due to the conversion time of 3 uS in U6, this kind of pulse generators certainly have very limited applications. In this case, however, the actual frequency range is 1 to 100 Hz, and stability of the pulse amplitude is considered more important that the shape of it.
To improve the pulse-shape somewhat, R9 is used to drop and filter the + 15 V line.

2.6. The Output Module.

This plug-in unit holds two printed circuit boards; one for all the relays, the other for the two Ax10 and Bx10 amplifiers. See Fig.10 for a schematic drawing. Layout of the components is shown in Fig.11 for the relay card and in Fig.12 for the amplifier card.

The main criteria for selecting the PA85A amplifiers were a requested output swing of +/- 85 volts, low offset voltage and driving capability for the plasma simulator cables.

A feedback resistor of 10 K was selected for stable operation and a moderate power dissipation in the network. Compensation capacitors of 47 pF (C3, C8) limit the power band-width to approximately 50 kHz. Resistors of 33 ohms (R9, R17) limit the output current to 40 mA.

With a quiescent current of 20 mA and a supply voltage of +/- 115 volts, each amplifier dissipates 4 watts. In addition, each amplifier consume 1,3 watts when the output swing is +,- 85 V and the feedback resistor of 10K is the only load.

The amplifiers are mounted with heatsinks (Apex HS01) at the rear panel of the plug-in unit. At an output swing of 100 volts peak-to-peak, the case temperature of PA85A is measured to max. 45 C.

Resistors of 68 ohm (R1 to R4) are added to preserve the wave forms, i.e. the zero-crossing edges at the plasma simulator end of the cables. This is especially significant when driving the cables at Ax1, directly from the HP generators.

2.7. The Mechanical Design.

The mechanical construction is based on a Vero KM6-II universal subrack system 3U x 84HP, 240 mm. deep, divided into two shielded halfs. Standard plug-in units for the power section and the GPIB interface unit are inserted from the rear, occupying the left portion of the card frame. The function panel covers the front of this section. Two plug-in units in the right section, the input and output modules, are accessed from the front.

A clamp, for support for the rather heavy cables to the plasma simulators is fastened to the rack at the right side of the EFW stimuli box.

Some of the front panels have been made of 2 mm. Copyllot anodized photoaluminium sheets with text and symbols in CopyColours blue Pc45 and orange Pc41.

All the electro mechanical relays are Teledyne type 13 JC-5, dobbel pole - dobbel throw (DPDT) with an internal CMOS driver and a suppressing diode. In all the drawings, the driver inputs are symbolized by coils, activated by a positive true (+ 5 V) level. The relays are shown in a de-energized state.

High performance film resistors +/- 1% (Caddock, MK 632) have been used for the amplifier feed-back circuitry and the voltage dividers. Load life: 1000 hrs. at 0.75 W, 125 C with delta R = +/- 0.4 % max. Temperature coefficient: 50 ppm/C.

3. Software Control.

A rather simple program was written in Microsoft Quick C to test and de-bug the stimuli box. The NI-448 MS-DOS software (C) package from National Instruments is used to communicate with and control the devices connected to the GPIB.

Software commands, hex bytes preceded by backslash and x, are listed below for the relay, timer and stimuli box functions.

Please recall that the GPIB address of the EFW stimuli box is 13 (decimal), and that an Interface Clear message (IFC) must be issued at the beginning of the of the program.

A typical command string, for selection of the Synth,/F.gen at the input module, may look like:

```
ibwrt(bd,\x68\x61,2);
```

Where:

- bd specifies the stim. box address
- \x68 turns relay K10 on
- \x61 turns relay K11 off
- 2 number of bytes.

The most significant nibble of the hex byte is related to the 3-to-8 line decoder functions (SEL) in Fig. 4, addressed by GPIB lines D7, D6 and D5. Output "0" is omitted to avoid the \x0A (line feed) and the \x0B (carriage return), misinterpreted by some GPIB interface cards.

Note that the commands described in the following TURN OFF all relays not being used in order to reduce power and noise.

3.1. The Input Module.

Relay:	K10	K11	K12	K13	K14	K15	K16
OFF	60	61	62	63	64	65	66
ON	68	69	6A	6B	6C	6D	6E

Command strings:

	Synth. /F.gen	MultiF Synth	Sine 10V	Sine 1V	Pulse 5V	Pulse 1V	Pulse .01V	GND
K10	60	68	68	68	68	68	68	68
K11	61	61	69	69	69	69	69	69
K12	62	62	6A	6A	6A	6A	6A	62
K13	63	63	63	6B	63	63	63	63
K14	64	64	6C	64	64	64	64	64
K15	65	65	65	65	6D	6D	65	65
K16	66	66	66	66	6E	66	66	66

When Sine 10V is selected be sure that the high voltage amplifiers are set to unity gain Ax1 and Bx1.

3.2. The Output Module.

The Ax10 and Bx10 outputs must be considered carefully when writing software commands for setting of the amplitudes in the external function generators.

Until further notice the amplitude must be limited to 65 volt in order to protect the EFW experiment.

Relay:	K1	K2	K3	K4	K5	K6	K7	K8	K17
OFF	E0	E1	E3	E2	E7	E5	E6	E4	67
ON	E8	E9	EB	EA	EF	ED	EE	EC	6F

Amplifier gain settings:

	Ax1	Ax10	Bx1	Bx10
K5	E7	EF	x	x
K6	x	x	E5	E5
K7	x	x	E6	EE
K8	x	x	E4	E4

Digital Multi Meter:

DMM:	to A	to B
K17	67	6F

Line B connections to:

	Phase Input	GND	
K7	E6	E6	(Set Bx1)
K6	ED	ED	
K8	E4	EC	

Routing of stimuli output.

To connector:	P1	P2	P3	P4	
Plasma sim.:	1	2	3	4	
From line A:	E0	E1	E3	E2	(Ax1 or Ax10)
From line B:	E8	E9	EB	EA	(Bx1, Bx10, Phase Inp. or GND)

3.3. Timer Set Up.

The hex bytes below set the counters to provide a 1 Hz signal from an input of 8 KHz.

Control word	Counter data bytes		
\xA3\x83\xC6	\xA0\x89\xC0	\xA0\x80\xC1	Counter 0
\xA3\x87\xC6	\xA1\x83\xCC	\xA1\x80\xC9	Counter 1

The control word, always preceded by A3, specifies that least significant bytes are written first (83, 87). Both counters are set to 16-bits binary, operating in mode 3 (C6).

The data bytes, the least significant first, are preceded by the counter address (A0,A1) are organized as:

\x8... and the most significant nibble.

\xC... and the least significant nibble.

3.4. The Plasma Simulators.

Each plasma simulator has four relays K1, K2, K3 and K4 for switching of the R/C networks and the box potential, see section 4. In the default, or initial state, the simulator box is driven and the 100 M resistor connected to the sphere

Plasma Simulator No.1 (P1):

Relay:	K1	K2	K3	K4
OFF	40	41	42	43
ON	48	49	4A	4B

	100M	5M	10K	5pF	Box driven	Box grounded
K1	40	40	48	48	x	x
K2	41	49	41	41	x	x
K3	42	42	42	4A	x	x
K4	x	x	x	x	43	4B

Plasma Simulator No.2 (P2):

Relay:	K1	K2	K3	K4
OFF	44	45	46	47
ON	4C	4D	4E	4F

	100M	5M	10K	5pF	Box driven	Box grounded
K1	44	44	4C	4C	x	x
K2	45	4D	4D	45	x	x
K3	46	46	46	4E	x	x
K4	x	x	x	x	47	4F

Plasma Simulator No.3 (P3):

Relay:	K1	K2	K3	K4
OFF	20	21	22	23
ON	28	29	2A	2B

	100M	5M	10K	5pF	Box driven	Box grounded
K1	20	20	28	28	x	x
K2	21	29	21	21	x	x
K3	22	22	22	2A	x	x
K4	x	x	x	x	23	2B

Plasma Simulator No.4 (P4):

Relay:	K1	K2	K3	K4
OFF	24	25	26	27
ON	2C	2D	2E	2F

	100M	5M	10K	5pF	Box driven	Box grounded
K1	24	24	2C	2C	x	x
K2	25	2D	25	25	x	x
K3	26	26	26	2E	x	x
K4	x	x	x	x	27	2F

4. The EFW Plasma Simulator.

During the EFW tests at bench-level, and calibration at the spacecraft level, the spherical sensors with stubs and guards will be located inside the plasma simulator box, see Fig.13.
The sphere is placed on a support board (F), and connected to the relays and R/C networks in box (G) by a thin wire.

4.1. The plasma simulator box (Fig.13), the Faraday cage, consists of four hinged 1 mm aluminium plates with a cladding of 4 mm PVC, (A,B,C,D). Two side walls (E) are fastened by screws to the bottom plate (C) and back wall (B), holding the box together.
The left side wall has a slit and a cable clamp, see Fig.14, for the EWF boom-wire.
The plasma simulator box is fully electrically isolated to prevent any hazard when driven by the high voltage amplifiers.
When packed for transport, the hinged plates are folded and the side walls are used to enclose the 15 m cable.

4.2. The sphere support board (Fig.14), held by two aluminium profiles on the side walls, is easily taken in and out of the simulator box. The sphere is resting with it's two rigid parts of the stubs on beddings of teflon, and secured with a turnable spring loaded piece of teflon.

The stimuli to sphere connector is a female contact, removed from a DIN 41612 connector, with the tip of it trimmed down to fit a 1 mm hole in the sphere assembly. When pressed together, inserted in the hole and released, it has sufficient spring to make good contact and to hold the flying wire.

At the right side of the board is a turnable PVC drum to wind the outer stub and guard of the sphere. It has two chambers to isolate the two wire parts being at different potentials.

A drum to wind the inner stub and guard is sketched on the left side. In order to avoid kinks on the wire, the mid-point of it is placed in a horse-shoe shaped plate, and the two wire parts are simultanuosly wound in the two chambers.

The boom wire clamp will pick up an accidentially pull of the wire. It is a split PVC cylinder, partly filled with silicon rubber (General Electric RTV 615 A+B) which is pressed against the wire. The silicon rubber is quite soft and give sufficient friction to lock the wire without degradation.

4.3. The simulator electronics (Fig.15) is connected to the stimuli box output via a 15 m long cable (Habia Type M17/4E, Sweden). The cable has two outer screens connected to the stimuli box cardframe, a RG 058 coax cable and six AWG 22 wires.

The elctronics box has two printed circuit boards 15 cm apart;

- One for relays K1,K2,K3 to switch the R/C network being plugged onto the board.
- One for K1, either connecting the Faraday cage to signal ground, or to the stimuli output via R4, box driven.

R4 is used for damping of oscillations (Ca. 2 MHz) most likely to occur at the edges of a square wave. Measurements indicate that the EFW plasma simulator represent a load of 10 uH in parallell with 100 pF.

Pulldown resistors of 22 K are connected to the relay driver inputs and to the +5 volts line.

5. The EPLD Design Files.

A programming software system (A+Plus) from Altera has been used with entry of Boolean equations for all the EPLD's in this section. The stand-alone microsequencer EPS448 is programmed in the design support software (SAM+PLUS) by use of the microcode assembler.

The commented design files describe the implemented logic functions, and are to be considered as guide lines for programmers. See the Altera handbooks for description of the macro cells and the programming conventions.

5.1. GPIB Acceptor Handshake Function. U6 in Fig.4.

```
Definition of logic levels:
    GPIB operates with low levels for logical true.
    The stimuli box operates with high levels for logical true
    with EXEPTION of: NRFD and NDAC beeing true when low.

T. A. Sten
Univ. of Oslo
April 4, 1989

PART: EPS448

INPUTS: ATN,                Attention from controller
        DAV,                Data Valid from controller
        LAD,                Listener Addressed, from Listener
        RXRDY               Stimuli box electronics ready

OUTPUTS:NRFD,               Not ready for data
        NDAC,               No data accepted
        RXSTR,              Strobe pulse for stim.box electronics
        ACD                 AH in active data state

DEFAULT: [1100]             Default output [], bits from left:
                            NRFD  NDAC  RXSTR  LAD

PROGRAM:                    Progr. state OD entered on r set by
                            IFC , internal counter loaded with 12
                            decimal is a "empty statement".

   OD: [] LOADC 12D;        Output default value [].

AIDJ:                       Acceptor Idle Stat

     IF ATN'& LAD' THEN [] JUMP AIDS;
                            If no ATN from controller and
                            Listener not in ADdressed State, set
                            NRFD and NDAC high and remain in idle
                            state. This statement is repeated in
                            all states below.
```

```
     ELSEIF ATN + LAD THEN [0000] JUMP ANRS;
                          Asume controller send a message,
                          initiated by ATN true. AF responds to
                          this by setting NRFD and NDAC low,
                          which informs the controller that we
                          are in busines so far.
                      or
                          Asume controller send data and that
                          Listener is ADdressed then NRFD and
                          NDAC must be low, informing the
                          controller that AH is ready for a
                          data-transfer sequence.

                          Note that AH is not ready for message
                          or data yet, jump to ANRS.

     ELSE [] JUMP AIDS;   If the controller has sent UNListen
                          message

ANRS:                     Acceptor Not Ready State

     IF ATN + RXRDY THEN [1000] JUMP ACRS;
                          If ATN is true, a message is under
                          way.
                      or
                          RXRDY is true, i.e. the stimulibox is
                          ready for data. Note that RXRDY is
                          wired to VCC in present the circuitry.
                      then
                          set NRDF high, telling the controller
                          that the stimuli box is ready for
                          data .
                          or message. By now such a byte is
                          placed on GPIB, and the controller
                          waits to see NRFD before it sets DAV
                          true after controller dependent time
                          TP.

                          jump to ACceptor Ready State and wait for

                          DAV to be true.

     ELSEIF ATN'& LAD' THEN [] JUMP AIDS;

     ELSE [0000] JUMP ANRS;

ACRS:                     Acceptor Ready State

     IF ATN' & LAD' THEN [] JUMP AIDS;

     ELSEIF ATN' & RXRDY' THEN [1100] JUMP ANRS;
                          Jump to ANRS if the stimuli box is
                          not ready for data.



     ELSEIF DAV THEN [0101] JUMP ACDS;
```

```
                              Data valid on bus.
                              Set NRFD low, not ready for more
                              data.
                              Keep NDAC high, no data accepted yet.
                              Set ACceptor Data State (ACD) flag,
                              and jump to ACDS

ACDS:                         Accept Data State

     IF ATN THEN [0001] LOADC 2D GOTO T3;
                              If ATN is true a message is valid on
                              bus. Load internal counter with 2
                              dec. and go to delay T3.

     ELSEIF ATN' & LAD' THEN [] JUMP AIDS;

     ELSEIF ATN' THEN [0110] JUMP AWNS;
                              Valid data on bus, set strobe pulse
                              RXSTR for stim.box latches and
                         registers over one CP.

T3:  [0001] LOOPNZ T3 ONZERO T3A;
                              Wait in ACDS for 3 CP before setting
                              NDAC high.

T3A: IF ATN THEN [0100] JUMP AWNS;
                              NDAC set high, indicating to
                              controller that stim.box has accepted
                              data. When sensing this the
                              controller will set DAV false after
                              1P.

     ELSE [0001] JUMP ACDS;

AWNS:                         Acceptor Wait for New Cycle

     IF DAV' THEN [0000] JUMP ANRS;
                              If DAV false, jump ANRS and a new
                              cycle may start. RXSTR is now set
                              low.

     ELSEIF ATN' & LAD' THEN [] JUMP AIDS;

     ELSE [0100] JUMP AWNS;
                              Keep NRDF and NRFD high, wait for the
                              controller to set DAV false.

END$
```

5.2. GPIB Listen Function. U5 in Fig.4.

All logic symbols below are true when high EXEPT for IFC and SEL3 beeing active low.

T. A. Sten
Univ. of Oslo
March 1, 1989

PART: EP610

INPUTS:

ATN, DAV,	GPIB handshake lines
IFC,	InterFace Clear
ACD,	Active data state flag ACD from AH
D0 to D7,	Data bits on internal bus
CP,	System clock 4.160 MHz.
pon,	Power On information
RXSTR	Strobe pulse for SEL3

OUTPUTS:

LAC,	Listener Active State
DCL,	Device Clear
SEL3	Decoder output addr. 3

NETWORK:

```
ATN = INP(ATN)
DAV = INP(DAV)
IFC = INP(IFC)
pon = INP(pon)
ACD = INP(ACD)
RXSTR = INP(RXSTR)
CP = INP(CP)
CPI = CLKS(CP)

LAC,LACF = SOSF(FSI,CPI,FRI,CLRI, ,VCC)
                          A clocked Set/Res flip-flop
                          with:
                          - LAC output, LACF feedback
                          - FSI   set input
                          - CPI   clock input
                          - FRI   reset input from logic
                          - CLRI  clear input

DCL = CONF(DCI,VCC)       Buffer output DCL, input DCI.

SEL3 = CONF(YJI,VCC)      Buffer output SEL3, input YJI
```

```
EQUATIONS:

      FSI = ATN & DAV & MLA;
                                    Set f-f when:
                                    - ATN is true, message present
                                      on GPIB
                                    - DAV is true, data valid on bus
                                    - MLA My Listen Address is true

      FRI = ATN & DAV & UNL
                                    Reset f-f when UNListen message
                  +                 or
            ATN & DVA & MTA;        My Talk Address has been
                                    detected.

      DCI = ATN & ACD & SDC & LACF;
                                    Set Device CLear output high if:
                                    - Listen Active State, LACF
                                    - AH is in ACceptor Data State
                                    - ATN is true
                                    - Selected Device Clear message
                                      is detected.
                        +       or
            ATN & ACD & DCLR;
                                    - When a universal Device CLeaR
                                      is received

      SDC = D6' & D5' & D4' & D3' & D2 & D1' & D0';
                                    Selected Device Clear Code

     DCLR = D6' & D5' & D4  & D3' & D2 & D1' & D0';
                                    Device Clear Code

      MLA = D6' & D5  & D4' & D3  & D2 & D1' & D0 ;
                                    My Listen Address. 1' decimal.

      MTA = D6  & D5' & D4' & D3  & D2 & D1' & D0 ;
                                    My Talk Address. 13 decimal.

      UNL = D6' & D5  & D4  & D3  & D2 & D1  & D0 ;
                                    UNlisten Code

      CLRI = IFC' & pon;
                                    Clear f-f when IFC and pon are
                                    true

      Y3I = /' D7' & D6 & D5 & RXSTR);
                                    Set SEL) output low when
                                    addressed to 3x  Hex) and RXSTR
                                    is present.

END$
```

5.3. Relay Function Decoder. U15 in Fig.4.

T. A. Sten
Univ. of Oslo
Oct. 29, 1990

```
PART: EP310

INPUTS:

        K10, K11, K12, K13,                 See input module Fig.8
        K14, K15, K16                       for relay functions.

OUTPUTS:
                                        To LED drivers for:

        Fgen,                               HP 3325A
        Ngen,                               HP 8904A
        S10, S1,                            Sine Ref. 10V and 1V
        P5, P1,                             Pulse 5V, 1V, and
        P01                                 .01V
        GRND                                Signal Ground

NETWORK:

        K10 = INP(K10)                      A standard input
              :                             configuration
        K16 = INP(K16)                      as in section 4.2.

        Fgen = CONF(FgenI,VCC)              Configuration of the
        Ngen = CONF(NgenI,VCC)              output buffers,
        S10  = CONF( S10I,VCC)              Combinatorial
        S1   = CONF(  S1I,VCC)              Output
        P5   = CONF(  P5I,VCC)              No
        P1   = CONF(  P1I,VCC)              Feedback.
        P01  = CONF( P01I,VCC)              Output enable is
        GRND = CONF(GRNDI,VCC)              connected to VCC.


EQUATIONS:                                  For the buffer
                                            inputs:
        FgenI = K10';
        NgenI = K10 & K11';
        S10I  = K10 & K11 & K12 & K13' & K14;
        S1I   = K10 & K11 & K12 & K13' & K14';
        P5I   = K10 & K11 & K12 & K13  & K15 & K16;
        P1I   = K10 & K11 & K12 & K13  & K15 & K16';
        P01I  = K10 & K11 & K12 & K13  & K15';
        GRNDI = K10 & K11 & K12';

END$
```

5.4. Timer latches. U7 in Fig.4.

T. A. Sten
Univ. of Oslo
Sept. 19, 1990

```
PART: EP 610

INPUTS:
      D0, D1, D2, D3,              To both latches.
      D5, D6, D7,                  3-to-8 line dec.
      DCL,                         Device clear.
      RXSTR                        Strobe pulse.

OUTPUTS:
      DO4, DO5, DO6, DO7,          Latched data.
      A0, A1,                      Latched addr.
      SEL0, SEL1, SEL2,            Decoder outputs
      SEL6, SEL7

NETWORK:
      D0 = INP(D0)
         :
      D7 = INP(D7)
      DCL    = INP(DCL)
      RXSTR = INP(RXSTR)
                                   Asyncron clocks for
      CLK1   = CLKB(CLK1I)         data latch
      CLK2   = CLKB(CLK2I)         addr. latch.

      DO4 = RONF(D0,CLK1,DCL,VCC)  D-type flip-flops.
      DO5 = RONF(D1,CLK1,DCL,VCC)
      DO6 = RONF(D2,CLK1,DCL,VCC)
      DO7 = RONF(D3,CLK1,DCL,VCC)

      A0  = RONF(D0,CLK2,DCL,VCC)
      A1 =  RONF(D1,CLK2,DCL,VCC)

      SEL0 = CONF(Y0I,VCC)                    Buffers.
      SEL1 = CONF(Y1I,VCC)
      SEL2 = CONF(Y2I,VCC)
      SEL6 = CONF (Y6I,VCC)
      SEL7 = CONF(Y7I,VCC)

EQUATIONS:

      CLK1I =  D7  & D6  & D5' & RXSTR;        Clock inputs.
      CLK2I =  D7  & D6' & D5  & RXSTR;

       0I   = (D7' & D6' & D5' & RXSTR)';      Buffer inputs.
      Y1I   = (D7' & D6' & D5  & RXSTR)';
      Y2I   = (D7' & D6  & D5' & RXSTR)';

      Y6I   = (D7  & D6  & D5' & RXSTR)';
      Y7I   = (D7  & D6  & D5  & RXSTR)';
END$
```

5.5. Function Panel Logic. U3 in Fig.6.

T. A. Sten
Univ. of Oslo
Feb. 2, 1991.

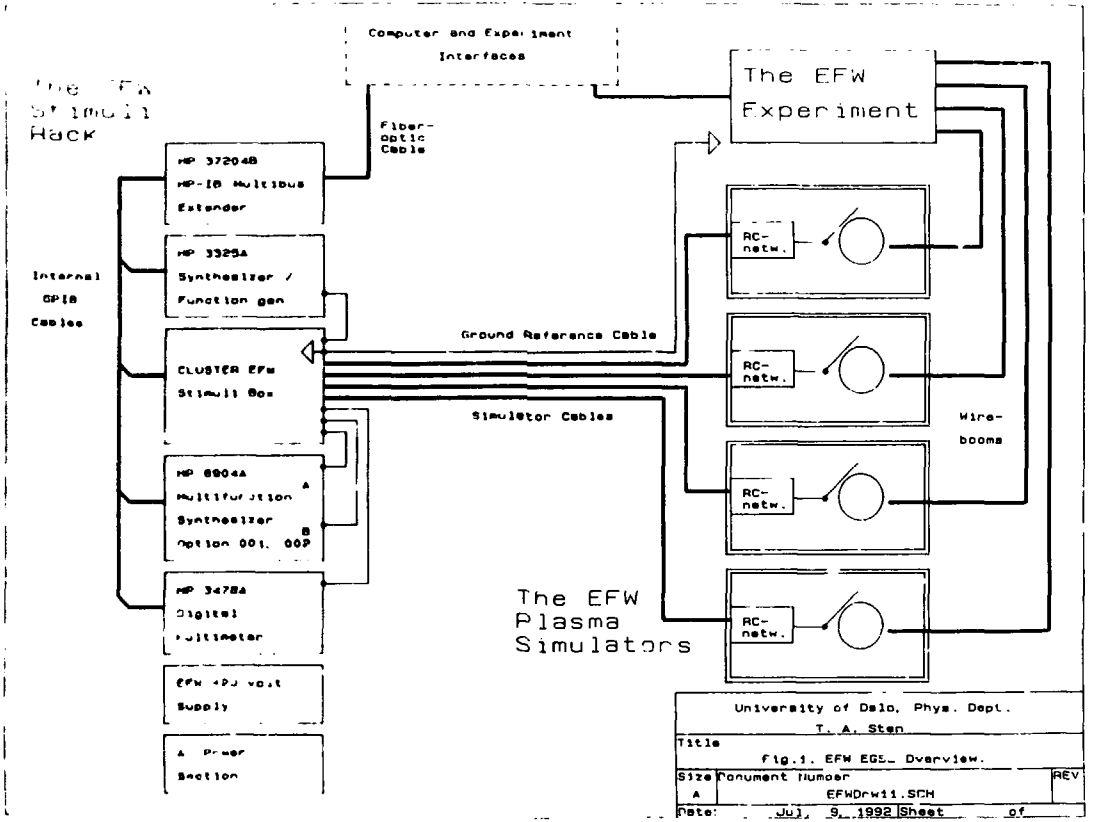
```
PART: EP 310

INPUTS:

      K6, K7, K8,                    See output module
                                     Fig.10.
      LTN                            Listener addressed.

OUTPUTS:
                                     To LED drivers for:

      BX1,                           HV-amplifier in
      BX10,                          Line B.
      PHA,                           Phase input.
      GRN,                           Ground.
      LISTN,                         Listen.
      AB                             Solid state relay
                                     driver.

NETWORK:

      K6 = INP(K6)
      K7 = INP(K7)
      K8 = INP(K8)

      LTN   = INP(LTN)

      BX1   = CONF(BX1I,VCC)
      BX10  = CONF(BX10I,VCC)
      PHA   = CONF(PHAI,VCC)
      GRN   = CONF(GRNI,VCC)
      LISTN = CONF(LITNI,VCC)
      AB    = CONF(ABI,VCC)


EQUATIONS:

      BX1I  = (K7' & K6')';          Theese indicators will

      BX10I = (K7  & K6')';           be switched off if:

      PHAI  = (K6  & K8')';           Phase input, or

      GRNI  = (K6  & K8 )';           Ground is selected.

      LITNI = LTN';

      ABI   = K5 + K7;                Solid state relay on
                                      if Ax10 or Bx10
END;
```

5.6. Pulse Attenuator. U6 in Fig.8.

T. A. Sten
Univ. of Oslo
Oct. 29, 1990.

```
PART: EP310

INPUTS:
  P,                          Pulse frequency
  K15, K16                    and amplitude control

OUTPUTS:

  B1,                         Pulse to bit 1, MSB
  B2, B3, B4,                 Bit groups, page 8.
  B9, B10, B11, B12           Bits 9 to 12, LSB

NETWORK:

  B1  =  CONF(P   , VCC)        Declaration of
  B2  =  CONF(BI2 , VCC)        output buffers
  B3  =  CONF(BI3 , VCC)
  B4  =  CONF(BI4 , VCC)
  B9  =  CONF(BI9 , VCC)
  B10 =  CONF(BI10, VCC)
  B11 =  CONF(BI11, VCC)
  B12 =  CONF(BI12, VCC)


EQUATIONS:
                              Set amplitude to:
 A = K15' & K16';              5 volt
 B = K15' & K16 ;              1 volt
 C = K15  & K16';              0.01 volt

                                        P is bit 1, MSB

 BI2  = P & A + P' & B + P' & C;      Bit 2 and 3

 BI3  = P & A + P' & B + P' & C;      Bit 4, 5 and 8

 BI4  = P & A + P  & B + P' & C;      Bit 6 and 7

 BI9  = P & A + P' & B + P' & C;      Bit 9

 BI10 = P & A + P  & B;               Bit 10

 BI11 = P & A + P  & B + C;           Bit 11

 BI12 =         P  & B + C;           Bit 12, LSB.

END$
```

For the nominal output of +/- 5 mV, please note that the terms BI10-12 introduce an off-set and provide an output of + 3.66 mV and - 4.88 mV.


Computer and Experiment Interfaces
The EFW Experiment
The EFW Stimuli Rack
Fiber-optic Cable
HP 37204B
HP-IB Multibus Extender
HP 3325A
Synthesizer / Function gen
Internal GPIB Cables
CLUSTER EFW Stimuli Box
Ground Reference Cable
Simulator Cables
HP 8904A
Multifunction Synthesizer
Option 001, 002
HP 3478A
Digital Multimeter
EFW +PJ volt Supply
A Power Section
RC-netw.
RC-netw.
RC-netw.
RC-netw.
Wire-booms
The EFW Plasma Simulators
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Title
Fig.1. EFW EGSE Overview.
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Document Number
EFWDrw11.SCH
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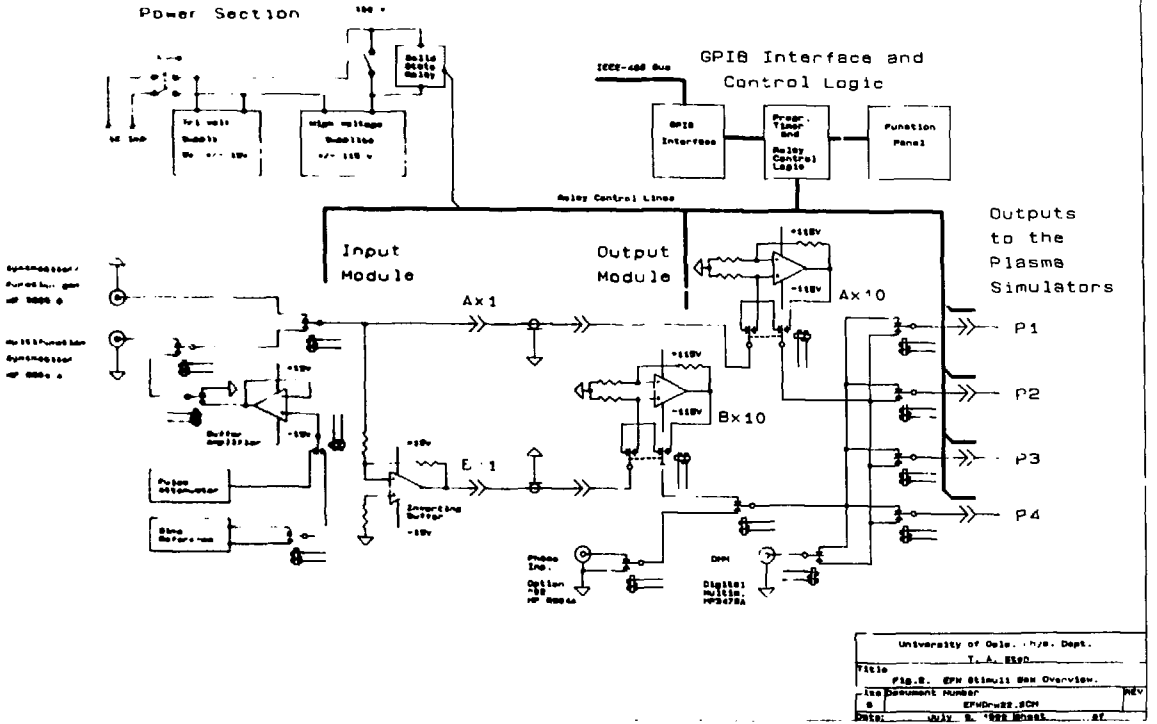
Date: Jul, 9, 1992 Sheet of


Power Section
GPIB Interface and
Control Logic
IEEE-488 Bus
GPIB
Interface
Timer
and
Relay
Control
Logic
Function
Panel
Relay Control Lines
Input
Module
Output
Module
Outputs
to the
Plasma
Simulators
Ax1
Ax10
Bx10
E x 1
P1
P2
P3
P4
+15V
-15V
Buffer
Amplifier
Inverting
Buffer
Pulse
Generator
Sine
Reference
Phase
Inv.
Option
-59
DPM
Digital
Multim.
HP3478A
University of Colo. - H/B. Dept.
T. A. ESD
Title
Fig.8. EPH Stimuli Box Overview.
Size
B
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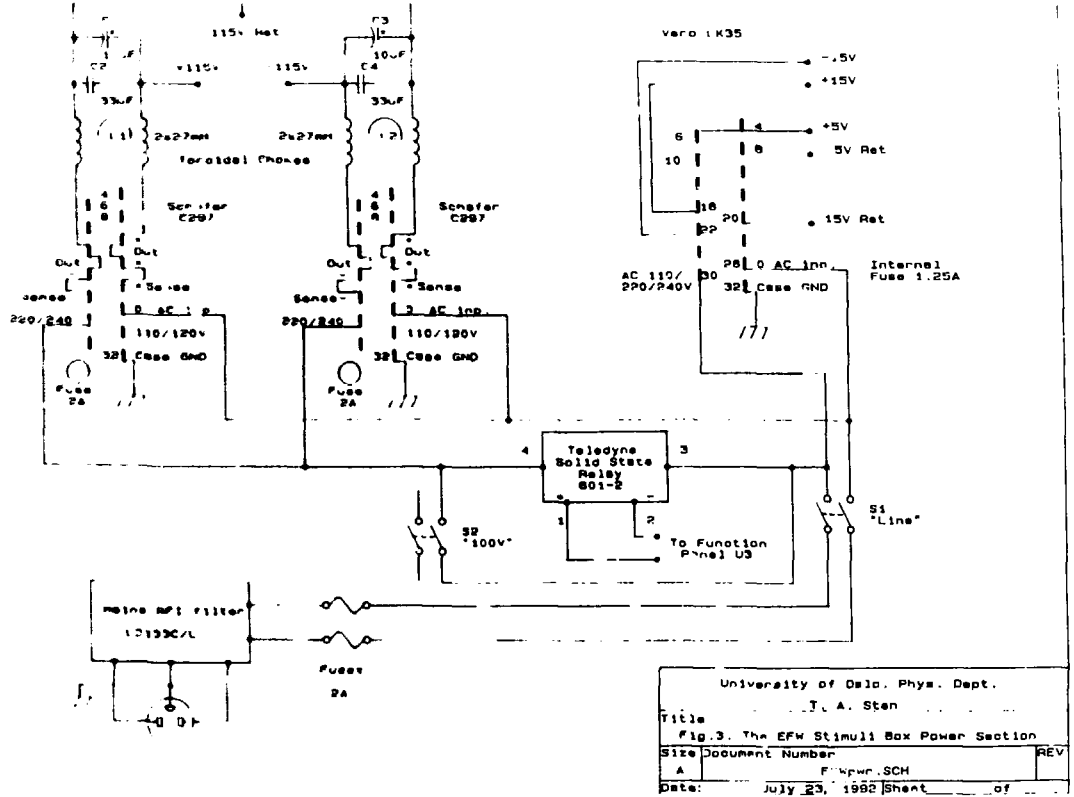
EPHOvw22.SCH
REV
Date:
July 8, 1988
Sheet
of


115v Hot
C3
10uF
C2
+115v
115v
C4
33uF
33uF
(1)
2x27mH
2x27mH
(2)
Toroidal Chokes
Schafer
C297
Schafer
C297
Out
Sense
AC inp.
110/120v
220/240
Case GND
Fuse
2A
Vero iK35
-15V
+15V
+5V
5V Ret
15V Ret
AC 110/
220/240V
AC inp.
Case GND
Internal
Fuse 1.25A
Teledyne
Solid State
Relay
601-2
To Function
Panel U3
S2
"100V"
S1
"Line"
Mains RFI Filter
Fuses
2A
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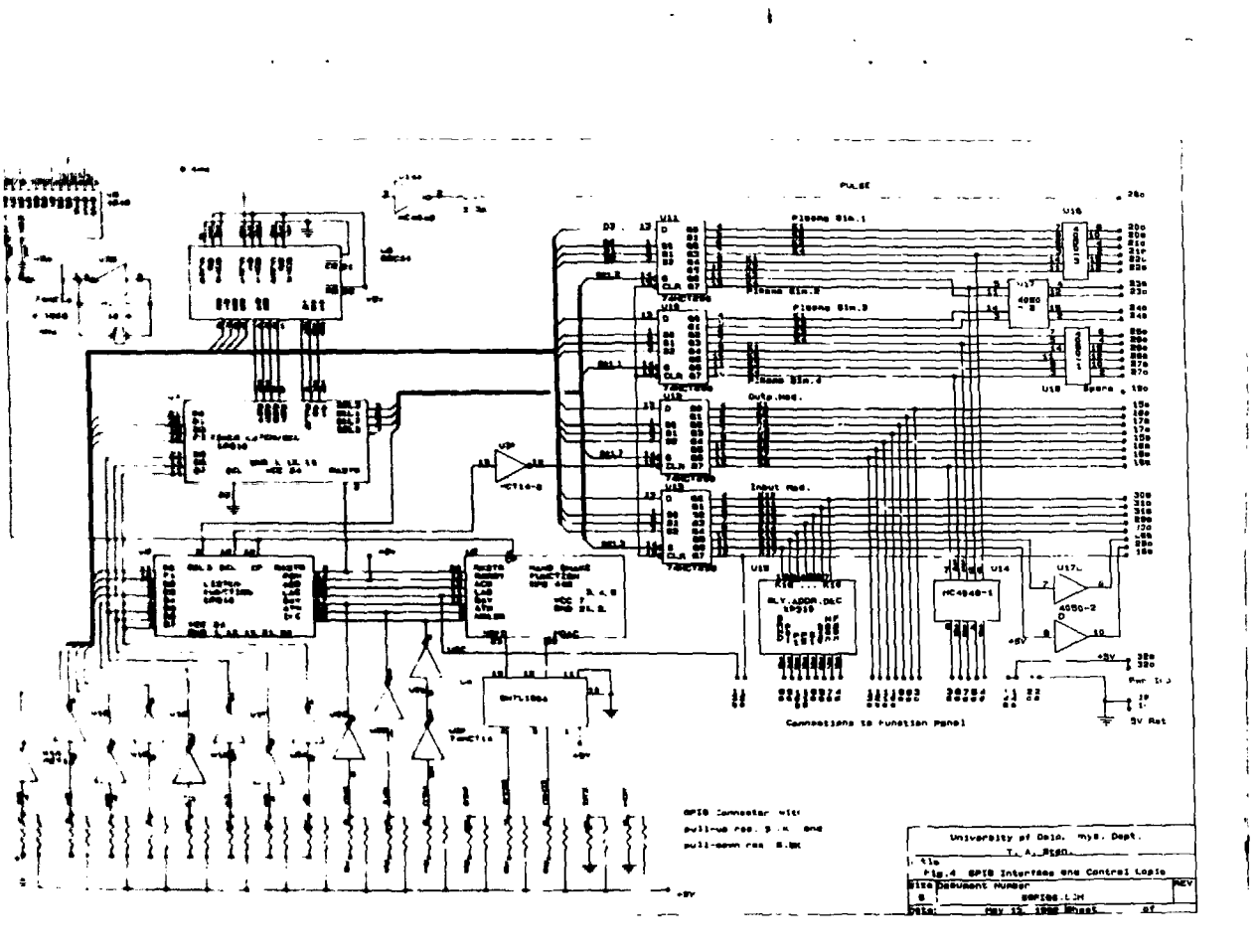
T. A. Sten
Title
Fig.3. The EFW Stimuli Box Power Section
Size
A
Document Number
EFWPWR.SCH
REV
Date:
July 23, 1992
Sheet
of


PULSE
Plasma Dis.1
Plasma Dis.2
Plasma Dis.3
Plasma Dis.4
Outp.Mod.
Input Mod.
Spare
MC4040-1
4050-2
+5V
Connections to Function Panel
GPIB Connector with
pull-up res. 3 K ohms and
pull-down res. 5.6K
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T. A. Bjøn.
Fig.4 GPIB Interface and Control Logic
Size
Document Number
GPIB6.1.SCH
Date:
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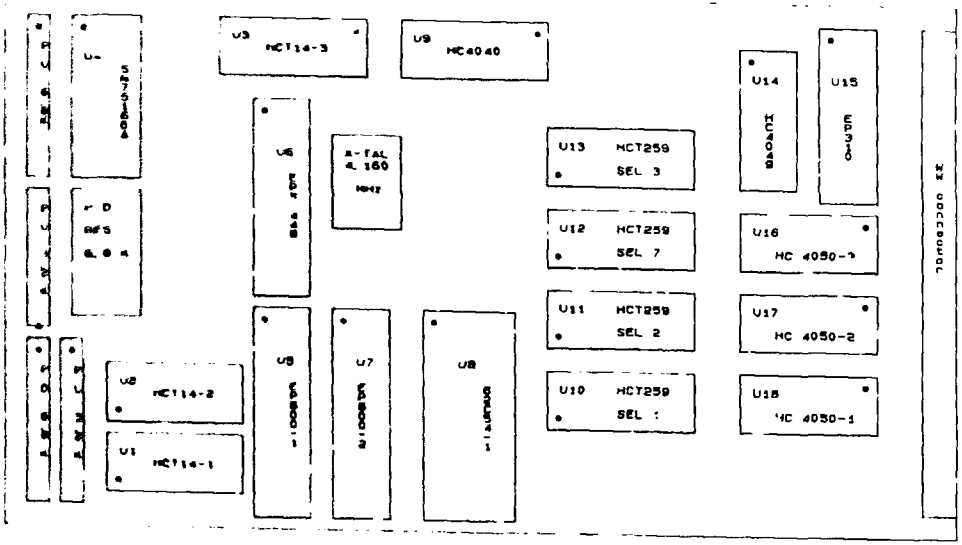
of



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T. A. Sten		
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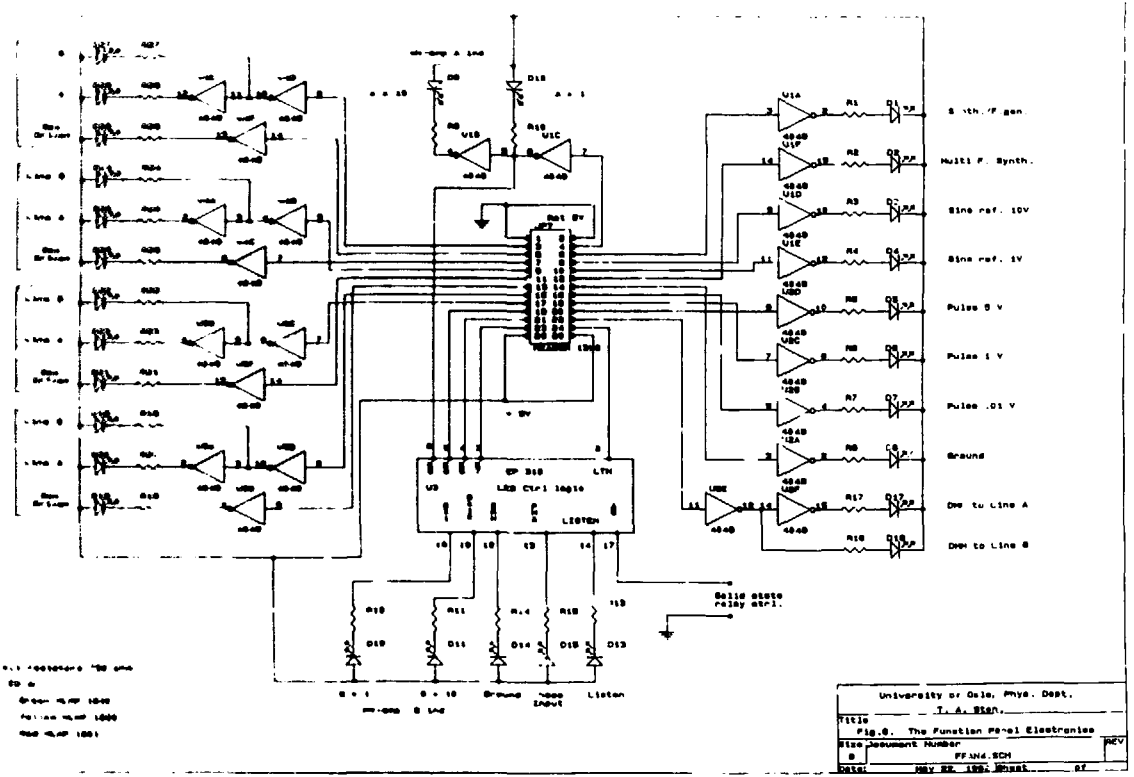
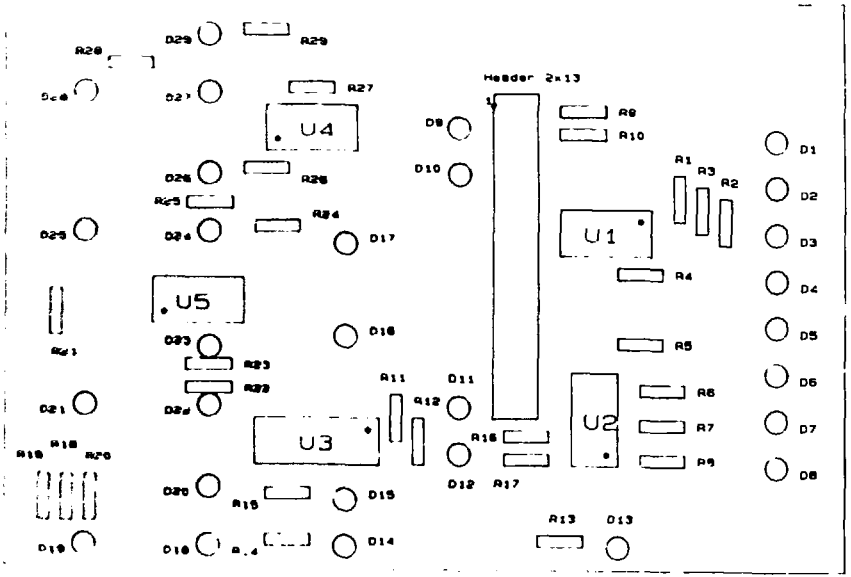
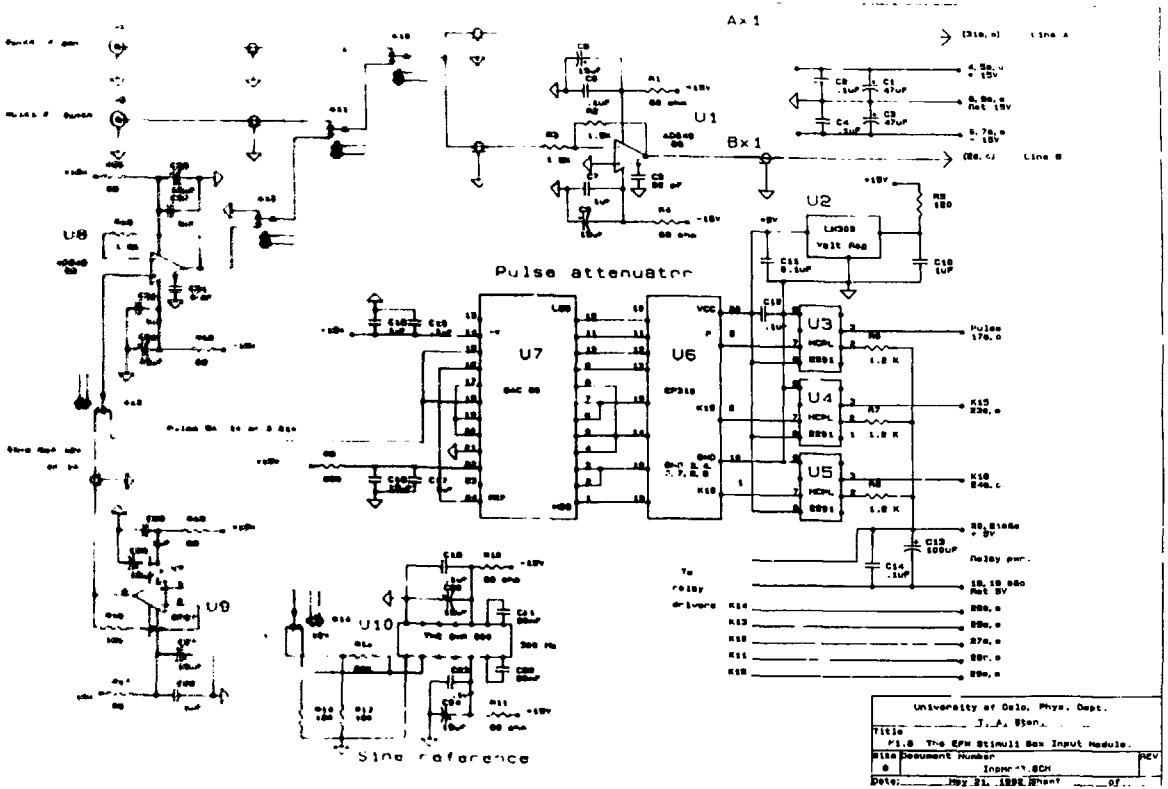

Sine ref. 10V
Sine ref. 1V
Pulse 0 V
Pulse 1 V
Pulse .01 V
Ground
Solid state relay ctrl.
Listen
University of Oslo, Phys. Dept.
T. A. Bjøn
Fig.8. The Function Panel Electronics
FFUnd.SCM



University of Oslo, Phys. Dept. T. A. Stan		
Title: Fig.7. The Function Panel Card.		
Size: A	Document Number: FpanLo SCH	Rev
Date: May 22, 1992	Sheet of	


Ax1
Bx1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
Pulse attenuator
Sine reference
Pulse 170.0
K15 830.0
K10 840.0
Relay pwr.
Relay drivers
K14 880.0
K13 890.0
K12 870.0
K11 880.0
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University of Oslo, Phys. Dept.
Title
P1.8 The EPN Stimuli Box Input Module.
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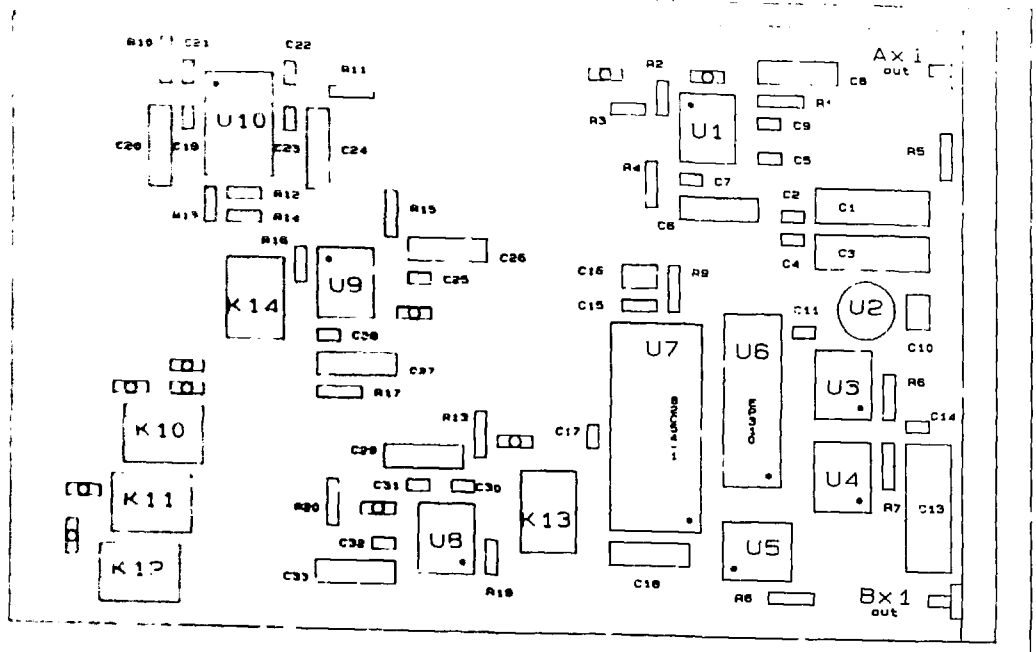

University of Oslo, Phys. Dept.		
T. A. Sten		
Title: Fig.6 The Input Module Card		
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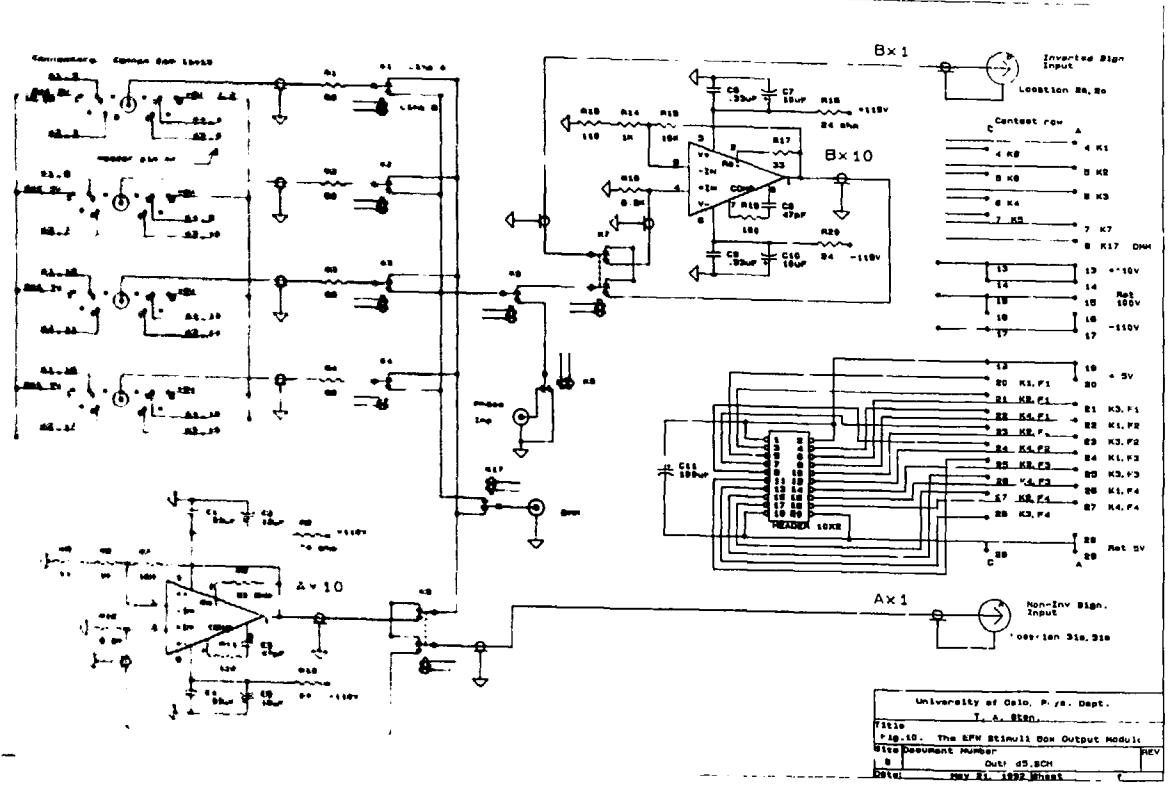
Date: May 22, 1992	Sheet of	


Bx1
Bx10
Ax10
Ax1
Inverted Sign Input
Location R6,R8
Context row
4 K8
5 K8
6 K4
7 K5
4 K1
5 K2
6 K3
7 K7
8 K17 DMM
+10V
Ref 100V
-110V
+5V
K1,P1
K8,P1
K5,P1
K8,P
K4,P2
K8,P3
K4,P3
K8,P4
K3,P4
K3,P1
K1,P2
K3,P2
K1,P3
K3,P3
K1,P4
K4,P4
Ref 5V
C11 100nF
HEADER 10X8
Non-Inv Sign. Input
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T. A. Bjøn.
Title
Fig.10. The EPW Stimuli Box Output Module
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B Out d5.SCH
Date: May 01, 1992 Sheet

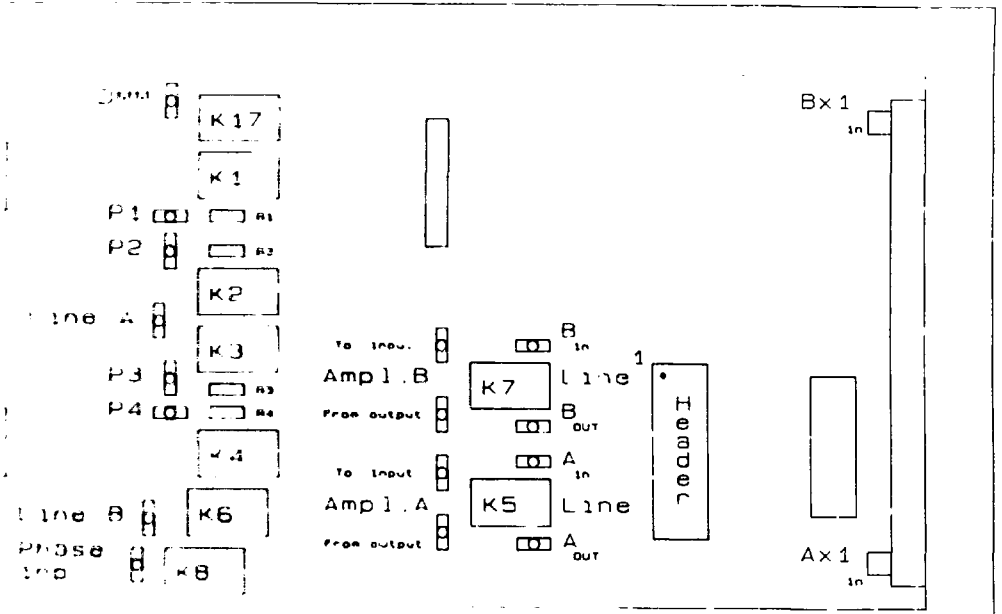

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Fig.11. The Output Module Card		
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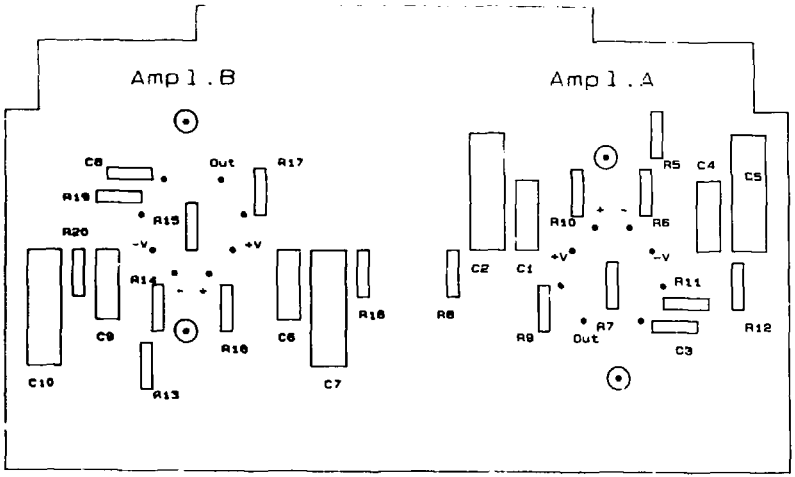
Date: May 22, 1992	Sheet of	



University of Oslo. Phys. Dept.		
T. A. Sten		
Title Fig.12. Output Module Amplifier Card.		
Size A	Document Number 4Vampord.SCH	REV
Date: May 21, 1992	Sheet of	

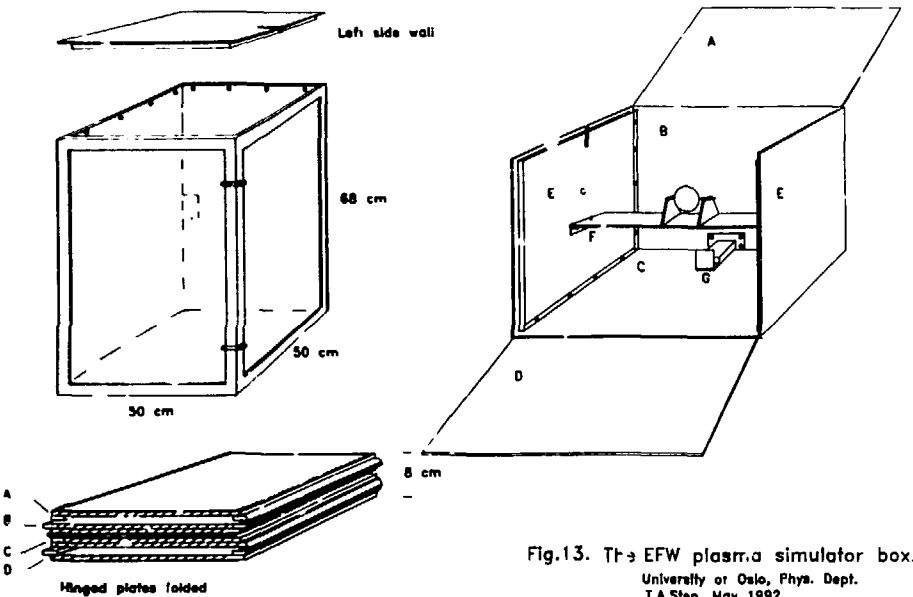


Fig.13. The EFW plasma simulator box.

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T.A.Sten, May 1992.

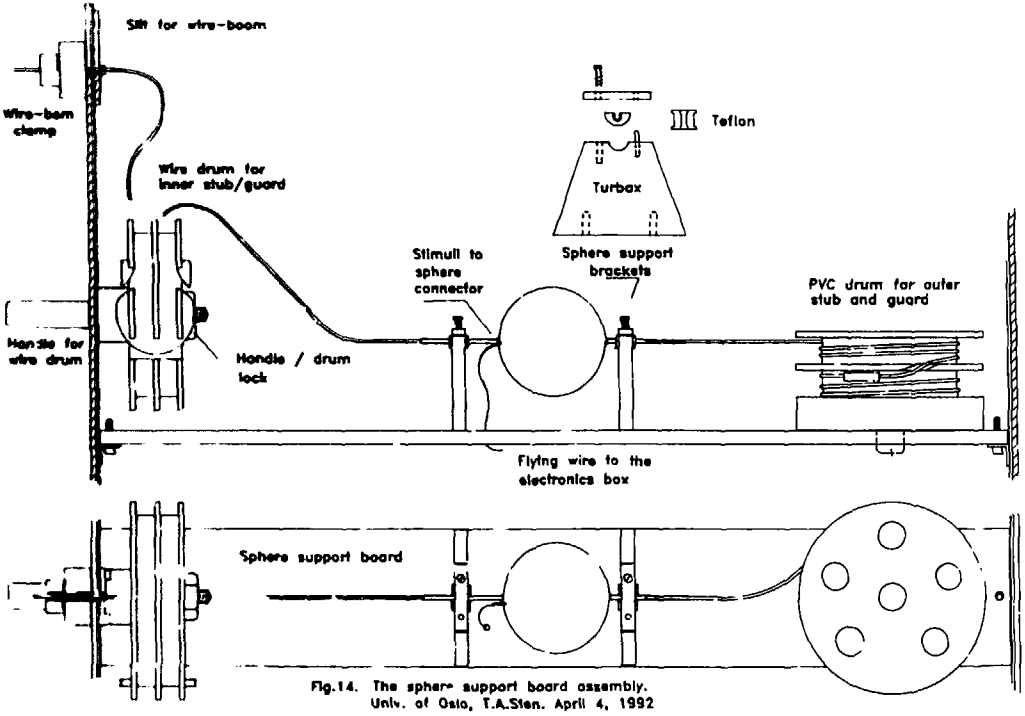
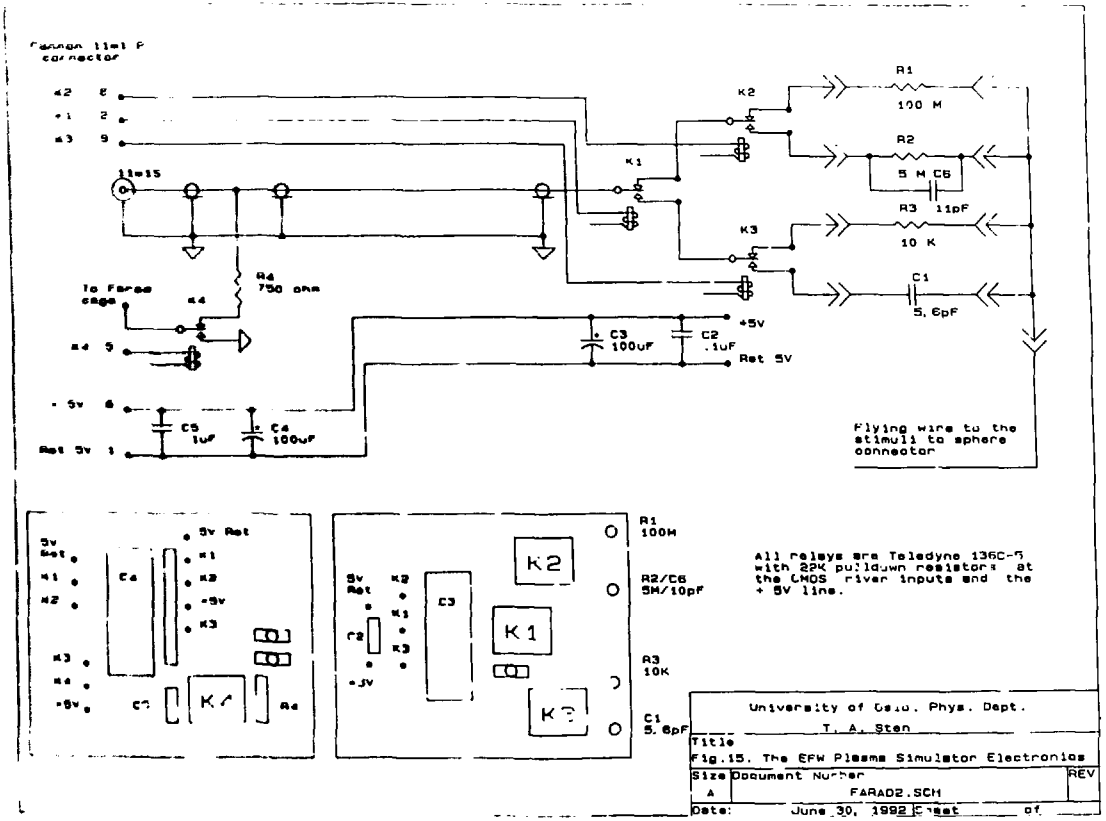


Fig.14. The sphere support board assembly.
Univ. of Oslo, T.A.Sten. April 4, 1992


Faraday 11ml P connector
K2
K1
K3
11=15
R1
100 M
R2
5 M C6
R3 11pF
10 K
C1
5.6pF
R4
750 ohm
To Farad cage
K4
K4
5
-5v
6
Ret 5v
1
C5
1uF
C4
100uF
C3
100uF
C2
.1uF
+5V
Ret 5V
Flying wire to the stimuli to sphere connector
5v Ret
K1
K2
K3
K4
-5v
C4
C5
C6
R4
C3
C2
+5V
R1
100M
R2/C6
5M/10pF
R3
10K
C1
5.6pF
All relays are Teledyne 136C-5 with 22K pulldown resistors at the CMOS driver inputs and the + 5V line.
University of Calif. Phys. Dept.
T. A. Sten
Title
Fig.15. The EFW Plasma Simulator Electronics
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A
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June 30, 1992
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Elementærpartikkel-fysikk	Experimental Elementary Particle physics
Faste stoffers fysikk	Condensed Matter physics
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