PROGRAMMABLE LOGIC CONTROLLERS IN HEAVY WATER PROJECT, MANUGURU

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Enhancement to plant operational flexibility has been achieved in Heavy Water Project, Manuguru by installing Programmable Logic controllers for its control equipment. Earlier Sulfide based Heavy Water Plant, Kota is using Relay logic and Diode based Program-matrix for binary controls. Performance improvement and advantages of PLC and experience in its operation are described in the paper. The different parts of the paper are as follows.

1. The scheme used in Kota.

2. Limitations of the scheme(Realy logic plus Diode Matrix) used at Kota

3. Description of the PLC system used in Heavy water plant, Manuguru.

4. Specifications of PLC used at Manuguru.

5. Brief description of system structure & software of PLC used.

6. Experience in PLCs' operation.

7. Conclusions.

1. SCHEME USED IN KOTA :

The Heavy Water Plant Kota uses diode matrix scheme for its open loop controls which consists of control loops of shutdown valves & pumps for its exchange unit. The scheme is described by the fig(1).

2. LIMITATIONS OF RELAY LOGIC AND DIODE MATRIX SCHEME :

1. Modifications in the programme need wiring modifications in the relay logic which is a cumbersome job.

2. With diode matrix, only logic capability available is 'ORing'

3. Short circuit of a diode leads to unintended operations. for eg., if diode at A is shorted, then upon actuation of PT Scram, all actions of M-Scram will be initiated. This is a serious fault as unintended operations will occur.

4. To find a fault (such as the short circuited diode at A) it takes lot of time thus increasing down time.

3. DESCRIPTION OF PLC SYSTEM :

There are 3 PLCs used in HWP, Manuguru each one catering to (i) exchange unit I (ii) exchange Unit II & (iii) utilities consisting of open loop binary controls for H2S generation plant, sealant system, drain system and H2S monitors.

PLC-1 has 500 inputs and 600 outputs. Each plc cabinet, as such can take 3200 inputs, outputs, flags & network inputs etc. However, as a large no. of flags are employed and large amount of logic is executed, each PLC as originally envisaged has been built around 2 nos. of PLCs. The network diagram is placed at Fig.2.

Each PLC processing the logic has hot active redundancy in CPU (with associated memory, watch dog monitors and power supplies) so that failure of a single CPU does not affect the plant operation. To reduce the cost, input and output cards have not been duplicated but the cards procured are testable through a combination of hardware and software design.

For sequence of events recording, a separate single - CPU based PLC is used corresponding to each of the three main PLCs. Similarly a separate single - CPU based PLC is used in case of PLCs for XUs to gather data from 2 nos. of sub-PLCs to corr. Sequence of Event Recording PLCs. Figure 2 shows the interface net work. As shown in the figure, 2 nos. of programming units are used to connect to various PLCs for use in monitoring their operation, forcing inputs and outputs as also to load the CPUs with the project programme to begin with, or in case of modifications after the initial loading.

4. SPECIFICATIONS OF PLC H-50H USED IN HWP, MANUGURU :

Mechanical design	19" Modular.
Processor	Microprocessor Z80A.
Program memory	CMOS-RAM buffered with lithium battery.
Max. memory size	64 K byte. for user 32 K byte.
Interfaces	
RS 232C	Max 8 nos.
Average cycle time	3 ms/k instructions.
Max size	3600 sum of all binary, digital, analog inputs, outputs, flags etc. Max. 256 I/O Cards.
Time ranges	0.1 S, 1 s, 1 min upto 65534 min (max. 43 days) programmable.
Binary inputs	Contacts, proximity switches.
Binary outputs	400 mA short circuit proof. Higher capacities through relays.
Mains supply	24 V DC, +20%, -15% rpp<15% obtained from 110 V DC thro' a DC-DC convertor.
Ambient conditions	0 to 60 °C.
Storage temperature	-40 °C to 85 °C.

Operating voltage 5V (micro processor)
24V (peripheral units).

5. BRIEF DESCRIPTION OF THE SYSTEM STRUCTURE & SOFTWARE :

1. Structure of the system with 2 central processors.
Ref to drawing no. at A1.

2. The user's program is operated synchronously in phases in 2 central processors. After each phase, the results are compared and necessary data are sent to the other central processor. The central processors operate in master slave principle. The master system processes the inputs and outputs and sends the needed data to the slave sysyem. If there is an error in one CPU,a message results and the CPU in question switches itself off. The other CPU then takes over instantaneously using all the data present. According to the degree of fail-safe operation required single-channel operation can e.g. continue for a limited time, an unlimited time - or the whole system can switch off immediately, this option being determined via the user's program through an operational building block. After each cycle, master & slave CPUs exchange roles.

The fail-safe input/output circuits include testable input/output amplifiers which are tested automatically by the system during each cycle and their faults can be indicated.

The necessary test routines for the CPUs and for the testable input/output amplifiers are called up by the input of the type of testable input/output amplifiers in the program "name coordination" and by the use of required operating system in the CPU (EPROM).

The system checks the testable input amplifiers to determine whether the input channels are ready to switch through both signal levels (low or high signal), irrespective of the current input signal. When a fault occurs, a low signal is produced internally for a logic processing for the faulty channel of the card positions in question. For the user this signal represents a logical extension to input level of the fail-safe principle. Circuit discontinuity or errors in the input amplifier produce a low signal (usually resulting in trip).

In the testable output amplifiers, the output signals are read back during each cycle and compared with the output signals of the user's program. In addition, switchability of the output is tested not less than once every ten minutes. This means that irrespective of the current logic signal, a complete signal change low to high/ high to low or high to low/ low to high is carried out. In case of an error, a second cutoff circuit is provided, which switches off the supply voltage of the output amplifier in question. The user's program also includes whether in the case of a fault all the outputs or only the specific group of output amplifiers shall be switched off.

The operational system of the building block permits:

- One channel start-up after power failure.
- Forcing of testable I/O amplifiers.
- On-line alterations depending on conditions.
- Use of software building blocks.
- Set up of a network system to connect printers, VDUs, PLCs or to transmit data to other systems.
- Direct connection of 2 process control systems.

The operational system of building block offers:

- Complete supervision of the central processor rack with a high availability by the second cen tral processor rack.

- Supervision of the complete I/O range using testable coupling cards and testable I/O amps.

- An instant and specific annunciation for a safe and fast repair just by replacing the faulty card during operation of the plant.

General Operating System test routines:

CPU:

- Hardware monitoring of clock pulse.
- Cycle monitoring via hardware and software watchdog.
- Process monitoring by the CPU in the other central rack.
- Range monitoring.
- Self tests.
- Comparison of different independent hardware timers.

Memory:

- Memory comparison with the other CPU.
- Program store: modified checksum test.
- Data store: test for read/write ability.

Monitoring unit:

- Monitoring correct sequence through comparison of independent hardware times.
- Monitoring for switch-off capability.

High speed serial Interface RS 422 :

- Continuous testing through comprehensively pro tected comparison of transmissions and memory.
- Test of the DMA modules for the time behavior, address and blocking errors.

Coupling units

- Test for interlock and enabling of access to the input/output level.

- Test of all circuits via sophisticated read rou tine for testable input/output amplifiers.

Real time clock

- Test whether a real time clock is actually present.
- Test for regular interrupt.

PIO module

- Reception of regular interrupt.

In case of not allocated errors, a comprehensive self test is started in the related central processor rack while the other central processor rack continues the plant operation in single run. In controls with safety applications, the controls are completely switched off in case of not allocated errors.

6. EXPERIENCE IN OPERATION OF PLCs :

The PLC system has been found to be highly useful because of (i) ease with which modifications in the control logic of binary equipment have been possible through the flexibility in reprogramming the user's programme, (ii) on-line by-passing of defective switches in the input logic of binary control equipment through the feature of input/output forcing, and (iii) availability of graphic representation of the logic on the screen with identification of input/ outputs being in '0' or '1' state, and thus helping in identifying the root cause of any unsuccessful logic implementation. However, a few problems have also been faced, some of which are peculiar to programmable systems in general. The problems faced are:

(a) Spurious faults:

Many a time, spurious faults appear in PLC cabinets. On resetting,the faults disappear. The exact cause of such spurious faults is not known. The matter is under investigation with the foreign vendor. However, due to redundancy in the CPUs and other units as mentioned earlier, these spurious faults have normally not resulted in a trip of the plant.

(b) Memory erasure:

Many a time, the memory gets erased in one CPU and it has to be reloaded through the programming unit. Again, exact cause is not known, and the matter is resting with the foreign vendor. And as in earlier case, normally no trip has resulted on this account.

(c) Hardware Failures:

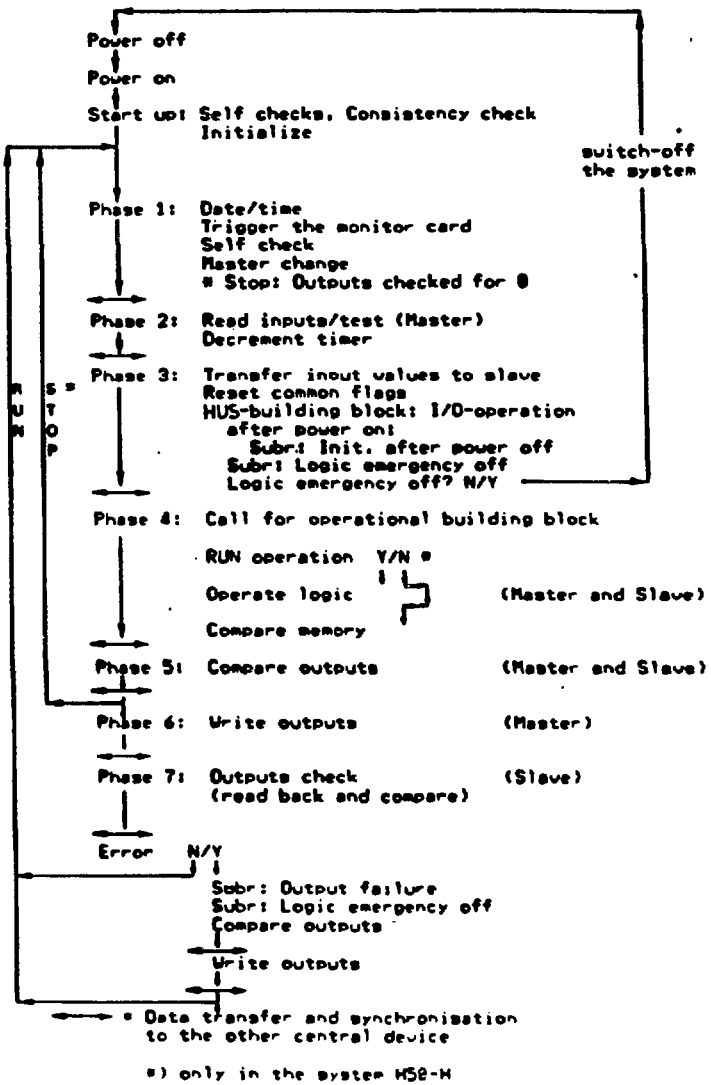
Compared to the high MTBF figures claimed by the vendor, a somewhat larger no. of various cards have failed (O/P cards =12, I/P Cards=2, Communication Cards=2, CPU cards=2 against installation populations of around 170, 110, 30, 17

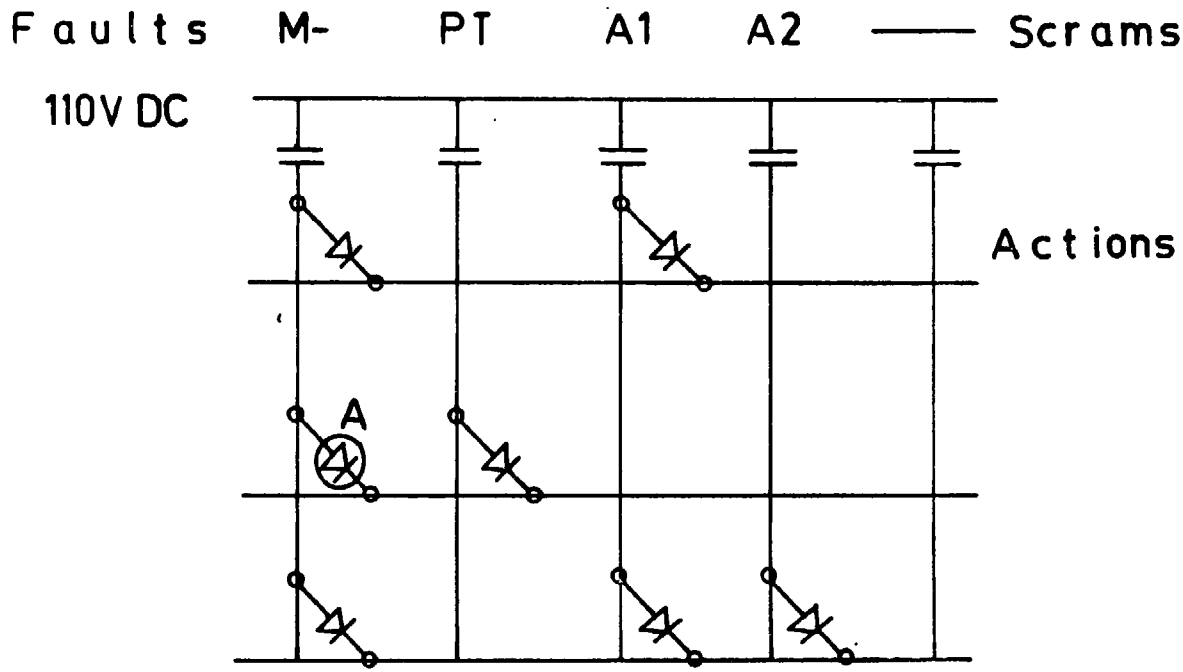
respectively). DC-DC convertors have also failed a no. of times but have been repaired locally. However, PLC cards are not recommended to be repaired locally for they are multi-layer PCB based, and though it may be possible to repair them for apparently satisfactory working for the time being, it is indicated by the vendor that it can give rise to subtler problems later. The matter is under investigation by the vendor.

7. CONCLUSION :

The problems referred above could normally be sorted out in a much quicker manner but for the fact that the vendor is located in W.Germany with practically no support in India. It is mentioned that, at the time of procurement, the foreign vendor had almost finalised a collaboration venture in India, and it was expected that after-sales service will be available indigenously which has not happened that way. The aspect of availability of sure support indigenously or alternatively ofother quick and reliable means to get after-sales service cannot be over-emphasized.

A1. Cycle Sequence in a PLC with increased availability & Safety features





Diode Matrix
Scheme used in Kota
< Fig.1 >

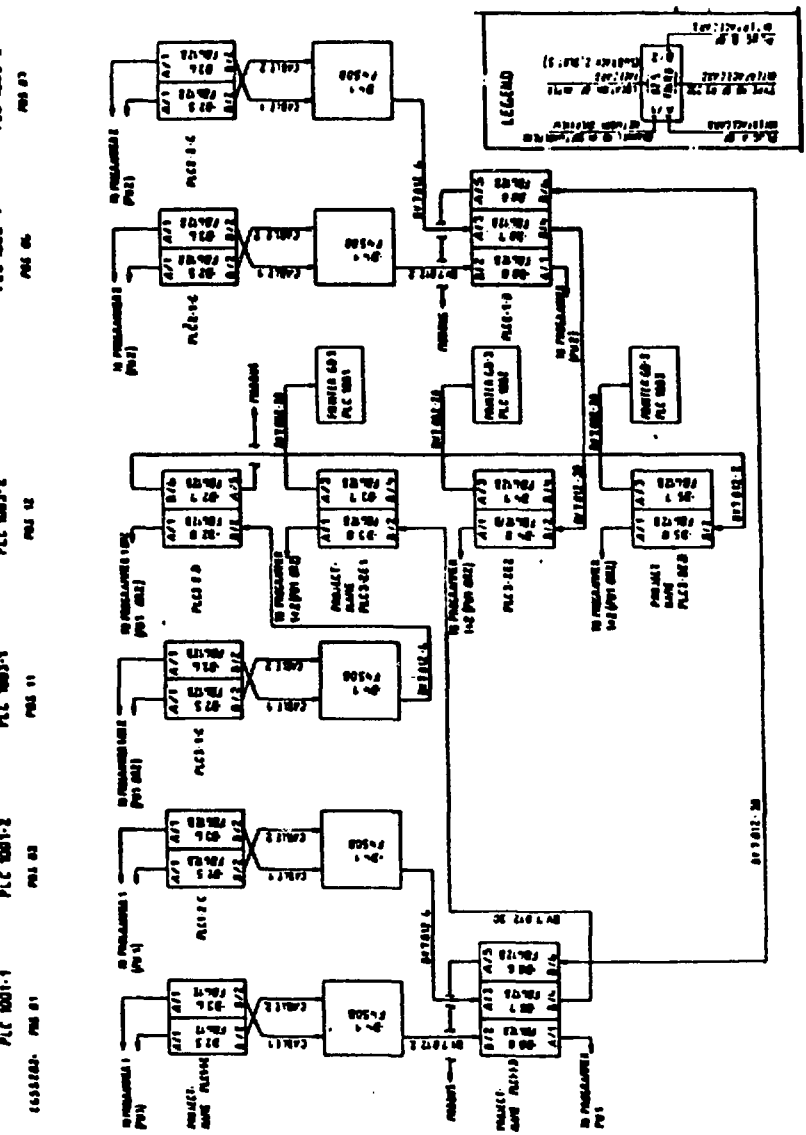


Fig. 2

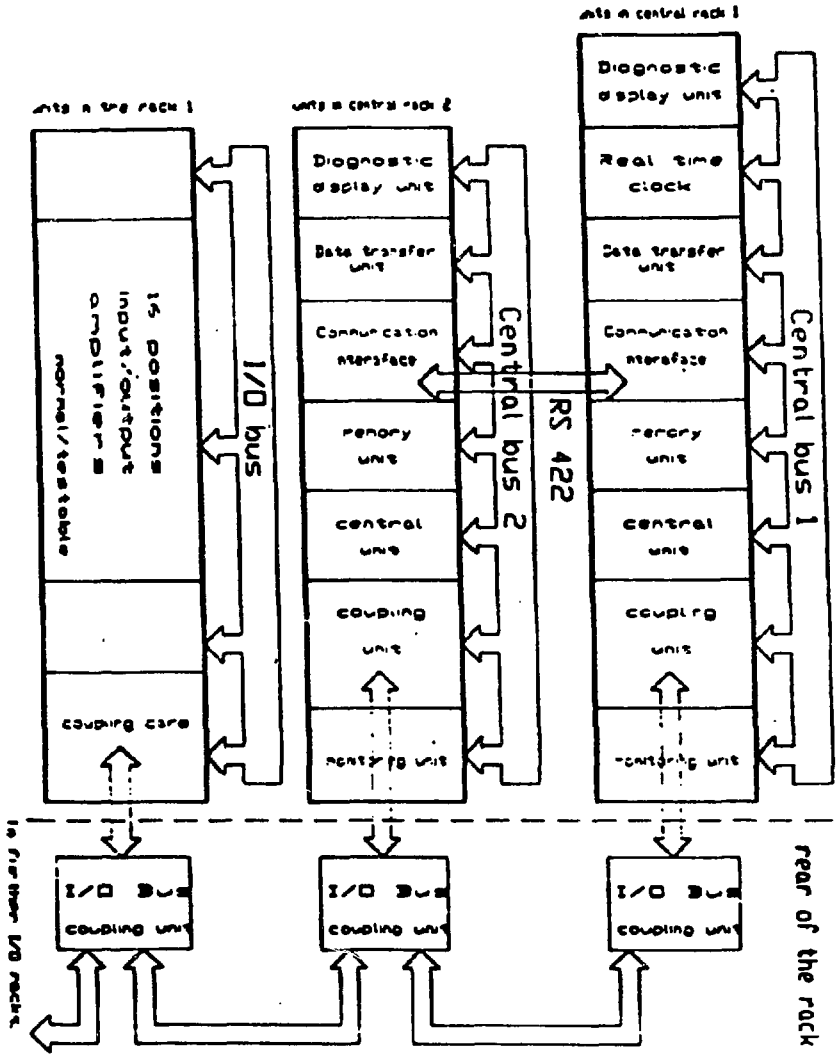


FIG. 3 STRUCTURE OE THE PLC·