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Control Units for APS Power Supplies*

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Abstract

The Advanced Photon Source (APS) accelerator facility is made up of five major subsystems in addition to the linac: the positron accumulator ring (PAR), low energy transport (LET), booster synchrotron (SYNCH), high energy transport (HET), and the storage ring (SR). Each subsystem has multiple magnet and power supply combinations, some requiring multiple modes of operation. These magnet and power supply combinations are computer controlled and monitored. The power supply control unit (PSCU) is the first layer of hardware and software directly above the power supply itself and is described in this paper. The description includes the basic philosophy for each mode of operation and how it influences the topology and means of implementing control. The design of the analog reference blocks (ARBs) influenced the design of other custom functions as well as the feedback controls for vibration and other dynamic corrections. The command set supported by the PSCU is discussed.

I. INTRODUCTION

Four basic ideas form the control philosophy that determined the design of the power supply control unit (PSCU): 1) buy commercial rather than build, 2) use optical/fiber transmission for digital signals, 3) use differential twisted shielded pairs for short off-card analog transmission, and 4) control analog reference via pulses to an UP/DN counter feeding the reference digital-to-analog converter (DAC) to improve noise rejection. The PSCU is the first layer of hardware and software above the power supply itself. A typical rack with eight power supplies is controlled by one PSCU. Each PSCU is connected to the host computer via a two-tiered local area network (LAN) (see Figure 1).

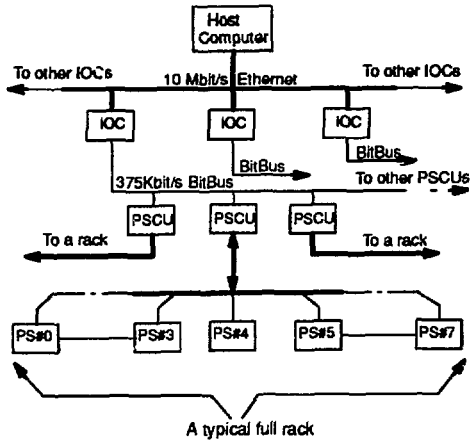

Figure 1. APS Control Hierarchy

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The host computer is connected via a 10-MBit/sec Ethernet LAN to VME-based Input/Output Controllers (IOCs) distributed around the accelerator facility. The IOCs are connected to the PSCUs and other field instruments by a 375-KBit/s master-slave BitBus network. Each PSCU is connected to the power supplies it controls via custom cabling. The Ethernet and BitBus networks are implemented with optical fibers. All digital signals from and to the PSCU are optically coupled to improve noise immunity. To reduce the number of cables between the PSCU and the controlled power supplies, serial transmission of digital signals is used. Analog signals with 10-bit or less resolution are transmitted and received differentially using twisted pairs. A key function block is the analog reference block (ARB) located in the remote DAC/ADC board (see Figure 2). This design results from implementation of the fourth idea of the control philosophy, i.e. analog reference should change only as a result of counting UP/DN pulses to assure smooth changes in the reference voltage.

1.1 Hardware

The PSCU is a 680xx microprocessor-based system housed in a 16-slot Eurocard chassis using a G-6-64/G-96 compatible bus. A 250-watt, built-in power supply provides ±12 V and +5 V power to the chassis. The compatible cards (commercially produced by GESPAC Inc. [1] of Mesa, AZ and custom-made (see *) by ANL) for a typical full rack configuration are:

Items	# of Cards
CPUCard with memory	1
BitBus Adapter	1
Differential input analog card	2 (32)
Opto Coupled digital In	2 (64)
Opto Coupled digital out	2 (64)
16-bit timer card *	2 (4)
Arbitrary Fnc Gen (AFG) *	2 (4)
ADC/DAC Intf *	1 (8)

1.10 CPU Cards (GESSBS6-A, Gesmpu-30H)

The booster synchrotron has four types of dynamic supplies, namely: dipole, quadrupole, sextupole, and correction supplies. A MC68030 25-MHz CPU board Gesmpu-30H is used for these. All other supplies use an MC68000 16-MHz CPU board Gessbs6-A.

1.11 BitBus Adapter

This card is the interface to the 375-KBit/s network between the IOCs and all PSCUs. This master/slave network implementation was chosen for its simplicity but with a standard communication protocol (transparent error correction).

1.12 Differential ADC (GESADC-3)

This unit provides 16 analog channels with differential inputs. It is built around an Analog Devices AD576 (12-bit ADC)

and a unity gain, high voltage, common mode instrumentation amplifier (Burr Brown INA117). Its conversion time is 35 μs.

1.13 Digital Inputs (GESINP-2A)

Thirty-two optically coupled digital signals are connected to this unit via two 26-pin connectors. The nominal input level required is 12 volts for a HIGH and 0 volt for a LOW. Isolation is rated at 1500 V.

1.14 Digital Outputs (GESOUT-3A)

Thirty-two optically coupled digital signals are output from this unit via two 26-pin connectors. It has a power-on reset only. Resetting the CPU board will not affect its output states. The open collector output lines can drive up to 100 mA. The voltage rating of the output transistor is 24 V. Isolation is rated at 1500 V.

1.15 Timer Card (Custom)

Two 9513 counter chips together with an 8-bit digital I/O for control and monitoring are provided. This card generates a programmed number of pulses for four power supplies. The power supplies can be programmed individually, generating the pulses upon receiving the software command (SyncMode=0), or as a group, waiting for an external trigger (SyncMode=1) before delivering the pulses. This card also provides the two quadrature clock pulse trains used by the pulse width modulated (PWM) chopper supplies. Its output consists of differential line drivers for optical couplers to provide isolation and reduced interference pickup.

1.16 ADC/DAC Interface (Custom)

This unit accepts pulse train input from up to eight remote ADCs/DACs. This allows the monitoring of analog signals of higher precision than that provided by the GESADC-3 described earlier, such as transductor or shunt signal. It enables the readback of the reference DAC's digital input. This card also allows selection of the control source for the DAC's input from the PSCU or some other external source (such as the Diagnostics group).

1.17 Arbitrary Function Generator (Custom)

The design of this arbitrary function generator (AFG) card is based on the design described in a paper published in the 1991 PAC Proceedings entitled "Arbitrary function generator for APS injector synchrotron correction magnets," [2]. The design is constrained by the way the analog reference block works. The idea is to control gating of the UP/DN pulses to the DAC counter in order to direct the analog output of the DAC to follow the desired function. The information that determines if a pulse is allowed to reach the UP/DN counter as well as the direction (up/dn) information is stored in a first-in-first-out (FIFO) memory of the appropriate depth.

It is worth mentioning that only two bits of information are needed to encode a point in the waveform for any DAC resolution compared to a full n-bit requirement for the conventional AFG design. As a consequence, the standard 9-bit FIFO can store information for four channels. This card is used to generate the reference analog voltage required by the dynamic supplies of the injector synchrotron.

1.2 Software Modules

The embedded application software that runs in the PSCU is a multi-tasking program written in the C language under Microware's OS-9 operating system. The modules that make up the application are the **main**, **my_defs.h**, **pscu_9513.h**, **shmem.h**, **rs232**, and **bitbus** modules. These modules, when compiled and linked together, produce the executable code burned into the application EPROMs.

1.20 **main** This module initializes the hardware and software states of the PSCU. It creates the shared data block **shmem** and also forks (creates) the two tasks **rs232** and **bitbus.**

1.21 **my_defs.h** This module contains defined constants global to the program, such as board ID numbers, control port, and data port addresses for all cards in the PSCU.

1.22 **pscu_9513.h** Constants for programming master registers as well as counter mode registers for all timers are contained in this module.

1.23 **shmem.h** This is the data module created by **main** as part of program startup. It is a global module.

1.24 **rs232** and **bitbus** These are the two tasks that support the full operation of the PSCU. The **rs232** module supports the use of RS232-C for local control of the PSCU after local control is granted by the host while **bitbus** is intended for normal operation.

1.3 Command Set

All commands are associated with a power supply number. The standard command syntax of a PSCU command is: *command* <power supply #> <argument0 argument1 ...argument*n*>. Below is a partial listing of the commands.

rampto <ps> <value>
Ramp <ps> to <value> where <value> is a decimal integer (i.e. 9000).

setrate <ps> <ramprate>
Set ramp rate divider of <ps> to <ramprate> where <ramprate> is an integer

setbyte <ps> <hexval>
Set control byte of <ps> to <hexval> where <hexval> is a hex byte (i.e. 8f).

getsb <ps>
Print hex byte content of input port.

showstate <ps>
Print summary of <ps> database contents.

calibrate <ps>
Calibrate precision ADC of <ps>.

getrb <ps> <rb>
Perform A/D conversion and print result in hex format where <ps> is 0–7 (–1 means all), <rb> is 0–4 (–1 means all).
0 means precision ADC (5 chars printed),
1–4 means 12bit ADC (4 chars printed).

getdac <ps>
Print hex value of hardware DAC input.

setaf <ps> <npts> <time value pairs>
Set arbitrary function for <ps> with <npts>

time value pairs. <time value pairs> are the data points to specify.

setbias <ps> <bias>
Set arbitrary function for <ps> to <bias> bias value.

II. GENERAL OPERATION

Figure 2 shows the typical magnet power supply control chain that starts from the VAX or SUN host, to the IOC, to the power supply control unit, down to the regulator and signal conditioning block. The PSCU communicates to each power supply using optically coupled digital signals and differential shielded twisted pairs for analog signal transmission.

The BitBus command packet transmitted to the PSCU contains the node address (rack number), the command code, power supply number ID, and the required parameter bytes appropriate for the command as well as the bytes required for the host communication protocol. The node address selects one of the 221 cabinet racks on top of the storage ring tunnel. Each rack has one PSCU that handles the operation and monitoring of six to eight magnet/power supply pairs.

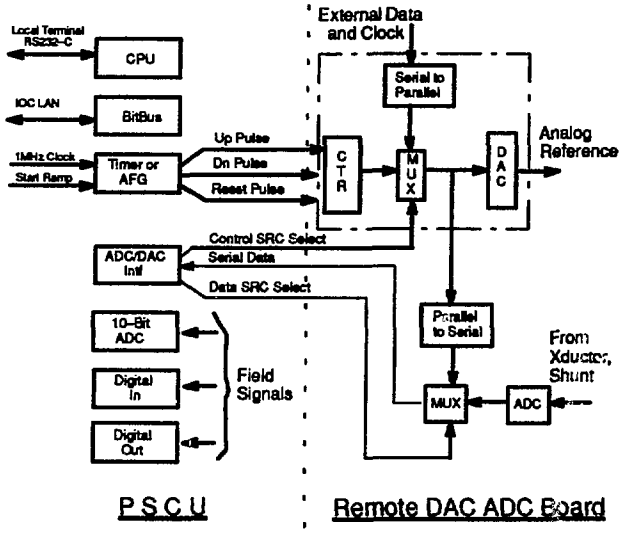

Figure 2. Signals between PSCU and a Typical Power Supply

When a command is received from the host via the LAN, the PSCU receives an interrupt from the communication hardware. The message is sent according to a specific format, decoded into its various components (command, power supply #, and appropriate parameter values), and used by the embedded PSCU software to execute the command. All commands received are compared to a table of commands supported by the particular PSCU; an invalid command results in a null operation.

III. CONCLUSION

The control unit designed for the APS power supplies tried to follow the control philosophy outlined: buy rather than build, use optical/fiber coupling for digital signal transmissions and differential twisted shielded pairs for short off-card analog transmission, and control analog reference via UP/DN pulses to a counter feeding the reference DAC. For certain functions, the desired features can only be supplied by custom design as in the cases of the Timer card, ADC/DAC interface card, and the AFG card. However, custom design has allowed the use of dense, electrically programmable logic devices (EPLD) [3] that has resulted in reduced component counts which should, in turn, improve overall system reliability.

IV. REFERENCES

[1] GESPAC, Inc. 1987 G-64/G-96 Data Book Interfaces.

[2] O. D. Despe, "Arbitrary Function Generator for APS Injector Synchrotron Correction Magnets," 1991 IEEE Particle Accelerator Conference Proceedings, Vol. 3, p. 1461, 1991.

[3] Altera Corporation, 1990 Data Book.