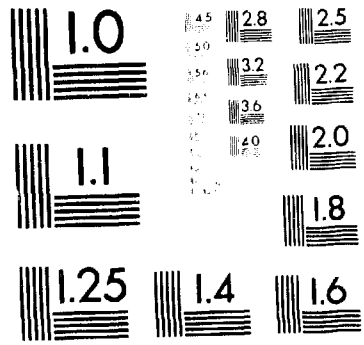
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PROGRESS ON THE DESIGN OF A DATA PUSH ARCHITECTURE FOR AN ARRAY OF OPTIMIZED TIME TAGGING PIXELS

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ABSTRACT

A pixel array has been proposed which features a completely data driven architecture. A pixel cell has been designed that has been optimized for this readout. It retains the features of preceding designs which allow low noise operation, time stamping, analog signal processing, XY address recording, ghost elimination and sparse data transmission. The pixel design eliminates a number of problems inherent in previous designs, by the use of sampled data techniques, destructive readout, and current mode output drivers. This architecture and pixel design is directed at applications such as a forward spectrometer at the SSC, an e^+e^- B factory at SLAC, and fixed target experiments at FNAL.

INTRODUCTION

Pixel devices, in particular PIN diode arrays, are a natural choice for vertex detectors. These devices provide three-dimensional coordinate information with spatial resolution of a few microns, and so provide efficient track finding with a minimum number of layers. Much effort has gone into the development of pixel arrays which correlate the time-of-arrival of a charged particle with its address, in terms of rows and columns, and the pulse height left by the charge traversing the detector [1,2]. Recent improvements in design have been effected to include a data-push feature which allows the detection of the particle itself to initiate the read-cycle [3,4,5]; these design improvements are reported here.

The development of the data push architecture (DPA) was motivated by two goals: first, having a simple, rugged, small chip periphery, resulting in a high fill factor; and second, the desire to have the silicon vertex detector participate in the trigger. These goals have been achieved, at least at the design level, while retaining important features of previous arrays—such as exceptionally low noise operation, time stamping, analog signal processing, XY address recording, ghost elimination, and sparse data transmission.

The data push pixel and a number of related analog circuits will be submitted to MOSIS in early June 1993. The design of these test chips was guided both by simulation and by experience gained in previous work on the Hughes CHIP 5 array, a 32×64 array of time tagging pixels. Simulation shows the input noise performance of the DPA pixel to be approximately 150 e^- rms. The size of the pixel is 30 μm× 135 μm, and the details of this layout are presented. The expected spatial resolution from an array of pixels of this size is deduced from actual test data from arrays having 30 μm^2 pixels, and is presented briefly as well [6]. Lastly, actual data from Hughes CHIP 4 relating to time walk are presented, and improvements in the DPA design relating to time walk are discussed.

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HYBRIDS

Figure 1 is a schematic of a silicon array hybrid. The charged particle detector, a silicon PIN diode array, and the readout electronics are constructed as two separate silicon chips, each optimized for its specific function. The two chips are then indium (or solder) bump-bonded together to form the array hybrid.

An earlier hybrid—designed in cooperation with the Hughes Aircraft Company, comprised of 256×256 pixels, each 30 μm^2—was tested by placing three arrays configured as a beam telescope in a 450 GeV/c beam of muons at Fermilab [6]. Figure 2 is a residual plot for muons at normal incidence demonstrating a resolution (σ) of 2.6 μm in both transverse coordinates. A publication is in progress demonstrating the resolution of these devices at other than normal incidence. Sherwood Parker and his colleagues have demonstrated spatial resolution of less than 7 μm at angles of up to 56° to the normal [7] for pixel detectors of a size similar to that of the DPA pixel.

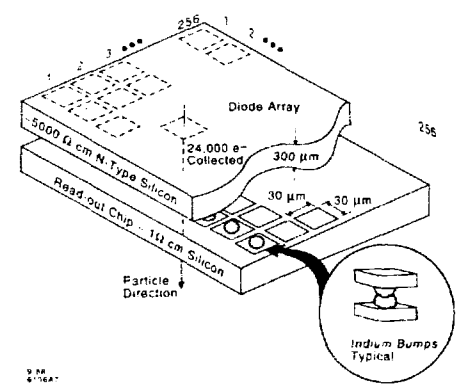

Figure 1. Schematic representation of a hybrid detector showing the two separate silicon chips and their bump-bond interconnects.

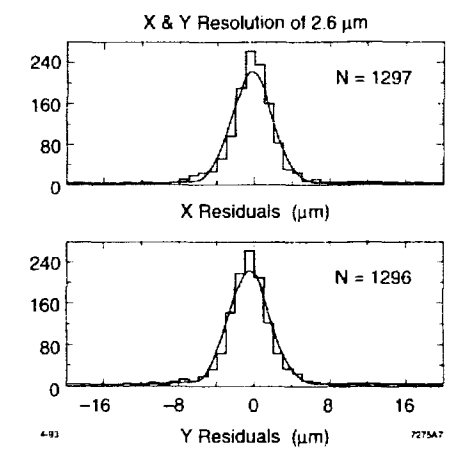

Figure 2. Residual plot for straight tracks traversing three detector hybrids at normal incidence that demonstrate 2.6 μm (σ) spatial resolution in both transverse dimensions.

THE DATA PUSH ARCHITECTURE (DPA)

The data push architecture (DPA) was developed both:

- to simplify the digital periphery of the detector array—compared to previous designs developed for use at the SSC's central detectors—and thereby increase the fill factor (detector array area/total silicon area) and yield of the readout chip, and
- to make the data available to participate in a vertex trigger.

The DPA allows the detection of the high energy particle to initiate the read sequence, sending the address of the "hit" in terms of rows and columns within the array, the time of arrival, and the pulse height reflecting the energy deposited by the detected particle onto a data bus for use by the data acquisition system and/or

trigger system. The pixel size in this first attempt at a DPA pixel is 30 μm×135 μm. A column is a stack of pixels whose base is 135 μm, and the row is the orthogonal direction.

The most significant feature of this design is, therefore, the specification that the maximum time necessary to completely read out one "hit" should be less than 200 ns. A "hit" is defined to be the pixel containing most of the charge deposited by the particle and the two adjacent neighbors within the same column. To achieve this throughput specification, the pixel's digital periphery employs sparse scanning, self clocking, and priority selection.

The DPA retains the ability to eliminate "ghosts" (false hits which can occur when there are multiple interactions within an array at the same time). The digital periphery is designed to transmit only bone-fide hits, no zeros, and no ghosts. The DPA design has eliminated a number of problems inherent in previous designs as well. The effects of threshold mismatches and nonuniformities have been reduced by the use of sampled data techniques to reset the pixel discriminator. The use of a destructive readout rather than storing the pulse height for later retrieval insures its integrity and reduces the parts count within the pixel. Crosstalk due to large voltage swings on traces which abut adjacent pixels has been virtually eliminated by the use of current mode output drivers. Chip dead time has been reduced to a minimum by the infrequent need to reset the front-end amplifier.

Figure 3 is a block diagram of the data push architecture, highlighting the role of the pixel in generating the "HIT" pulse which starts the read cycle. A FIFO four deep is included in the column logic to act as a buffer should additional hits arrive before the read cycle has processed the current hit.

Figure 4 is a block diagram of the data push architecture which emphasizes the analog functions of the design. Details of the timing diagram and the various analog blocks are provided in the references.

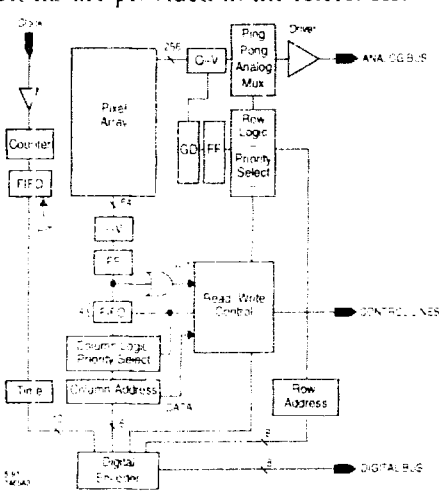

Figure 3. Block diagram showing the data push architecture digital design.

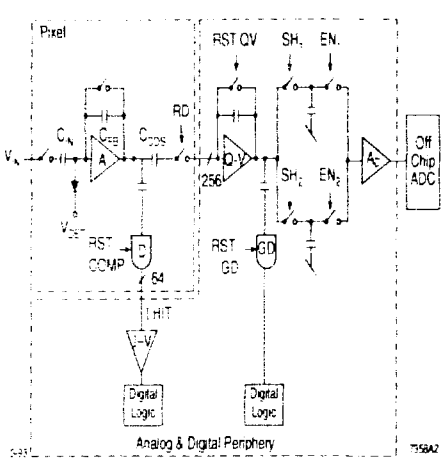

Figure 4. Block diagram highlighting the data push architecture analog design.

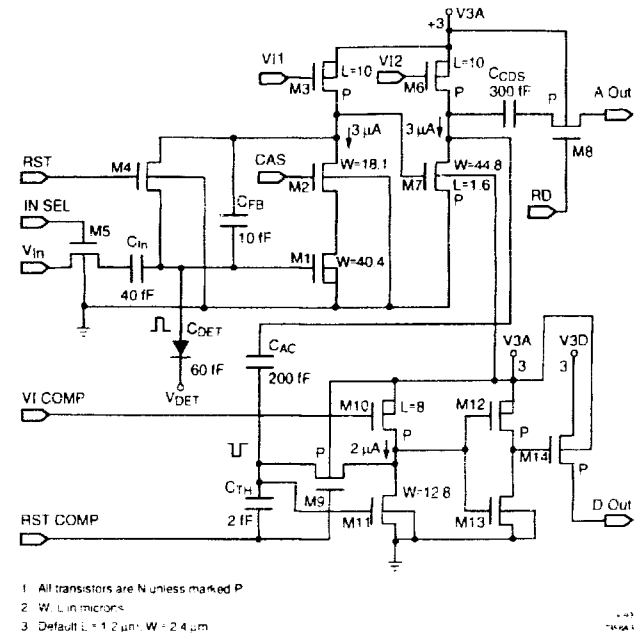

Figure 5. Transistor level schematic of the data push unit cell showing 14 FETs, 5 capacitors, and 14 lines.

Figure 5 is a transistor level schematic of the unit cell, while Fig. 6 is a layout showing all of the various layers with the transistors, control lines, and biases clearly labeled. The unit cell has been laid out following the HP 1.2 μm double-metal-single-poly design rules for fabrication by MOSIS.

The input amplifier is a single stage cascoded inverting amplifier followed by a buffer stage. The feedback capacitor is 10 fF, corresponding to 16 μV/e⁻. Thus, a minimum ionizing particle passing through 300 μm of silicon produces about 0.4 V at the preamp output. The input stage is AC-coupled to the analog storage section via C_{cds} and the comparator via C_{ac}. After the detection of the first hit in a pixel, the analog storage block and the pixel comparator are reset for all pixels in the column, but the front end amplifier need not be reset. This avoids array dead time! As there is about 2 V of dynamic range, each pixel can be hit a number of times before a reset is needed.

The capacitor C_{cds} is the correlated double sampling capacitor whose function it is to eliminate the $\sqrt{kT/C}$ noise associated with the resetting of the 10 fF capacitor (about 40 e⁻). It is also useful in reducing 1/f noise.

Crosstalk, always an issue in small geometry circuits, has been addressed by placing the RST-COMP line in the center of the pixel, far from the sensitive front end and separated by six metal lines from the front end of the adjacent pixel.

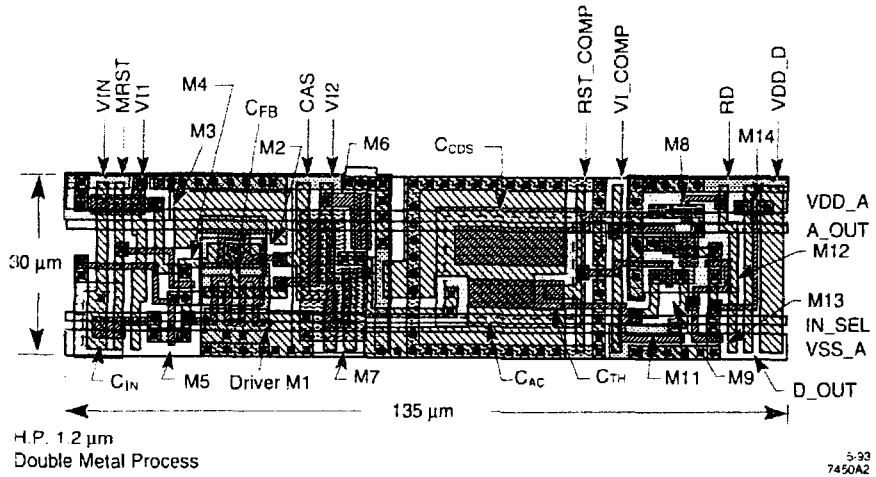

Figure 6. Layout of the unit cell in the HP 1.2 µm double-metal–single-poly process measuring 30 µm × 135 µm is shown, with its transistors, capacitors, and lines called out.

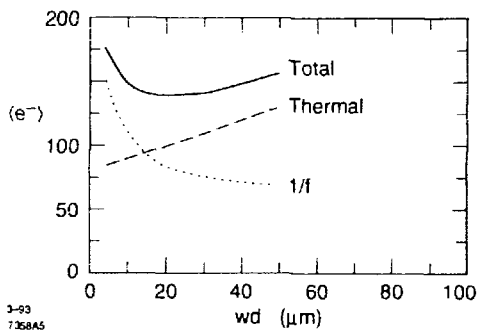

Figure 7. Computer simulation of the expected input referred noise showing that for our choice of input gate width 150 e^- noise is predicted.

Figure 7 is a simulation of the two major components of input referred noise as a function of the input transistor (M_1) width. This width has been set to 40 µm.

Figure 8 is a plot of time walk as a function of input charge, for the Hughes CHIP 4 array, one of our early efforts. For this pixel, there was a time walk of about 280 ns from twice threshold (4,000 e^-) to twelve times threshold (24,000 e^-). This pixel had 1 µA of standing current in the amplifier and 0.4 µA of standing current in the comparator. Our DPA pixel will have 3 µA standing in the amplifier and 2 µA in the comparator, and will surely be faster, resulting in less time walk. In the DPA concept, the analog information is available to perform a timing correction. Figure 8b shows that even with a time walk as bad as that in the CHIP 4 pixel, we can achieve 30 ns resolving time if we measure the analog information to ±3%, which is all the accuracy we need to achieve superb spatial resolution.

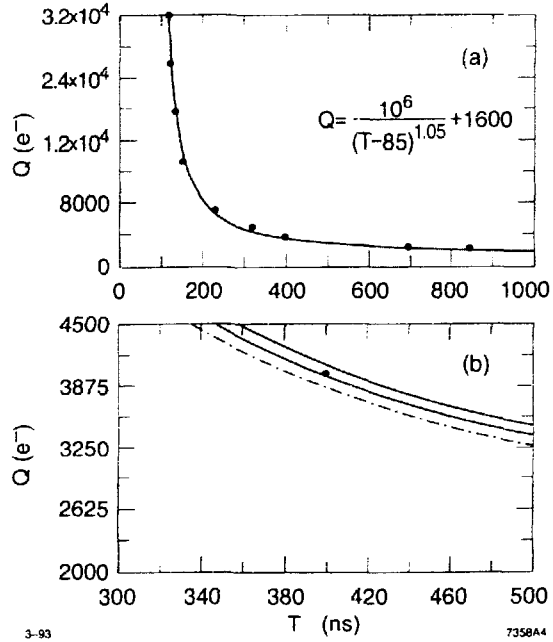

Figure 8. (a) plot of time walk versus input charge representing data taken from the Hughes CHIP 4. and (b) plot showing that the effect of measuring pulse height to four bits (±3%) is adequate to resolve the time-of-arrival to about 30 ns, even if the time walk is as bad as that of CHIP 4.

The operating cycle of the chip begins with the pixel comparator firing on the detection of the particle. It generates a current and sends it to the current-to-voltage converter (I-V) at the column periphery. The I-V causes a HIT signal to be generated by the digital logic, which records the time and address of the hit and generates the read (RD) to the effected column. The analog information from the entire column is sent to the row periphery, where it is received by the charge-to-voltage converter (Q-V), and these voltages stored on the ping-pong multiplexer for ultimate transmission off chip.

The ghost discriminator senses this analog information and places a pattern of hits into the row registers. Then the column is reset (the pixel comparator, I-V, Q-V, and GD). During this time, the analog information is being sent off chip, and the column logic is preparing to handle the next column's hits. The column reset process causes a column dead time of about 100 ns. Additional details of this process are available in the references, as are discussions about radiation hardness and the treatment of hot pixels.

Figure 9 is a schematic of the test chip being readied for submission to MOSIS in June 1993. This chip includes the unit cell (UC), the charge-to-voltage converter (Q-V), the ghost discriminator (GD), the current-to-voltage converter (I-V), and a number of transmission gates to allow the testing of individual sections of the test chip. Figure 10, a second test chip consisting of a 4x4 array of unit cells and a simplified periphery, is also being readied for submission.

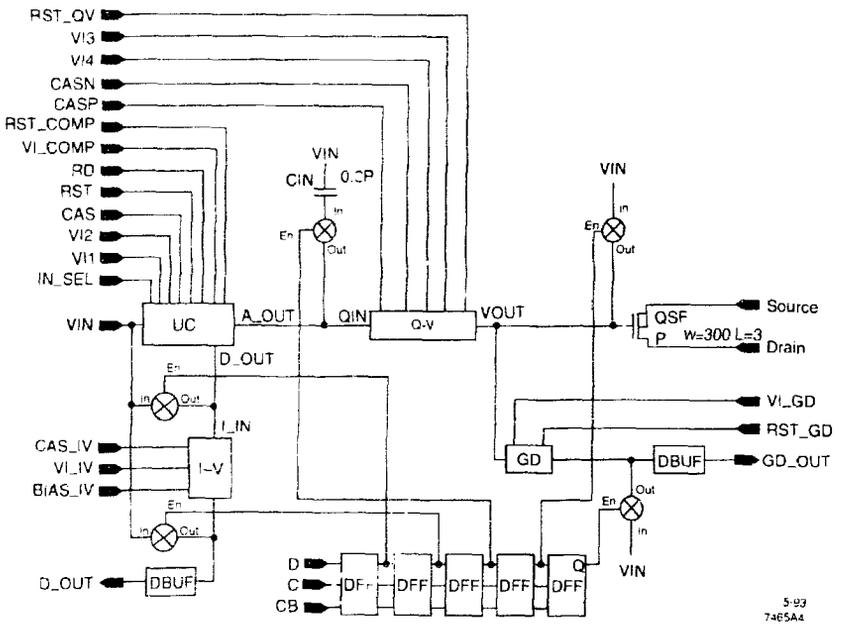

Figure 9 Schematic diagram of the test chip being readied for submission to MOSIS containing the new unit cell, the current-to-voltage converter, the charge-to-voltage converter, the ghost discriminator and a number of transmission gates that allow testing of individual functional blocks.

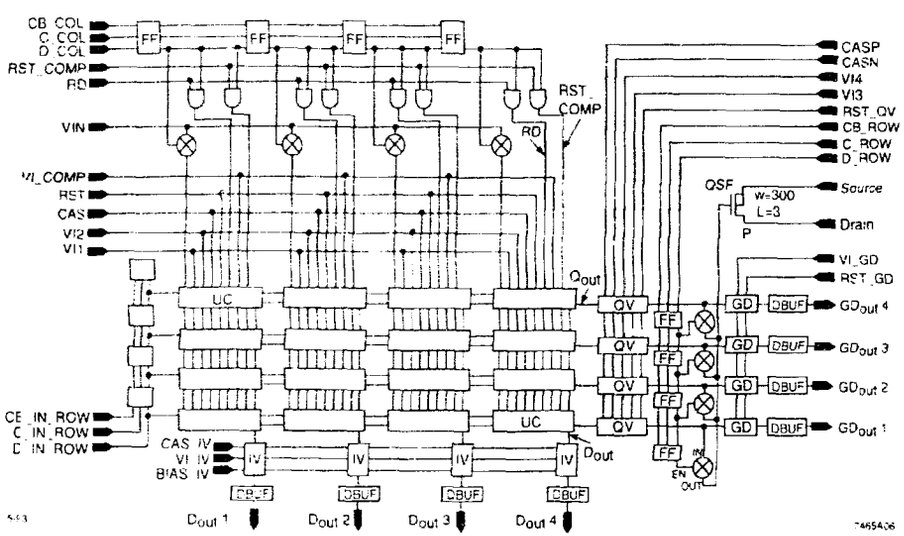

Figure 10. Schematic diagram of the 1.2 test chip being submitted to MOSIS.

SUMMARY

A summary of the design specifications for the first array based on our design efforts to date is presented below; many improvements and corrections will ultimately be made.

SUMMARY OF DESIGN SPECIFICATIONS	
Pixel size	30 μm x 135 μm
Throughput	< 200 ns
Time walk [4–50 ke⁻]	< 250 ns
Noise [input referred]	< 200 e⁻
Gain	16 μV/e⁻
Pixel comparator reset	< 100 ns
Chip reset	< 1000 ns
Pileup	> 3
Settling accuracy	4 bits or 6%
Threshold of pixel comp	800–2400 e⁻
Power/pixel	< 30 μW

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